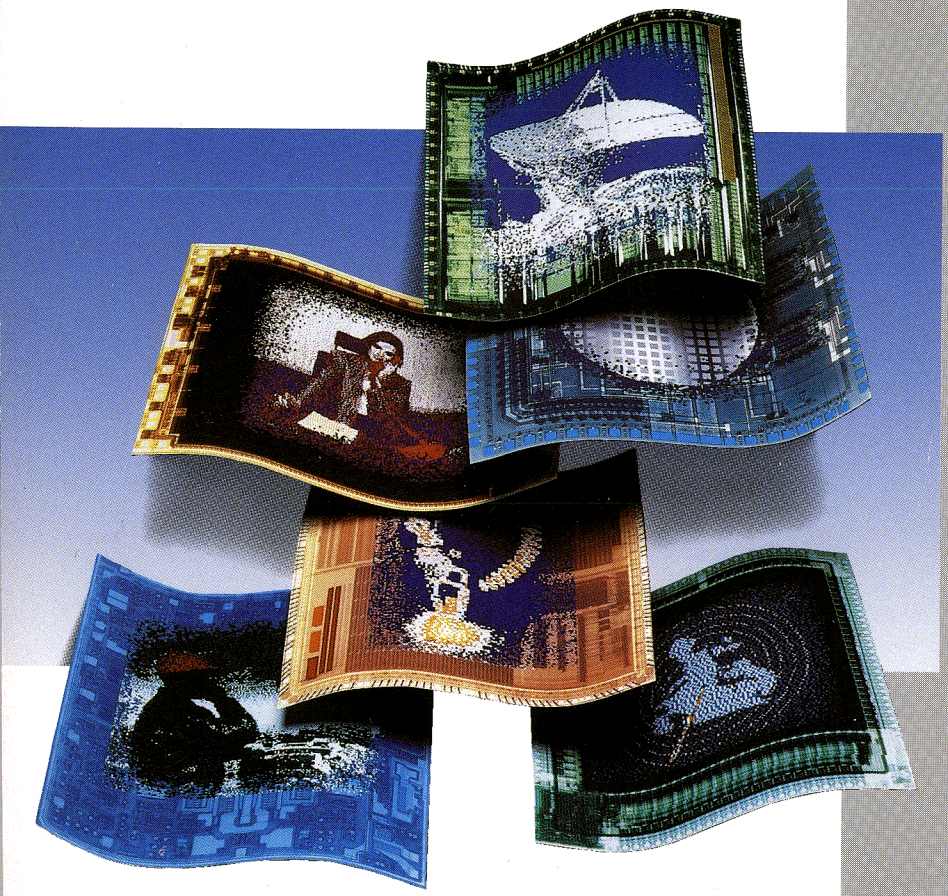
Telecoms

IC Handbook

February 1994



GEC PLESSEY
SEMICONDUCTORS

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TELECOMS

IC Handbook

GEC PLESSEY

SEMICONDUCTORS

Foreword

GEC Plessey Semiconductors is committed to the development of highly sophisticated and innovative products for the Telecommunications Industry.

Technical experience and close links with major equipment manufacturers have resulted in a wide range of IC products ideally suited to all aspects of telecommunications equipment, from Central Office and PBX to Subscriber.

Dedication to customer needs is demonstrated by a range of high voltage bipolar SLIC (Subscriber Line Interface Circuit) devices, designed to cater for a variety of line lengths and conditions.

To complement the SLICs, the low voltage CMOS MV3010-1 SLAC (Subscriber Line Audio Circuit) brings the accuracy and repeatability of DSP (Digital Signal Processing) to the traditionally analog line card. Significant benefits of the DSP approach include a greater degree of flexibility and the ability to adapt automatically to different line conditions. The rigorously tested and completely robust echo cancellation algorithm ensures dynamically that optimum Echo Return Loss is achieved over a wide range of line lengths and terminating impedances. The GPS combination of SLICs and SLAC is believed to offer the ulimate high performance, cost effective, line card solution. The unique features of the SLAC can also be used to good effect in mobile applications where unwanted echos at the 2 to 4 wire interface cause problems in the RF interface.

In addition to innovative new products, GPS offers a comprehensive range of industry standard devices, including Pulse, DTMF and switchable Pulse/DTMF Diallers (approved in most European countries), Codecs, Digital Switch Modules and PCM circuits (up to 8Mbits) with a custom design option - all backed up by a dedicated customer support team.

GPS is continually assessing the needs of equipment manufacturers and is actively engaged in carrying out an expansion of its range of products for the future needs of the Telecommunications Industry.

Personal Communications

GEC Plessey Semiconductors has also created a range of products specific to applications in the growing markets for radio-communications equipment (such as CT2, DECT, GSM and radiopagers). Technical details for these devices can be found in the Personal Communications IC Handbook.

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Section 1
Telephone Circuits

GEC PLESSEY
SEMICONDUCTORS

Pulse, DTMF and Dual Mode Dialler ICs - Selection Guide

The GEC Plessey Semiconductors range of diallers is the most comprehensive available, comprising Pulse, DTMF and switchable Pulse/DTMF devices.

The majority of switchable dual-mode Pulse/DTMF diallers are part of a pin-compatible family - allowing a single circuit and PCB design to provide a range of telephones simply by exchanging chips. An extensive selection of mask-programmable options allows each device to offer different dialling parameters, keypad options and protocols for various countries while different output polarities and configurations allow optimisation of telephone design for minimum component cost.

GPS dialler chips are comprehensively tested and quality controlled during manufacture and are used in telephones approved by most European PTTs. All are available in DIL and surface mount miniature DIL packages.

Type number	Dialling mode	Last number redial	Memories	Dedicated memory keys	Member of pin-compatible family	Selectable break/make and IDP options	Timed flash options 100-600ms	Extensive metal mask options	Internal on-hook timeout	Page
MA535	DTMF	✓					✓	✓	✓	9
MA541	LD/DTMF	✓			✓	✓	✓	✓	✓	16
MA544	LD/DTMF	✓	10		✓	✓	✓	✓	✓	24
MA545	LD/DTMF	✓	10		✓	✓	✓	✓	✓	31
MA547	LD/DTMF	✓	10	✓	✓	✓	✓	✓	✓	38
MA548	LD/DTMF	✓	10	✓	✓	✓	✓	✓	✓	45
MA585	LD/DTMF	✓	20	✓(1)	✓	✓	✓	✓	✓	52
MA587	LD/DTMF	✓	20	✓	✓	✓	✓	✓	✓	59
MA5883	LD/DTMF	✓	20	✓(1)	✓	✓	✓	✓	✓	66
MA589	LD/DTMF	✓	20	✓	✓	✓	✓	✓	✓	74
MA525	LD/DTMF	✓	Fully micro controlled, all parameters programmable						✓	82

NOTES: 1. For 10 memories 2. All MA5xx devices use an inexpensive 560kHz ceramic resonator.

MA535

DTMF DIALLER WITH REDIAL

The MA535 is a low power CMOS DTMF dialler with a 21-digit last number redial store.The device is capable of generating all 16 DTMF characters including *, #, A, B, C and D.

The 21-digit LNR store will automatically retain the digits dialled in a call for redial later. A PIN (Personal Identification Number) confidentiality feature ensures that security codes are not retained. The store contents are maintained by a minimal current leaked from the telephone line whilst on-hook.

The MA535 can also generate an accurate Timed Break Recall (Flash) signal and offers a common operating protocol for Earth Loop Recall. Mask options are available for various TBR (Flash) periods and DTMF tone on/off periods.

The oscillator circuit is of the 'single pin' type and requires no external components other than an inexpensive 560kHz ceramic resonator, resulting in substantial cost savings compared with crystal based oscillator circuits.

For applications where tone filtering is required, an onchip unity-gain amplifier is provided, requiring only passive external components to implement a second-order low pass filter.

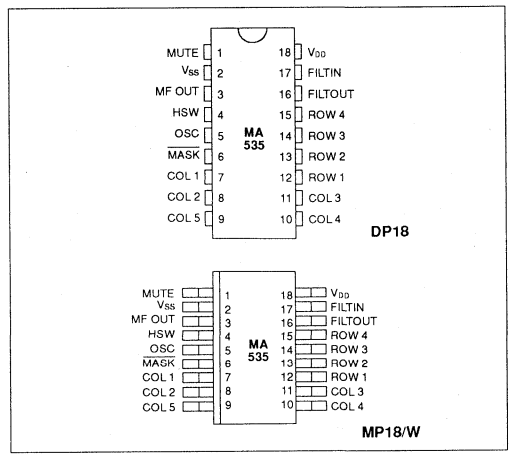


Figure 1: Pin connections - top view (not to scale)

FEATURES

- Full 16 Tone Pairs with Controlled Minimum Tone Burst.
- 21 Digit Last Number Redial.
- Timed Break Recall (Flash)
- Common Protocol for TBR (Flash) and Earth Recall.
- Uses Inexpensive 560kHz Ceramic Resonator.
- Low Power CMOS.
- Mask Programmable Options to suit Application.
- PIN (Personal Identification Number) Confidentiality Feature.
- No Signalling Output for Simultaneous Key Depressions.

PIN FUNCTIONS

Pin number	Pin name	Function
1	MUTE	Output active during keying and tone transmission (see note 1)
2	V_{SS}	Negative supply
3	MF OUT	Unfiltered DTMF output
4	HSW	Hookswitch input - a logic 1 at this pin indicates 'Off-Hook'
5	OSC	Connect a 560 kHz ceramic resonator between this pin and VSS
6	$\overline{\text{MASK}}$	Output used to signal TBR (Flash) (see note 2)
7	COL1	Connections for 20 button single contact keypad
8	COL2	
9	COL5	
10	COL4	
11	COL3	
12	ROW1	
13	ROW2	
14	ROW3	
15	ROW4	
16	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
17	FILT OUT	
18	V_{DD}	Positive supply

1. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.
2. $\overline{\text{MASK}}$ may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.

Table 1: Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA535 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the onhook state is not recognised for 217-224ms. This is so that short line breaks of less than 217ms, such as line reversals applied by the exchange, are ignored. In this case the $\overline{\text{MASK}}$ output will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted. This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic '1' level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a hey is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 6.7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start up time if it was not already running).

	COL 1	COL 2	COL 3	COL 4	COL 5
ROW 1	1	2	3	A	LNR
ROW 2	4	5	6	B	TBR
ROW 3	7	8	9	C	
ROW 4	*	0	#	D	

Figure 2: Keypad layout and connections

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again. Keypad layout and connections are shown in Fig. 2.

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 21 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number.

The last number redial store has several features designed to assist the user.

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the LNR key. In this case, the remainder of the number will be dialled when the LNR key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

PIN contidentiality feature

DTMF signalling is often used for data transactions, where the characters A, B, C, D, * and #, which are not normally required in telephone numbers, are used

To ensure confidentlality of PIN (Personal Identification Number) codes, If a call contains the digits A, B, C, D, * or #. only those digits dialled prior to the first press of either A, B, C, D, * or #, will be retained in the LNR store.

Timed Break & Earth Loop Recall (TBR) (Flash)

The MA535 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the LNR store is cleared. No further digits will be accepted during the current off-hook period.

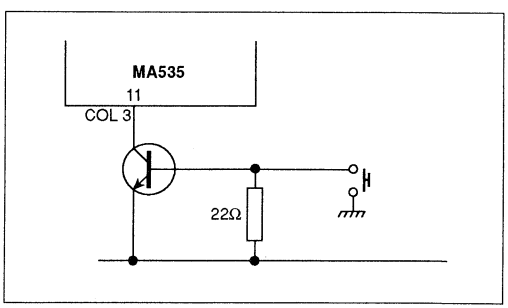


Figure 3: Earth loop recall

A TBR (Flash) of 98ms[1] is generated when the TBR key is pressed. The MASK output goes low in order to produce the line break. The MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin. If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown on previous page in Fig 3, or by use of a double contact switch.

[1] *Other TBR (Flash) periods are available as mask options (see page 1-20)*

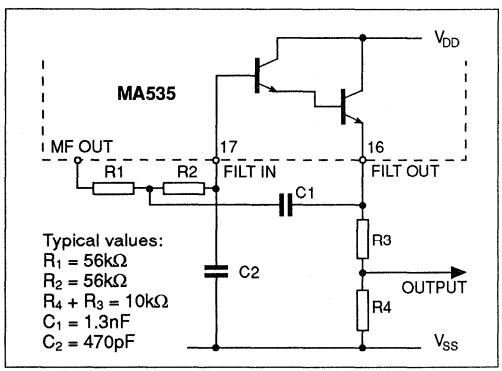


Figure 4: DTMF tone filtering

Oscillator Circuit

This requires an external 560kHz cerarnlc resonator connected between OSC and V_{SS} to provlde a timing reference for all chip functions No other components are required or should be used.

Tone Filtering

The specIral purlty of the DTMF output is sufficlent for rnost applicatiuns However, where lower distortion DTMF tones are requlred, an on-chip darlington pair is provided (accessible vla plns 16 & 17) for use in a low pass active filter

Fig 4 shows !loW a 2-pole Sallen and Key filter can be implemented The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0 5dB.

DTMF DIALLING

During DTMF dlalling the MUTE output goes to logic '1' and remains there for -the duration of the tone transrnission The MF OUT output rises to its DC level of 0.9 VDD at the start of the tone transmission and is kept there between tone bursts This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 98ms on, followed by 98ms off [1] If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate Dialling from the LNR store occurs at the rnaxlmum rate.

If a key is held down for longer than 98 ms, the tone output will continue until the key is released

[1] *Tone on-off periods of 84/84 ms are available as mask options (see page 1-20).*

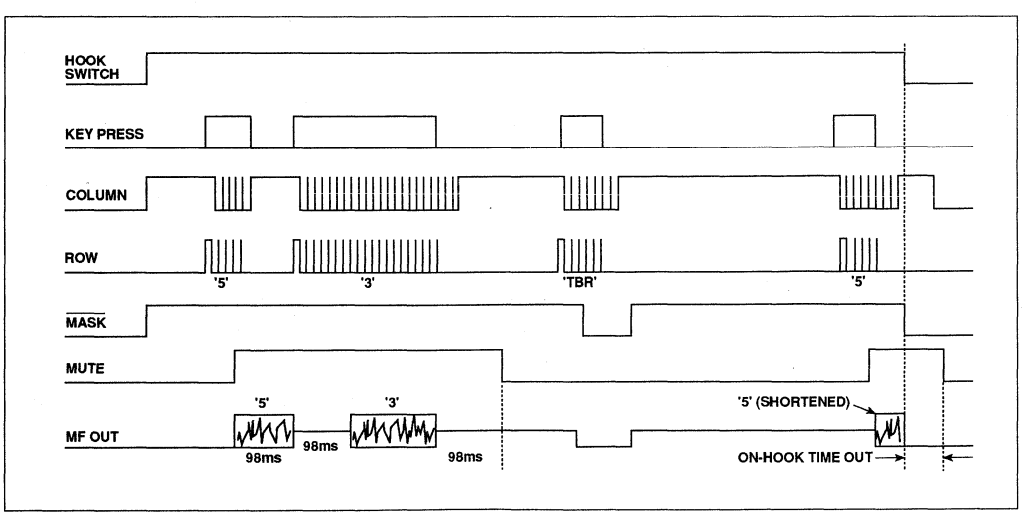


Figure 5: DTMF timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	-0.07	-0.10	+0.19	-0.15	-0.17	-0.20	-0.22	-0.31

Table 2: Tone frequencies

MASK OPTIONS

The MA535 has been designed so that the TBR (Flash) period and DTMF tone on/off periods can be altered quickly and inexpensively at the final stage of manufacture These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit.

The options, listed in Table 3, are possible in any combination. Standard options are listed first in bold italics at 'a'. Other options may be produced by arrangement.

TBR (Flash) period		DTMF tone on/off period	
Option	**Duration**	**Option**	**Duration**
a	***98 ms***	***a***	***98/98 ms***
b	105 ms	b	84/84 ms
c	196 ms		
d	210 ms		
e	294 ms		
f	315 ms		
9	392 ms		
h	420 ms		
i	490 ms		
j	525 ms		
k	588 ms		
l	630 ms		

Table 3: Mask options

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Supply current:	On-hook		<1	5.0	µA	V_{DD} = 2.0V
	Off-hook		1.5		µA	MF OUT low
	MFtone sending			1.0	mA	
Output high voltage (MASK and MUTE outputs)		2.2			V	I = -1mA
Output low voltage (MASK and MUTE outputs)				0.3	V	I = +1mA
MF OUT DC level during tone sending			$0.9V_{DD}$		V	
MF OUT output resistance			3		kΩ	
'Key Pressed' resistance				2	kΩ	2.5V < V_{DD} < 5.7V
'Key Not Pressed' resistance		500			kΩ	2.5V < V_{DD} < 5.7V
Darlington pair current gain (see fig 4)		600	50,000			I_E = 100µA, V_{CE} = 2V

AC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Tone output:	low group	57	64		mV rms	No load. See note 1
	high group		81	91	mV rms	No load. See note 1
High-to-Low group amplitude ratio (pre emphasis)		1.5	2	2.5	dB	See note 2
Total harmonic distortion:	0-4 kHz		1.5		%	
	0-10 kHz		2.5		%	
	0-50 kHz		5.0		%	
	0-200 kHz		6.5	.10	%	
Oscillator start-up time			<0.1	1	ms	

NOTES

1. DTMF tone output level is proportional to supply voltage (V_{DD}).
2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition		Min.	Typ.	Max.	Units	Notes
Supply Voltage:	On-hook	2.0		5.7	V	
	Off-hook	2.4		5.7	V	
Hookswitch input:	On-hook			$0.2V_{DD}$	V	
	Off-hook	$0.8V_{DD}$			V	
Oscillating frequency			560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}-V_{SS}	- 0.3 to + 6 5V
Voltage on any pin (except HSW)	V_{SS} - 0.3V to V_{DD} + 0 3V
Voltage on HSW pin (See note 1)	V_{SS} - 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	±1 mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	-5 to 0mA
Storage temperature	-55°C to + 125°C
Operating temperature range	-10°C to + 55°C

NOTES

1. A diode is internally connected between this pin and VDD. Provided current is externally limited to 300µA max. no damage will occur.

2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

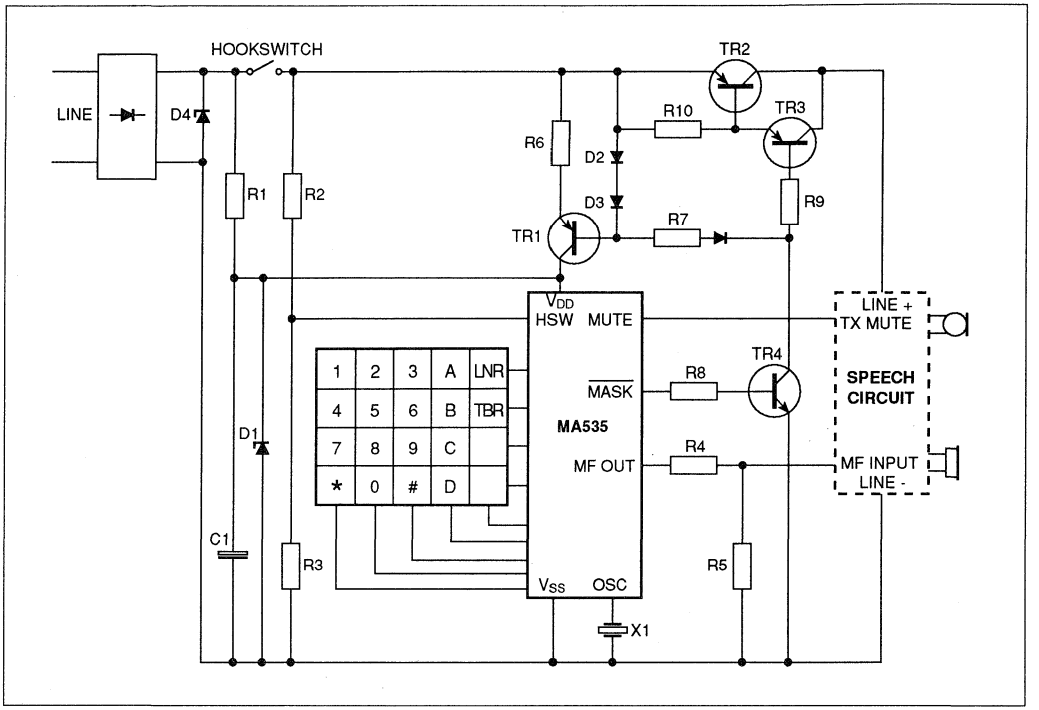


Figure 6: Application circuit 1 (with TBR)

Component	Norninal Value	Function
R1	2.2MΩ	R1 provides current to maintain redial memory whilst on-hook.
R2, R3	560kΩ	R2 & R3 present a logic '1' to the HSW input when the instrument is off-hook.
R4 R5	See function See function	R4 and R5 provide the correct level of tone. When the filter current is incorporated, the sum of R4 and R5 should be between 1kΩ and 10kΩ to allow sufficient bias for the filter amplifier.
TR1 Dl D2, R6 R7	BF423 or MPSA93 2.5V Zener GP Diodes 200Ω 56kΩ	These components provide a stable supply voltage for the MA535. The constant current source delivers a current defined by I x 0.6/R6. The Zener diode (D1) defines the operating voltage and may comprise four BA314 diodes or a BZV462V0 and a BA314.
Speech circuit		The speech circuit of Fig. 6 is used to couple the DTMF lones to line.
C1	47µF	D4 provides current during line breaks.
X1	560kHz	XI is a ceramic resonator which provides accurate timing for the chip.
D4	130V	D4 provides protection from line transients.
D5 R8 R9 R10 TR2, TR3, TR4	GP Diode 4.7kΩ 100 kΩ 6.2kΩ BF423	These components allow the TBR (Flash) signal generated on the $\overline{\text{MASK}}$ output of the MA535 to be coupled to line. During a TBR, the speech circuit is cul off as is the normal supply to the MA535 via TRI, in order to produce a clean line break. During a TBR capacitor CI supplies the MA535.

Table 4: Application circuit 1 components

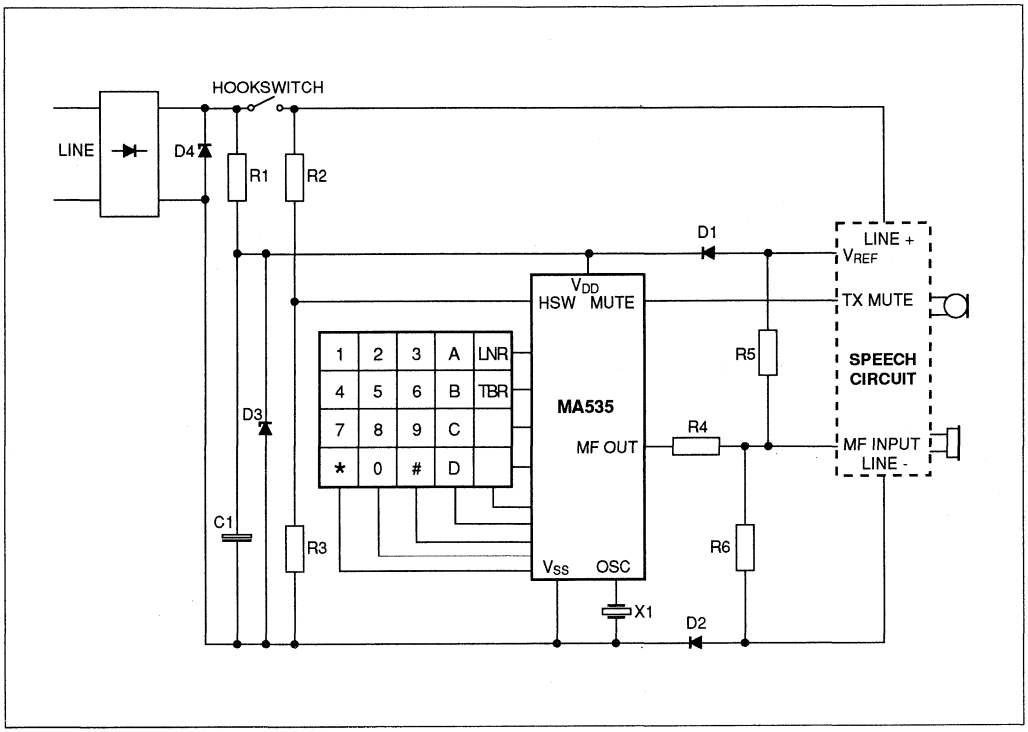


Figure 7: Application circuit 2 (without TBR)

Cornponent	Nominal Value	Function
R1	2.2MΩ	RI provides current to maintain redial memory whilst on-hook.
R2 R3	560kΩ 560kΩ	R2 8 R3 present a logic '1' to the HSW input when the instrument is off-hook
R4 R5 R6	See function See function See function	Resistors R4, R5, and R6 provide a potential divider network to set the tone levels and required DC bias for the speech circuit.
D1	GP diode	DI prevents the speech circuit from taking current from CI or R1.
D2	GP diode	D2 counteracts the voltage drop across D1.
D3	5.6V Zener	D3 is a protection diode.
Speech circuit	Integrated type	The speech circuit is an integrated type, supplying a stable reference voltage for the DTMF generator, and is also used to couple the DTMF tones to line.
CI	47µF	C1 provides current during line breaks.
X1	560kHz	X1 is a ceramic resonator which provides accurate timing for the chip.
D4	130V	D4 provides protection from line transients.

Table 5: Application circuit 2 components

MA541

LD/DTMF SWITCHABLE DIALLERS

The MA541 family are keypad switchable LD/DTMF dialler devices with a last number redial facility.

Two operating modes are available: LD mode, with the ability to temporarily switch to DTMF mode from the keypad during a call, and DTMF only mode. The former mode enables subscribers to access such services as home banking.

The MA541 devices are pin compatible with the GPS switchable dialler families MA526, MA527, MA545, MA547. MA585, MA587 and MA589 - providing a complete range of telephone features within a single PCB and circuit design.

Metal mask and pin selectable options are available to service specific requirements of particular countries and customers.

FEATURES

- Selectable Loop-Disconnect or DTMF Modes
- Keypad Switchable LD to DTMF
- 32 Digit Last Number Redial
- Selectable Make/Break Ratios 2:1 and 3:2
- Uses Inexpensive 560kHz Ceramic Resonator
- Low Power CMOS
- Mask Programmable Options to suit Application
- Timed Break Recall (Flash) and Earth Recall
- Reliable Power-on Reset

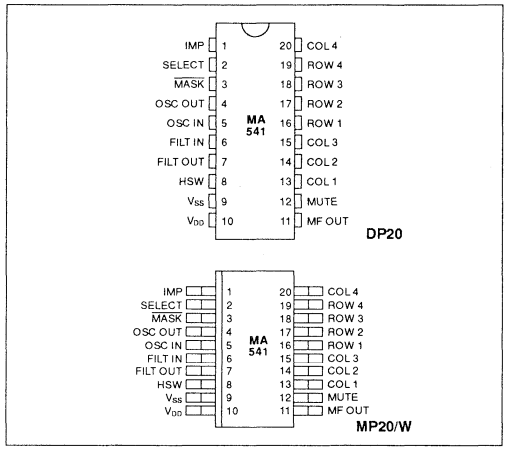


Figure 1: Pin connections - top view (not to scale)

PIN FUNCTIONS

Pin number	Pin name	Function
1	IMP	'Loop disconnect' dialling output
2	SELECT	LD/DTMF selection, IDP and B/M radio programming
3	MASK	Output to disable speech circuit during pulse dialling and recall (see note 1)
4	OSC OUT	Connections for 560kHz ceramic resonator
5	OSC IN	
6	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
7	FILT OUT	
8	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-hook'
9	VSS	Negative supply
10	VDD	Positive supply
11	MF OUT	Unfiltered DTMF output
12	MUTE	Output active during keying and tone transmission (see note 2)
13	COL1	Connections for 16 button single contact keypad
14	COL2	
15	COL3	
16	ROW1	
17	ROW2	
18	ROW3	
19	ROW4	
20	COL4	

1. $\overline{\text{MASK}}$ may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.
2. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1: Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA541 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the onhook state is not recognised for.200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied bv the exchange, are ignored. In this case the IMP and $\overline{\text{MASK}}$ outputs will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted.This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic '1' level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

	COL 1	COL 2	COL 3	COL 4
ROW 1	1	2	3	LNR
ROW 2	4	5	6	TBR
ROW 3	7	8	9	SAVE (1)
ROW 4	*	0	#	TONE (1)

TBR: Timed Break Recall (Flash)
LNR: Last Number Redial
SAVE: Save last number dialled in 'SAVE Store'
TONE: Change dialling mode from LD to DTMF

(1) These keys are only available as mask variants

Figure 2: Keypad layout and connections

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A key is accepted as valid when two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start up time if it was not already running).

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

The dialling mode may be selected via the SELECT pin (pin 2) as detailed in Table 2. Four Loop-Disconnect options are available with different Interdigit pauses and Break/Make ratios, and one DTMF mode. If the DTMF mode is selected then dialling will remain fixed in the DTMF mode. However, if one of the LD modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing either the *, */# or TONE key (depending on mask variant - see Fig. 2 and page 1-28), provided that dialling is not in progress. If any of these keys are pressed during LD dialling, they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to lhe on-hook state.

SELECT pin to	Dialling mode	IDP (ms)	B/M ratio
V_{SS}	LD	800	2:1
COL 1	LD	500	2:1
COL 2	LD	500	3:2
COL 3	LD	800	3:2
V_{DD}	DTMF	-	-

Table 2: Dialling mode selection

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 32 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. The last number redial store has several features designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the LNR key. In this case, the remainder of the number will be dialled when the LNR key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR -store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and is switched by the user (via the */# or TONE key) to DTMF mode, only the digits dialled in LD mode will be retained. Providing that the number of digits dialled in LD mode does not exceed 32, they will be retained regardless of the number of DTMF digits entered subsequently.

DTMF Calls

A mask option is available (see page 1-28) to allow protection of PIN (Personal Identitication Number) codes as follows: It a call contains the digits * or #, only those digits dialled prior to the first press of either * or # will be retained in the LNR store.

Store Operation (SAVE)

The SAVE store is available as a mask option (see page 1-28) in place of the LNR store and is 32 digits long. If the user attempts to save a number of more than 32 digits, the store is inhibited. The contents of the store are maintained until overwritten.

The SAVE key may be pressed at any time whilst off-hook. This action causes digits dialled since going off-hook to be retained and the previous contents of the store to be overwritten. Further digits may be dialled after depression of the SAVE key, but they will not be retained.

The number in the 'SAVE' store can be redialled by pressing the LNR key once, whilst in speech mode. However, if an LD to DTMF mode change was effected when the number was originally dialled, a marker(') in the 'SAVE' store will cause the redialling to pause at this point and the speech circuit will be reactivated. If the LNR key is then pressed again, the remaining digits in the store will be redialled in DTMF.

The SAVE store offers the same 'Moving Cursor Facility' as the LNR store.

(1) This marker requires one store location.

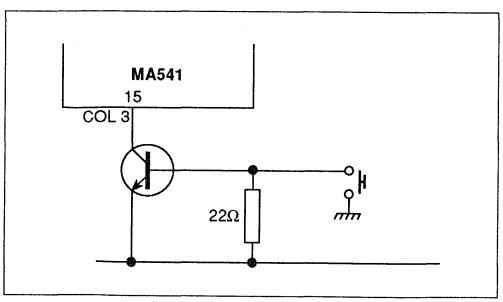


Figure 3: Earth loop recall

Timed Break & Earth Loop Recall (Flash)

The MA541 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the dialling mode selected via the SELECT pin will be restored. Also. only the digits dialled after the ELR/TBR operation will be retained in the LNR store [2].

A TBR (Flash) of 100ms [3] is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin. If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fig. 3, or by use of a double contact switch.

(2) A version where only the digits dialled before ELR/TBR are retained in the LNR store is available as a mask option (see page 1-28).

(3) Other TBR (Flash) periods are available as mask options (see page 1-28).

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the 'single pin' type. Internally, the OSC IN pin is connected to Vss and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 16 & 17) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

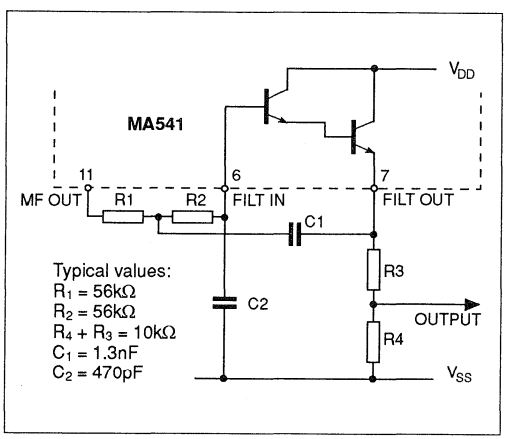


Figure 4: DTMF tone filtering

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission. The IMP output remains low during tone transmission. The MF OUT output rises to its DC level of 0.9 V_{DD} at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to llne is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and theh sent to line at the maximum rate. Dialling from the LNR store occurs at the maximum rate.

If a key is held down for longer than 100ms, the tone output will continue until the key is released.

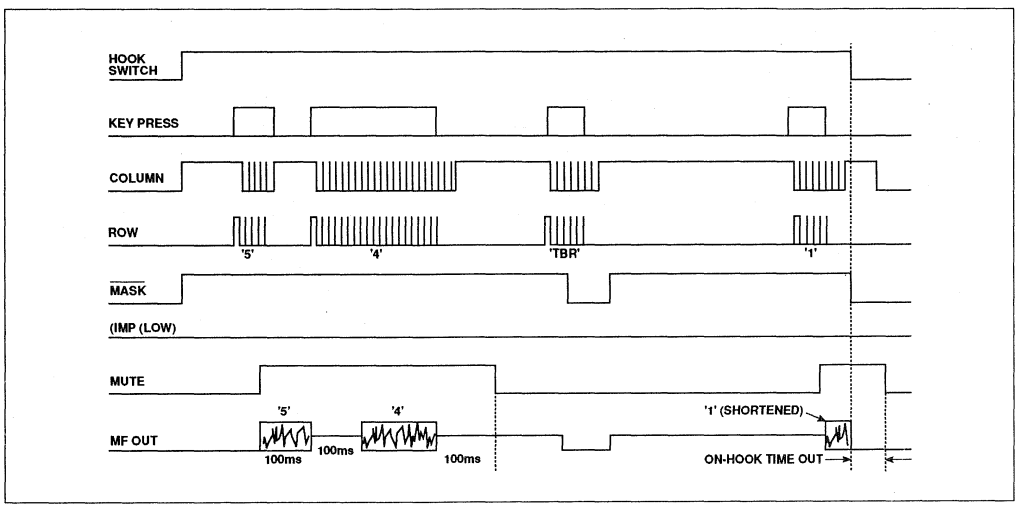


Figure 5: DTMF timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	-0.07	-0.10	+0.19	-0.15	-0.17	-0.20	-0.22	-0.31

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 3: Tone frequencies

LOOP-DISCONNECT DIALLING

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic '0' during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling. LD dialling is signalled on the IMP output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

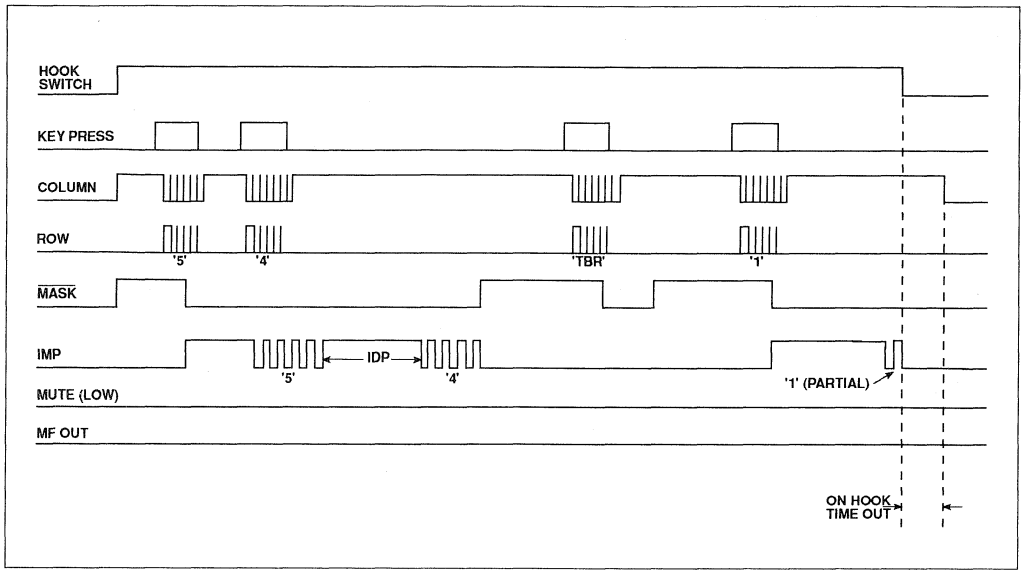


Figure 6: LD mode timing diagram

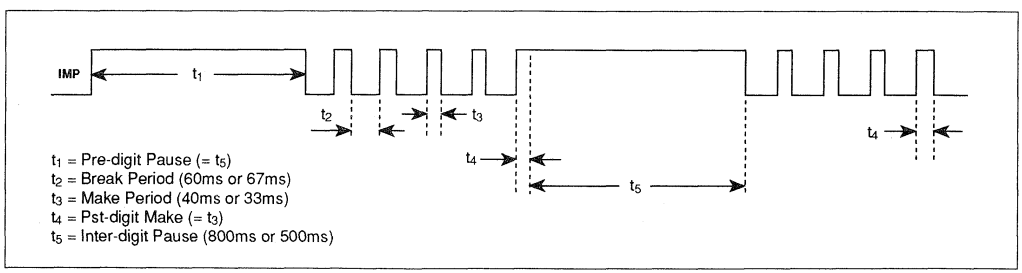


Figure 7: Timing data

MASK OPTIONS

The MA541 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufactute. These options allow the telephone manufacturer to cater for ditferent markel requirements throughout the world without changing the telephone circuit. The options, listed below, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

1. TBR (Flash) Period
a. 100 ms
b. 200 ms
c. 300 ms
d. 400 ms
e. 500 ms
f. 600 ms

2. LD to DTMF Keypad Switching
a. *and ,# keys
b. TONE key

3. Retention of Post - */# Digits in LNR Store (DTMF mode)
a. All digits retained
b. Digits before * or # retained

4. LNR or SAVE store
a. LNR
b. SAVE

5. Recall (Flash) / LNR Protocol
a. Digits dialled after recall retained
b. Digits dialled before recall retained

6. Pin 3
a. $\overline{MASK}$
b. MASK

7. Pin 1
a. IMP
b $\overline{IMP}$
c. (IMP + $\overline{MASK}$]
d. [$\overline{IMP}$ + MASK]

8. Pin 12
a. MUTE
b. $\overline{MUTE}$

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Supply current:	On-hook		<1	5.0	µA	V_{DD} = 2.0V
	Off-hook		1.5		µA	MF OUT low
	MFtone sending			1.0	mA	
	LD impulsing			200	µA	
Output high voltage ($\overline{MASK}$ and MUTE outputs)		2.2			V	I = -1mA
Output low voltage ($\overline{MASK}$ and MUTE outputs)				0.3	V	I = +1mA
MF OUT DC level during tone sending			$0.9V_{DD}$		V	
MF OUT output resistance			3		kΩ	
'Key Pressed' resistance				2	kΩ	2.5V < V_{DD} < 5.7V
'Key Not Pressed' resistance		500			kΩ	2.5V < V_{DD} < 5.7V
Darlington pair current gain (see fig 4)		600	50,000			I_E = 100µA, V_{CE} = 2V

NOTE 1. Specially screened versions with lower on-hook supply current are available.

AC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Tone output:	low group	57	64		mV rms	No load.
	high group		81	91	mV rms	No load.
High-to-Low group amplitude ratio (pre emphasis)		1.5	2	2.5	dB	See note 2
Total harmonic distortion:	0-4 kHz		1.5		%	
	0-10 kHz		2.5		%	
	0-50 kHz		5.0		%	
	0-200 kHz		6.5	10	%	
Oscillator start-up time			<0.1	1	ms	

NOTE 2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition		Min.	Typ.	Max.	Units	Notes
Supply Voltage:	On-hook	1.8		5.7	V	
	Off-hook	2.4		5.7	V	
Hookswitch input:	On-hook			$0.2V_{DD}$	V	
	Off-hook	$0.8V_{DD}$			V	
Oscillating frequency			560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}-V_{SS}	- 0.3 to + 6.5V
Voltage on any pin (except HSW)	V_{SS} - 0.3V to V_{DD} + 0.3V
Voltage on HSW pin (See note 1)	V_{SS} - 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	±1 mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	-5 to 0mA
Storage temperature	-55°C to + 125°C
Operating temperature range	-10°C to + 55°C

NOTES

1. A diode is internally connected between this pin and VDD. Provided current is externally limited to 300µA max. no damage will occur.

2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and tunctional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

APPLICATION CIRCUITS

The circuit in Fig. 8 uses a constant current supply to take current from the telephone line which is used to power the MA541. The 2.5V reference diode produces a stabilised supply voltage which determines the MF tone level of the MA541 .

In Fig. 9, a stabilising voltage from the speech circuit is used to supply the MA541 during MF dialling to give accurate tone levels.

The MA541 is powered via the 150kΩ resistor during TBR operations and LD dialling breaks, and via TR1 during dialling makes. This configuration minimises the component count at the expense of allowing a leakage current of about 450µA during dialling breaks. The 47µF reservoir capacitor maintains and smooths the supply to the chip.

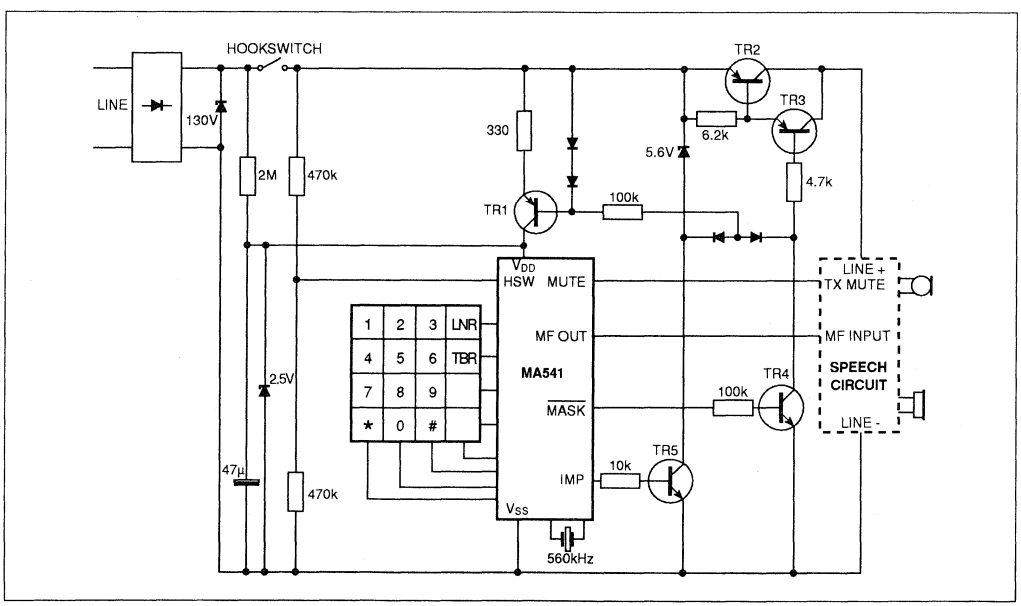


Figure 8: Application circuit 1

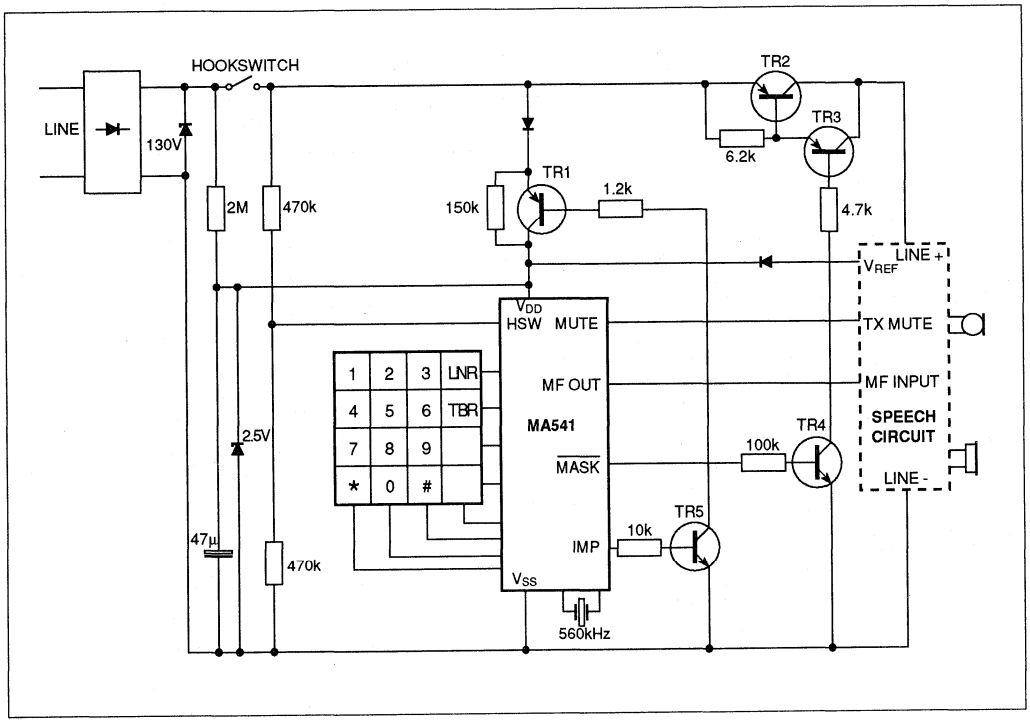


Figure 9: Application circuit 2

NOTE: Except for keypad functions and layout, the application circuits shown in Figures 8 and 9 apply equally to the MA545, MA547, MA585, MA587 and MA589 dialler families.

MA544 FAMILY

10-MEMORY LD/DTMF SWITCHABLE DIALLER CHIPS

The MA544 family is a range of keypad switchable LD/DTMF dialler devices with Last Number Redial facility and ten 24-digit memories.

Three operating modes are available: LD mode, with the ability to temporarily switch to DTMF mode from the keypad during a call, LD only mode and DTMF mode. The former mode enables users to access services such as home banking. Mixed LD and DTMF numbers can also be stored in memory.

The MA544 family is pin compatible with the GPS switchable dialler families MA545, MA547, MA541, MA548, MA585, MA587, MA588 and MA589 – providing a complete range of telephone features with a single PCB design.

Metal mask and pin selectable options are available to service the specific technical requirements of particular countries and for customers' preferred features and circuit configurations.

FEATURES

- Selectable Loop-Disconnect or DTMF Dialling Modes
- Keypad Switchable LD to DTMF
- 24 digit Last Number Redial
- 10 x 24 Digit Memories
- Selectable Break/Make Ratios 2:1 and 3:2
- Uses Inexpensive 560 kHz Ceramic Resonator
- Batteryless Operation: Low Power CMOS
- Standard DTMF Timings: 100ms ON, 100ms OFF (minimum), Other Options Available
- PIN Confidentiality Feature.
- Timed Break Recall (Flash) and Earth Recall.
- Timed Pause Release.

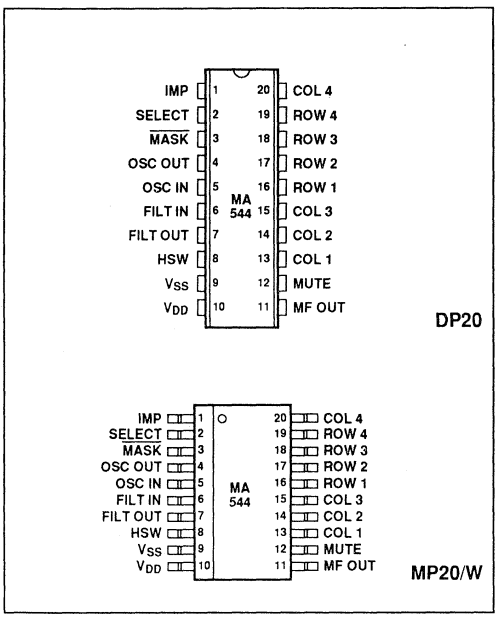


Fig. 1 Pin connections - top view (not to scale)

PIN FUNCTIONS

Pin Number	Pin Name	Function
1	IMP	'Loop disconnect' dialling output
2	SELECT	LD/DTMF selection, IDP and B/M ratio programming
3	$\overline{\text{MASK}}$	Output to disable speech circuit during pulse dialling and recall (see note 1)
4, 5	OSC OUT, OSC IN	Connections for 560 kHz ceramic resonator
6, 7	FILT IN, FILT OUT	Unity gain amplifier input and output for DTMF tone filtering
8	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-hook'
9	V_{SS}	Negative supply
10	V_{DD}	Positive supply
11	MF OUT	Unfiltered DTMF output
12	MUTE	Output active during keying and tone transmission (see note 2)
13	COL1	
14	COL2	
15	COL3	
16	ROW1	
17	ROW2	
18	ROW3	Connections for 16 button single contact keypad
19	ROW4	
20	COL4	

Note 1. The $\overline{\text{MASK}}$ output may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook, during a TBR (Timed Break Recall) operation or for LD dialling.

Note 2. The MUTE output is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1

OPERATION

Power-On

When power is applied to the chip, a power-on reset circuit operates and ensures that the stores are cleared and all logic is reset. On power-up the dialling mode is set to LD until a key is pressed. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the the stores may be corrupted, it will always, under all conditions, clear the stores so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA544 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the on-hook state is not recognised for 200-300 ms. On a device with Spanish DTMF (see page 6), the on-hook recognition time becomes 147-220ms when tones are being transmitted. This is so that short line breaks, such as line reversals applied by the exchange, are ignored. In this case the $\overline{\text{MASK}}$ and IMP outputs will go low immediately the HSW input goes low in order to conserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted. This conserves supply current so that the memory contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to logic '1' and remains there until dialling starts, a TBR (Flash) occurs or the HSW input goes low (see Figs. 4 and 5). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7 ms intervals on each output in sequence. A key is accepted as valid when two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minumum bounce-free key closure period which is necessary to guarantee detection is 14 ms (plus the oscillator start up time if it was not already running).

Keypad layout and connections

	COL1	COL2	COL3	COL4
ROW1	1	2	3	TBR
ROW2	4	5	6	REDIAL
ROW3	7	8	9	STORE
ROW4	*	0	#	PAUSE /CONT

Table 2

The keys * and # are used to change from LD to DTMF dialling and are available as digits when in DTMF mode.

TBR: Timed Break Recall (Flash).
REDIAL: Last Number and Memory Redial.
STORE: Memory Programming.
PAUSE/CONT: Insert pause in memory/continue dialling.

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

SELECT pin to:	Dialling Mode	IDP (ms)	B/M Ratio
V_{SS}	LD + DTMF	800	2:1
COL1	LD + DTMF	500	2:1
COL2	LD + DTMF	500	3:2
COL3	LD + DTMF	800	3:2
COL4	LD ONLY	800	2:1
V_{DD}	DTMF	-	-

Table 3

The dialling mode may be selected via the SELECT pin (pin 2) as detailed in Table 3. Four 'Loop-Disconnect + DTMF' options with different Inter-digit pauses and Make/Break ratios, one 'Loop-Disconnect only' and one DTMF mode are available.

If the 'LD only' mode or the DTMF mode is selected, then dialling will remain fixed in LD mode or DTMF mode respectively. However, if one of the 'LD + DTMF' modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing the */# key provided that dialling is not in progress. If either of these keys are pressed during LD dialling they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

Keying PAUSE while dialling or changing to DTMF mode will cause a delay of 3.5 seconds before the next digit is output.

Last Number Redial (LNR)

The function of the on-chip LNR store is to automatically retain a manually dialled number for redialling later. The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number.

To redial a number in the LNR store, the REDIAL key must be pressed twice.

The last number redial store has several features designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the REDIAL key. In this case, the remainder of the number will be dialled when the REDIAL key is pressed twice.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed mode calls

In the case of a call which starts in LD mode and is switched by the user (via the */# key) to DTMF mode, only the digits dialled in LD mode will be retained. Providing that the number of digits dialled in LD mode does not exceed 24, they will be retained regardless of the number of DTMF digits entered subsequently. This feature is provided to ensure security of PIN (Personal Identification Number) codes.

DTMF calls

If a call contains the characters * or #, only those digits dialled prior to the first press of either * or # will be retained in the LNR store. The exception to this is when either * or # is the first character dialled in a call, in which case all digits dialled (including further * or # characters) will be retained. This feature also ensures security for PIN codes whilst allowing exchange facility codes (for example) to be retained.

Memory Dialling

The MA544 provides 10 memories, each of which has a capacity of 24 digits. The memories can store pauses and digits to be dialled in LD, DTMF or mixed modes.

Programming memories

The MA544 must be 'off-hook' and idle:

1. Press the STORE key.
2. Press the number (0-9) indicating the memory to be programmed.
3. Enter digits to be stored (no digits will be dialled whilst programming.
4. To finish programming the memory either press the STORE key again or go 'on-hook'.
5. Repeat to programme other memories.

If more than 24 digits are entered while programming a memory, then the memory will be cleared until reprogrammed. If any 'non-valid' keys are pressed during programming (e.g. LNR, TBR) they will be ignored.

Mixed Mode Numbers and Pauses in Memory

Mixed mode (i.e. LD + DTMF) numbers are easily programmed into memory. The SELECT pin must be set to one of the 'LD + DTMF' modes (as it would be when dialling a mixed mode number), then the store is programmed using the same procedure as above. The first press of */# will be stored as a 'change to DTMF' and this will cause all subsequent digits to be sent in DTMF when redialling from memory.

Similarly, pauses can be stored in memory by pressing the PAUSE key in the appropriate position when programming.

When dialling from memory both pauses and LD to DTMF changeovers will cause dialling to halt for 3.5 seconds. The exception to this rule is when a changeover is stored in the first memory location: In this case, DTMF dialling will occur immediately when memory dialling is invoked - this allows DTMF codes to be easily stored and sent even in a telephone where the normal dialling mode is LD.

It should be noted that a pause or an LD to DTMF changeover each require one memory location.

Dialling from Memories

The MA544 must be 'off-hook' and idle:

1. Press the REDIAL key once
2. Press the appropriate memory key (0-9). Dialling will now start.
3. If dialling halts due to a pause or an LD to DTMF changeover in the memory, further dialling will be resumed after 3.5 seconds.

All keypad positions are disabled whilst memory dialling is in progress.

Timed Break and Earth Loop Recall (Flash)

The MA544 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the dialling mode selected via the SELECT pin will be restored. Also, only the digits dialled before the ELR/TBR operation will be retained in the LNR store.

A TBR (Flash) of 100 ms [1] is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the COLUMN 3 pin. If this pin is connected to ground for a minimum of 20 ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown in Fig. 2, or by use of a double contact switch.

Grounding COLUMN 3 will not directly affect the chip outputs. However, in order to prevent misoperation, the HSW timeout will be disabled during ELR. This is so that the MA544 cannot go into the on-hook state if the HSW input goes low as a result of ELR signalling (i.e whilst the telephone is, in reality, still off-hook). The $\overline{\text{MASK}}$ and IMP outputs will respond as normal to the status of the HSW input.

[1] Other TBR (Flash) periods are available as mask options (see page 6).

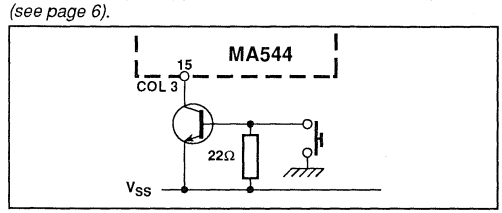


Fig. 2 Earth loop recall

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 6 & 7) for use in a low pass active filter.

Fig. 3 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5 dB.

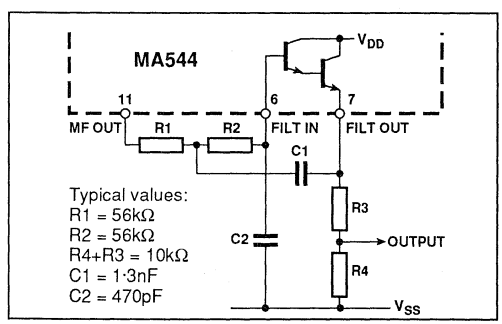


Fig. 3 DTMF tone filtering

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the 'single pin' type. Internally, the OSC IN pin is connected to V_{SS} and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

DTMF Dialling

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission. The IMP output remains low in DTMF mode. The MF OUT output rises to its DC level of 0.9 V_{DD} at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100 ms on, followed by 100 ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate. Dialling from the LNR store and memories occurs at the maximum rate.

If a key is held down for longer than 100 ms, the tone output will continue until the key is released.

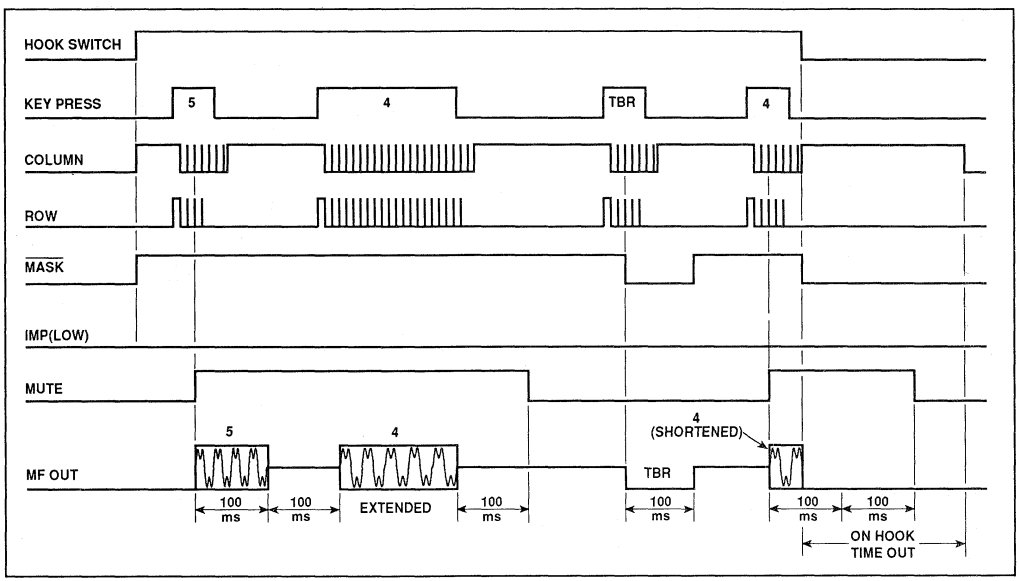


Fig. 4 DTMF mode timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477
Deviation from nominal (%)	-0.07	-0.10	+0.19	-0.15	-0.17	-0.20	-0.22

There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560 kHz.

Table 4 Tone frequencies

Loop-Disconnect Dialling

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic '0' during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling.

LD dialling is signalled on the IMP output: a break is signalled by a logic '0'; make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

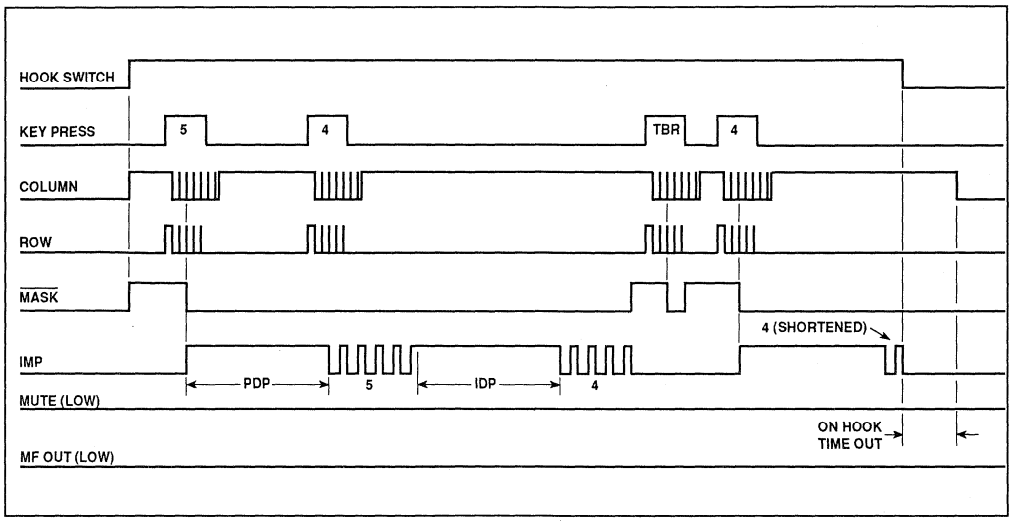
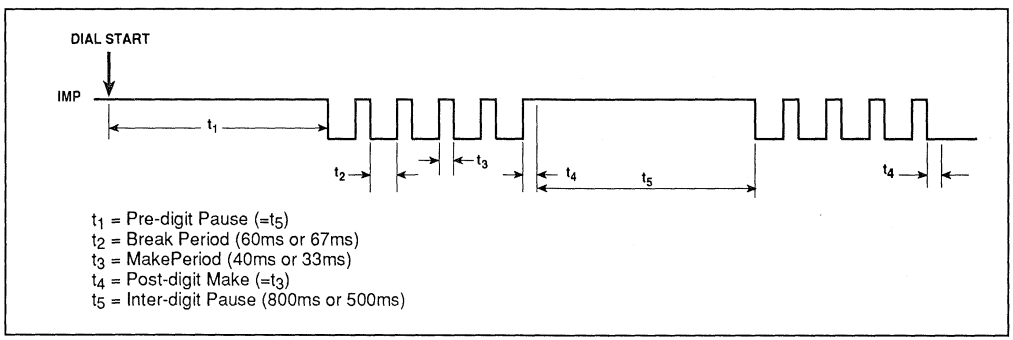


Fig. 5 LD mode timing diagram



t_1 = Pre-digit Pause (=t_5)
t_2 = Break Period (60ms or 67ms)
t_3 = MakePeriod (40ms or 33ms)
t_4 = Post-digit Make (=t_3)
t_5 = Inter-digit Pause (800ms or 500ms)

Fig. 6 Timing data

MASK OPTIONS

The MA544 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufacture. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit.

The options, listed below, are possible in any combination. Standard options are listed first in italics at 'a'. Other options may be produced by arrangement.

1. TBR (Flash) Period:
a. 100 ms
b. 200 ms
c. 300 ms
d. 400 ms
e. 500 ms
f. 600 ms

2. LD to DTMF Keypad Switching:
*a. * and # keys*
b. * key
c. No keypad switching

3. Retention of Post-*/#digits in LNR store (DTMF mode):
*a. Digits before * or # retained (except when * or # is first digit).*
b. Digits before * or # retained.
c. All digits retained.

4. LD dialling options:
a. Standard (n = n pulses, where 0 = 10)
b. Swedish (n = n + 1 pulses)
c. Norwegian (n = (11-n) pulses)
d. New Zealand (n = (10-n) pulses)

5. Recall (Flash)/LNR Protocol:
a. Digits after recall retained in LNR store
b. Digits before recall retained in LNR store
c. Recall inhibits LNR
d. For Danish PABX requirements

6. DTMF Minimum Timings:
a. 100 ms on, 100 ms off (UK PTT preferred)
b. 73.3 ms on, 73.3 ms off
c. 73.3 ms on, 146.7 ms off (Spanish PTT preferred)
d. 80 ms on, 80 ms off (German PTT preferred)

7. Pin 4:
a. $\overline{MASK}$
b. MASK

8. Pin 2:
a. IMP
b. $\overline{IMP}$
c. [IMP+$\overline{MASK}$]
d. $\overline{[IMP+\overline{MASK}]}$

9. Pin 15:
a. MUTE
b. $\overline{MUTE}$
c. $\overline{MUTE}$(Open-drain)

10. Timed Pause Release
a. 3.5 sec.
b. 0.5 to 7.0 sec in 0.5 steps

11. TBR Availability
a. LD and DTMF mode
b. DTMF mode only

ABSOLUTE MAXIMUM RATINGS

Parameter	Min.	Typ.	Max.	Units	Notes
Supply voltage V_{DD}-V_{SS}	-0.3	-	6.5	V	-
Voltage on any pin (except HSW)	V_{SS}-0.3	-	V_{DD}+0.3	V	-
Voltage on pin HSW	V_{SS}-0.3	-	-	V	See Note 1
Current at any pin (except HSW. FILTOUT and FILTIN)	-1	-	1	mA	
Current at pin FILTOUT	0	-	0.1	mA	-
Current at pin FILTIN	-5	-	0	mA	-
Operating temperature	-25	-	70	°C	-
Storage temperature	-55	-	125	°C	-

Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress ratingonly and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not Implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note 1. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300µA max. no damage will occur.
Note 2. These temperature ranges do not apply to all package types. Many package types are available and these may have limited temperature ranges. Further information is available on request.

Table 5

DC OPERATING CONDITIONS AND CHARACTERISTICS (Note 4)

Condition		Min.	Typ.	Max.	Units	Notes
Supply voltage:	On-hook	1.8	-	5.7	V	For memory retention
	Off-hook	2.4		5.7	V	
Hookswitch input:	On-hook	-	-	0.2 V_{DD}	-	-
	Off-hook	0.8 V_{DD}		-		

Characteristic		Min.	Typ.	Max.	Units	Notes
Supply current:	On-hook	-	0.1	5	µA	At V_{DD} = 2.0 V
	Off-hook		1.5		µA	True only if MF OUT is low
	MF tone sending			1.0	mA	-
	LD impulsing			200	µA	-
Output high voltage ($\overline{MASK}$ andIMP outputs)		2.2	-		V	I = −1 mA
Output off leakage (MUTE)		-	< 0.1	1	µA	$V_{MUTE} \leq V_{DD}$. Note 5.
Output low voltage ($\overline{MASK}$, MUTE and IMP outputs)		-	-	0.3	V	I = +1 mA
MF OUT DC level during tone sending		-	0.9 V_{DD}	-	V	-
MF OUT output resistance		-	3	5	kΩ	-
'Key Pressed' resistance		-	-	2	kΩ	2.5 V < V_{DD}< 5.7 V
'Key Not Pressed' resistance		500	-	-	kΩ	2.5 V < V_{DD}< 5.7 V
Darlington pair current gain		600	50,000	-	-	I_e = 100µA, V_{ce} = 2 V

Note 4. V_{DD} = 2.5 V at 25°C unless otherwise specified.
Note 5. A diode is internally connected between this pin and V_{DD}. The MUTE output may he held at a voltage above V_{DD} provided that current is externally limited to 300 µA max.

Table 6

AC OPERATING CONDITIONS AND CHARACTERISTICS

Condition	Min.	Typ.	Max.	Units	Notes
Oscillating Frequency	-	560	-	kHz	-

Characteristic		Min.	Typ.	Max.	Units	Notes
Tone Output:	Low Group	57	64	-	mV r.m.s.	No load. V_{DD} = 2.5V
	High Group		81	91	mV r.m.s.	No load. V_{DD} = 2.5V
High-to-low Group Amplitude ratio (pre-emphasis)		1.5	2	2.5	dB	See Note 6
Total Harmonic Distortion:	0-4 kHz	-	1.5	-	%	-
	0-10 kHz	-	2.5	-	%	-
	0-50 kHz	-	5.0	-	%	-
	0-200 kHz	-	6.5	10	%	-
Oscilllator Start-up Time		-	< 0.1	1	ms	-

Note 6. Typical value varies slightly dependent upon particular tone pair.

Table 7

MA545 FAMILY

LD/DTMF SWITCHABLE DIALLERS WITH 10 MEMORIES

The MA545 family are keypad switchable LD/DTMF dialler devices with a last number redial facility and ten 24digit memories.

Two operating modes are available: LD mode, with the ability to temporarily switch to DTMF mode from the keypad during a call, and DTMF only mode. The former mode enables subscribers to access such services as home banking. Mixed LD and DTMF numbers can also be stored in memory.

The MA545 devices are pin compatible with the GPS switchable dialler families MA526, MA527, MA541, MA547. MA585, MA587 and MA589 - providing a complete range of telephone features within a single PCB and circuit design.

Metal mask and pin selectable options are available to service specific requirements of particular countries and customers.

FEATURES

- Selectable Loop-Disconnect or DTMF Modes
- Keypad Switchable LD to DTMF
- 24 Digit Last Number Redial
- 10 x 24-Digit Memories
- Selectable Make/Break Ratios 2:1 and 3:2
- Uses Inexpensive 560kHz Ceramic Resonator
- Battery-less operation - Low Power CMOS
- Mask Programmable Options to suit Application
- Timed Break Recall (Flash) and Earth Recall

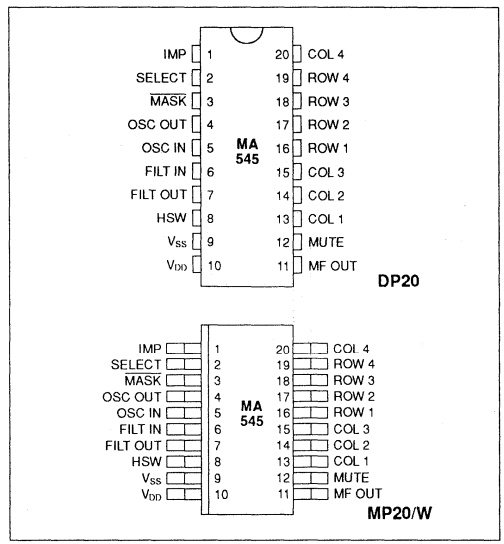


Figure 1: Pin connections - top view (not to scale)

PIN FUNCTIONS

Pin number	Pin name	Function
1	IMP	'Loop disconnect' dialling output
2	SELECT	LD/DTMF selection, IDP and B/M radio programming
3	MASK	Output to disable speech circuit during pulse dialling and recall (see note 1)
4	OSC OUT	Connections for 560kHz ceramic resonator
5	OSC IN	
6	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
7	FILT OUT	
8	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-hook'
9	V_{SS}	Negative supply
10	V_{DD}	Positive supply
11	MF OUT	Unfiltered DTMF output
12	MUTE	Output active during keying and tone transmission (see note 2)
13	COL1	Connections for 16 button single contact keypad
14	COL2	
15	COL3	
16	ROW1	
17	ROW2	
18	ROW3	
19	ROW4	
20	COL4	

1. $\overline{\text{MASK}}$ may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.
2. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1: Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA545 of whether the telephone is on or off hook. Logic 0 is recognised as on-hook, Logic 1 is recognised as off-hook. When the HSW input rises from 0 to 1 the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from 1 to 0 the onhook state is not recognised for 200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied by the exchange, are ignored. In this case the IMP and $\overline{\text{MASK}}$ outputs will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted.This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic 1 level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

	COL 1	COL 2	COL 3	COL 4
ROW 1	1	2	3	TBR
ROW 2	4	5	6	REDIAL
ROW 3	7	8	9	STORE
ROW 4	*	0	#	PAUSE

TBR: Timed Break Recall (Flash)
REDIAL: Last Number and Memory Redial
STORE: Memory programming
PAUSE: Insert pause in memory
TONE: (1) Change dialling mode from LD to DTMF

(1) Only available as a mask option, replacing the PAUSE key. TONE can be used to insert pauses in memory but only during DTMF dialling.

Figure 2: Keypad layout and connections

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start-up time if it was not already running).

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

The dialling mode may be selected via the SELECT pin (pin 2) as detailed in Table 2. Four Loop-Disconnect options are available with different Interdigit pauses and Break/Make ratios, and one DTMF mode. If the DTMF mode is selected then dialling will remain fixed in the DTMF mode. However, if one of the LD modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing either the *, */# or TONE key (depending on the mask variant - see Fig. 2 and page 1-36), provided that dialling is not in progress. If any of these keys are pressed during LD dialling, they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

SELECT pin to	Dialling mode	IDP (ms)	B/M ratio
V_{SS}	LD	800	2:1
COL 1	LD	500	2:1
COL 2	LD	500	3:2
COL 3	LD	800	3:2
V_{DD}	DTMF	-	-

Table 2: Dialling mode selection

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. To redial a number in the LNR store, the REDIAL key must be pressed twice.

The last number redial store has several features designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the REDIAL key; the remainder of the number will be dialled when the REDIAL key is pressed.

•If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of

the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the firs! digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and is switched by the user (via the *, */#, or TONE key) to DTMF mode, only the digits dialled in LD mode will be retained. This feature is provided to ensure security of PIN (Personal Identificabon Number) codes. Provided that the number of digits dialled in LD mode does not exceed 24, they will be retained regardless of the number of DTMF digits entered subsequently.

Memory Dialling

The MA545 provides 10 memories, each of which has a capacity of 24 digits. The memories can store digits to be dialled in LD, DTMF or Mixed modes and also pauses.

Programmin51 Memories

The MA545 must be off-hook and idle:

1. Press the STORE key.
2. Press the number (0-9) of the memory to be programmed.
3. Enter digits to be stored (no digits will be dialled whilst programming)
4. To finish programming the memory eilher press the STORE key again or go on-hook .
5. Repeat to programme other memories.

If more than 24 digits are entered while programming a memory, then the memory will be cleared until reprogrammed. If any non-valid keys are pressed during programming (e.g. REDIAL,TBR) they will be ignored.

Mixed mode numbers and pauses In memory

Mixed mode (i.e LD + DTMF) numbers are easily programmed into memory. The SELECT pin should be set to one of the LD plus DTMF modes (as it would be when dialling a mixed mode number), then the number entered using the same procedure as if programming normally. The first press of *, */# or TONE (according to the mask variant) will be stored as a change to DTMF, and this will cause all subsequent digits to be sent in DTMF when redialling from memory.

Similarly, pauses can be stored in memory by pressing the PAUSE key in the appropriate position when programming.

When redialling from memory, both pauses and LD to DTMF changeovers will cause dialling to halt temporarily until the user presses either the REDIAL or PAUSE key. The exception to this rule is when an LD to DTMF changeover is stored in the first memory location: In this case DTMF dialling will occur immediately when memory dialling is invoked - this allows DTMF codes to be easily stored and sent even in a telephone where the normal dialling mode is LD.

It should be noted that a pause or an LD to DTMF changeover each require one memory location.

Dialling from memoriles

The MA545 must be off-hook and idle:

1. Press the REDIAL key once.
2. Press the number (0-9) of the memory to be dialled. Dialling will now start.
3. If dialling halts due to a pause or an LD to DTMF changeover in the memory, further dialling can be resumed by pressing the REDIAL or the PAUSE key. Alternatively, the Column 4 pin can be pulled low (for a minimum of 14 ms) in order to achieve the same result, thus allowing an external timer circuit to be used.

All keypad positions are disabled whilst memory dialling is in progress.

Timed Break & Earth Loop Recall (Flash)

The MA545 supports both TBR and ELR and offers a common operating protocol in both cases.

Afler a recall (Flash) operation, the dialling mode selected via the SELECT pin will be restored. Also, only the digits dialled afler the ELR/TBR operation will be retained in the LNR store [1].

A TBR (Flash) of 100ms [2] is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin. If this pin is connected to ground for a minimum of 20ms during an

ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fiy. 3, or by use of a double contact switch.

[1] Other options are available, including an option for Danish requirements (see page 1-36). In Denmark, TBR (or ELR) is used to obtain an outside line in PABX use. Under these conditions the LNR store contents will be retained and can be redialled after a TBR or ELR. Digits manually entered afler a TBR or ELR will become the new LNR store contents.

[2] Other TBR (Flash) periods are available as mask options (see page 1-36).

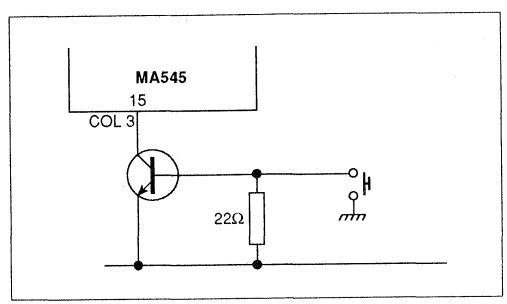


Figure 3: Earth loop recall

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing referlence for all chip functions. No other components are required or should be used.

The oscillator circuit is of the single pin type. Internally, the OSC IN pin is connected to V_{SS} and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

Tone Filtering

The spectral purity ot the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 6 & 7) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

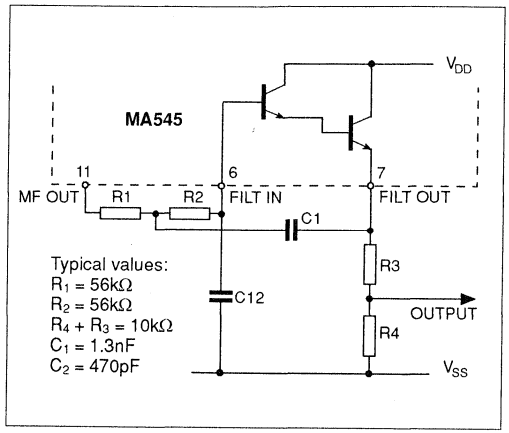


Figure 4: DTMF tone filtering

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic 1 and remains there for the duration of the tone transmission. The IMP output remains low duling tone transmission The MF OUT output rises to its DC level of 0.9 VDD at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate.

If a key as held down for longer than 100ms, the tone output will continue until the key is released.

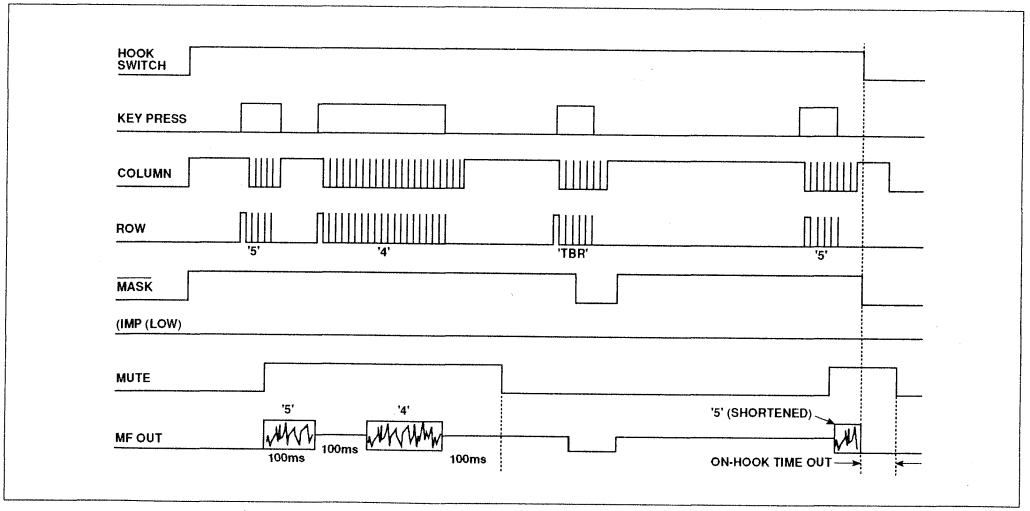


Figure 5: DTMF timing diagram

LOOP-DISCONNECT DIALLING

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic 0 during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling. LD dialling is signalled on the IMP output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	-0.07	-0.10	+0.19	-0.15	-0.17	-0.20	-0.22	-0.31

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 3: Tone frequencies

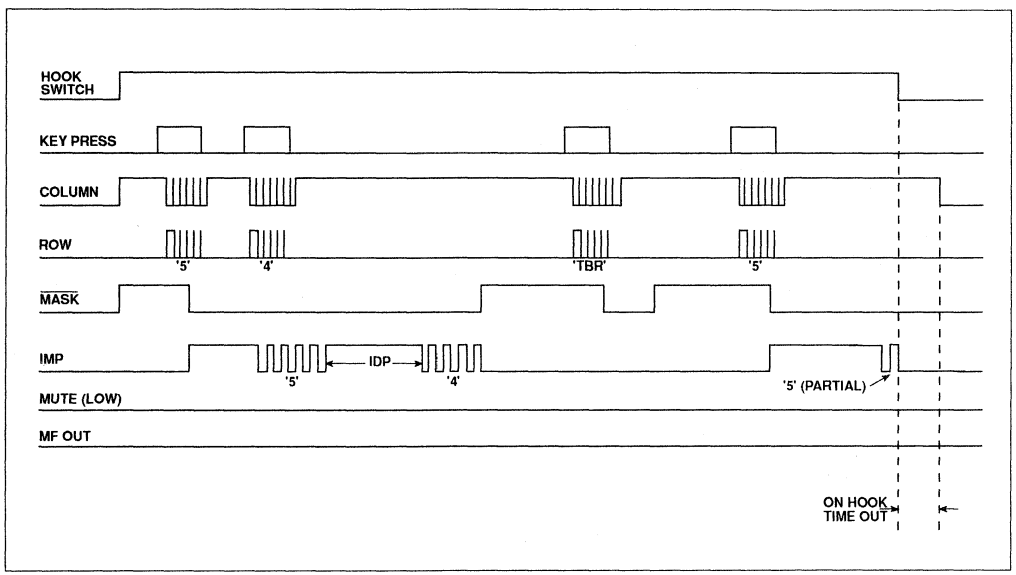


Figure 6: LD mode timing diagram

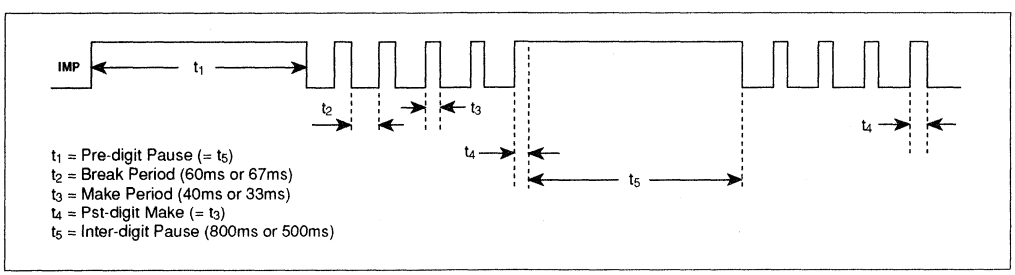


Figure 7: Timing data

MASK OPTIONS

The MA545 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufactute. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit. The options, listed below, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

1. TBR (Flash) Period
a. 100 ms
b. 200 ms
c. 300 ms
d. 400 ms
e. 500 ms
f. 600 ms

2. LD to DTMF Keypad Switching
a. *and ,# keys
b. TONE key
c, * key

3. Retention of Post - */# Digits in LNR Store (DTMF mode)
a. All digits retained
b. Digits before * or # retained
c. Digits before * and # retained (except when * or # is first digit

4. LD dialling options
a. Standard (n = N pulses, except 0 = 10 pulses)
b. Swedish (n = (n + 1) pulses)
c. Norwegian (n = (11 - n) pulses)
d. New Zealand (n = (10 - n) pulses)

5. Recall (Flash) / LNR Protocol
a. Digits dialled after Recall retained
b. Digits dialled before Recall retained
c. Recall inhibits LNR
d. For Danish PABX requirements

6. DTMF Minimum Timings
a. 100ms on, 100ms off
b. 73ms on, 73ms off
c. 73ms on, 147ms off

7. Keyboard Options (Key Position COL4, ROW4)
a. PAUSE key
b. TONE key (see option 2b)\c. LNR key (single press, replaces double press of REDIAL)

8. Pin 3
a. $\overline{MASK}$
b. MASK

9. Pin 1
a. IMP
b. $\overline{IMP}$
c. [IMP + $\overline{MASK}$]
d. [$\overline{IMP}$ + MASK]

10. Pin 12
a. MUTE
b. $\overline{MUTE}$

APPLICATION CIRCUITS

Refer to the MA541 data sheet, Figs. 8 and 9, on pages 1-29 and 1-30

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Supply current:	On-hook		<1	5.0	µA	V_{DD} = 2.0V
	Off-hook		1.5		µA	MF OUT low
	MFtone sending			1.0	mA	
Output high voltage ($\overline{MASK}$ and MUTE outputs)		2.2			V	I = -1mA
Output low voltage ($\overline{MASK}$ and MUTE outputs)				0.3	V	I = +1mA
MF OUT DC level during tone sending			$0.9V_{DD}$		V	
MF OUT output resistance			3		kΩ	
'Key Pressed' resistance				2	kΩ	2.5V < V_{DD} < 5.7V
'Key Not Pressed' resistance		500			kΩ	2.5V < V_{DD} < 5.7V
Darlington pair current gain (see fig 4)		600	50,000			I_E = 100µA, V_{CE} = 2V

NOTE 1. Specially tested versions with guaranteed lower on-hook supply current are available.

AC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Tone output:	low group	57	64		mV rms	No load.
	high group		81	91	mV rms	No load.
High-to-Low group amplitude ratio (pre emphasis)		1.5	2	2.5	dB	See note 2
Total harmonic distortion:	0-4 kHz		1.5		%	
	0-10 kHz		2.5		%	
	0-50 kHz		5.0		%	
	0-200 kHz		6.5	10	%	
Oscillator start-up time			<0.1	1	ms	

NOTE 2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition		Min.	Typ.	Max.	Units	Notes
Supply Voltage:	On-hook	2.0		5.7	V	For memory retention
	Off-hook	2.4		5.7	V	
Hookswitch input:	On-hook			$0.2V_{DD}$	V	
	Off-hook	$0.8V_{DD}$			V	
Oscillating frequency			560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}-V_{SS}	- 0.3 to + 6 5V
Voltage on any pin (except HSW)	V_{SS} - 0.3V to V_{DD} + 0 3V
Voltage on HSW pin (See note 1)	V_{SS} - 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	±1 mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	-5 to 0mA
Storage temperature	-55°C to + 125°C
Operating temperature range	-10°C to + 55°C

NOTES

1. A diode is internally connected between this pin and VDD. Provided current is externally limited to 300/1A max. no damage will occur.

2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

APPLICATION CIRCUITS

The circuit in Fig. 8 uses a constant current supply to take current from the telephone line which is used to power the MA541. The 2.5V reference diode produces a stabilised supply voltage which determines the MF tone level of the MA541 .

In Fig. 9, a stabilising voltage from the speech circuit is used to supply the MA541 during MF dialling to give accurate tone levels.

The MA541 is powered via the 150kΩ resistor during TBR operations and LD dialling breaks, and via TR1 during dialling makes. This configuration minimises the component count at the expense of allowing a leakage current of about 450μA during dialling breaks. The 47μF reservoir capacitor maintains and smooths the supply to the chip.

MA547 FAMILY

LD/DTMF SWITCHABLE DIALLERS WITH DEDICATED KEYS FOR 10 MEMORIES

The MA547 family are keypad switchable LDIDTMF dialler devices with a last number redial facility and ten 2 digit memories each with its own dedicated dialling key.

Three ope;ating modes are available: LD only mode, DTMF only mode and LD mode with the ability to switch temporarily to DTMF mode from the keypad during a call. This last mode enables subscribers to access such services as home banking. Mixed LD and DTMF numbers can also be stored in memory. The MA547 devices are pin compatible with the GPS switchable dialler families MA526, MA527, MA541, MA545. MA585, MA587 and MA589 providing a complete range of telephone features within a single PCB and circuit design. Metal mask and pin selectable options are available to service specific reauirements of particular countries and customers.

FEATURES

- Selectable Loop-Disconnect or DTMF Modes
- Keypad Switchable LD to DTMF
- 10X24-Digit Memories, each with Dedicated Key
- 24 Digit Last Number Redial
- Selectable Make/Break Ratios 2:1 and 3:2
- Uses Inexpensive 560kHz Ceramic Resonator
- Battery-less operation - Low Power CMOS
- Mask Programmable Options to suit Application
- Timed Break Recall (Flash) and Earth Recall

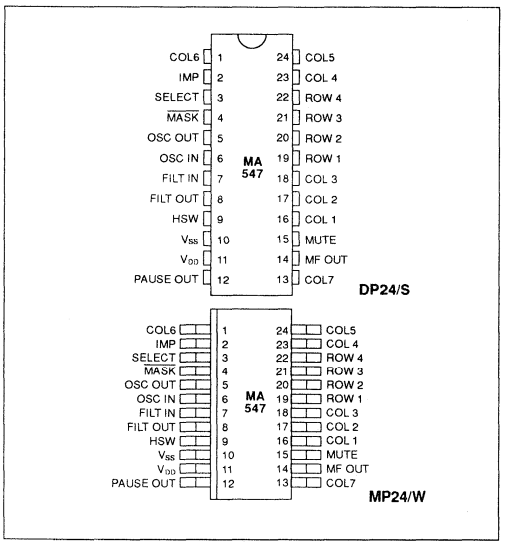


Figure 1: Pin connections - top view. DP24/S: 0.3in 'skinnydip' plastic DIL; MP24/W: wide-bodied Small Outline package

PIN FUNCTIONS

Pin number	Pin name	Function
2	IMP	'Loop disconnect' dialling output
3	SELECT	LD/DTMF selection, IDP and B/M radio programming
4	$\overline{\text{MASK}}$	Output to disable speech circuit during pulse dialling and recall (see note 1)
5	OSC OUT	Connections for 560kHz ceramic resonator
6	OSC IN	
7	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
8	FILT OUT	
9	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-hook'
10	V_{SS}	Negative supply
11	V_{DD}	Positive supply
12	PAUSE OUT	Active high output indicating a pause when dialling from memory
14	MF OUT	Unfiltered DTMF output
15	MUTE	Output active during keying and tone transmission (see note 2)
16	COL1	Connections for 28 key single contact keypad
17	COL2	
18	COL3	
23	COL4	
24	COL5	
1	COL6	
13	COL7	
19	ROW1	
20	ROW2	
21	ROW3	
22	ROW4	

1. $\overline{\text{MASK}}$ may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.
2. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1: Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA547 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the on-hook state is not recognised for 200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied bv the exchange, are ignored. In this case the IMP and $\overline{\text{MASK}}$ outputs will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted.This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic '1' level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start-up time if it was not already running).

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

The dialling mode may be selected via the SELECT pin (pin 3) as detailed in Table 2. Four 'LoopDisconnect + DTMF options and tour 'Loop-Disconnect only' options with different Interdigit pauses and Break/Make ratios are available and one DTMF mode If one of the 'LD only' modes or the DTMF mode is selected then dialling will remain fixed in LD mode or DTMF mode respectively .

	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7
ROW 1	1	2	3	TBR	S1	S2	S3
ROW 2	4	5	6	LNR	S4	S5	S6
ROW 3	7	8	9	STORE	S7	S8	S9
ROW 4	*	0	#	PAUSE/ CONT	MUTE	S0	

* or */# are used to change from LD to DTMF dialling and are available as digits when in DTMF mode

TBR: Timed Break Recall (Flash)
LNR: Last Number Redial
STORE: Memory programming
PAUSE/CONT: Insert pause in memory/continue dialling
MUTE: Activate MUTE output
S0-S9: Dedicated memory dialling keys
TONE: Change dialling mode from LD to DTMF

	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7
ROW 1	1	2	3	TBR	S1	S2	S3
ROW 2	4	5	6	LNR	S4	S5	S6
ROW 3	7	8	9	STORE	S7	S8	S9
ROW 4	*	0	#	TONE	MUTE	S0	PAUSE/ CONT

Figure 2: Keypad layout and connections

SELECT pin to	Dialling mode	IDP (ms)	B/M ratio
V_{SS}	LD + DTMF	800	2:1
COL 1	LD + DTMF	500	2:1
COL 2	LD + DTMF	500	3:2
COL 3	LD + DTMF	800	3:2
COL 4	LD only	800	2:1
COL 5	LD only	500	2:1
COL 6	LD only	500	3:2
COL 7	LD only	800	3:2
V_{DD}	DTMF	-	-

Table 2: Dialling mode selection

However, if one of the 'LD + DTMF' modes is selected, the chip will lie in LD mode initially in the off-hook condition but may be switched lo DTMF by pressing either the *, */# or TONE key (depending on the mask variant - see Fig. 2 and page 1-43), provided that dialling is not in progress. If any of these keys are pressed during LD dialling, they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. To redial a number in the LNR store, the LNR key must be pressed once.

The last number redial store has several leatures designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the LNR key; the remainder of the number will be dialled when the LNR key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and is switched by the user (via the *, */#, or TONE key) to DTMF mode, only the digits dialled in LD mode will be retained. This feature is provided to ensure security of PIN (Personal Identification Number) codes. Provided that the number of digits dialled in LD mode does not exceed 24, they will be retained regardless of the number of DTMF digits entered subsequently.

Memory Dialling

The MA547 provides 10 memories, each of which has a capacity of 24 digits and each of which has its own dedicated key. The memories can store digits to be dialled in LD, DTMF or mixed modes and also pauses.

Programming Memories

The MA547 must be 'off-hook' and idle:

1. Press the STORE key.
2. Press the key (S0-S9) of the memory to be programmed .
3. Enter digits to be stored (no digits will be dialled whilst programming)
4. To finish programming the memory either press the STORE key again or go 'on-hook'. 5. Repeat to programme other memories.

If more than 24 digits are entered while programming a memory, then the memory will be cleared until reprogrammed. If any non-valid keys are pressed during programming (e.g. LNR,TBR) they will be ignored.

Mixed mode numbers and pauses in memory

Mixed mode (i.e LD + DTMF) numbers are easily programmed into memory. The SELECT pin should be set to one ot the 'LD+DTMF' modes (as it would be when dialling a mixed mode number), then the number entered using the same procedure as if dialling normally. The first press of *, */# or TONE (according to the mask variant) will be stored as a 'change to DTMF', and this will cause all subsequent digits to be sent in DTMF when redialling from memory.

Similarly, pauses can be stored in memory by pressing the PAUSE key in the appropriate position when programming.

When redialling from memory, both pauses and LD to DTMF changeovers will cause dialling to halt temporarily until the user presses the PAUSE/CONT key. The exception to this rule is when an LD to DTMF changeover is stored in the first memory location: in this case, DTMF dialling will occur immediately when memory dialling is invoked - this allows DTMF codes to be easily stored and sent even in a telephone where the normal dialling mode is LD.

It should be noted that a pause or an LD to DTMF changeover each require one memory location.

Dialling from memories

The MA547 must be 'off-hook' and idle:

1. Press the appropriate dedicated memory key (S0-S9). Dialling will now start.
2. If dialling halts due to a pause or an LD to DTMF changeover in the memory, the PAUSE OUT pin will go high (logic '1'). Further dialling can be resumed either by pressing the PAUSE/CONT key or, alternatively, the Column 4 pin can be pulled low (for a minimum of 14 ms) to achieve the same result, thus allowing an external timer circuit to be used. The PAUSE/OUT output is reset when dialling resumes.

All keypad positions are disabled whilst memory dialling is in progress.

Timed Break & Earth Loop Recall (Flash)

The MA547 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the dialling mode selected via the SELECT pin will be restored. Also, only the digits dialled after the ELR/TBR operation will be retained in the LNR store [1].

A TBR (Flash) of 100ms [2] is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin. If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fig. 3, or by use of a double contact switch.

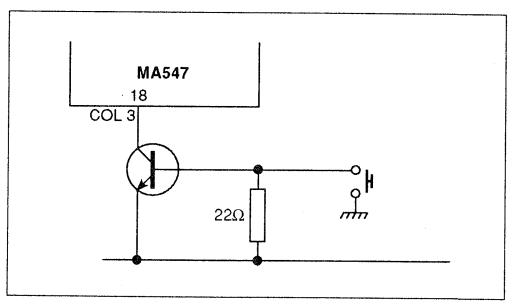


Figure 3: Earth loop recall

(1) Other options are available, including an option for Danish requirements (see page 1-43). In Denmarh, TBR (or ELR) is used to obtain an outside line in PABX use. Under these conditions the LNR store contents will be retained and can be redialled afler a TBR or ELR. Digits manually entered afler a TBR or ELR will become the new LNR store contents.

(2) Other TBR (Flash) periods are available as mask options (see page 1-43).

Oscillator Circuit

This requires an external 560kilz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the 'single pin' type. Internally, the OSC IN pin is connected to V_{SS} and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

Mute Facility

A MUTE facility is provided to allow the user to mute the transmit path (ie. the microphone) while still being able to hear the receive path.

A keypad position is provided for this facility, whenever, and for as long as, the MUTE key is pressed, the MUTE output will be active (logic '1') in order to disable the transmit path of the speech circuit. This is the same action as during DTMF transmission.

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 7 & 8) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented.

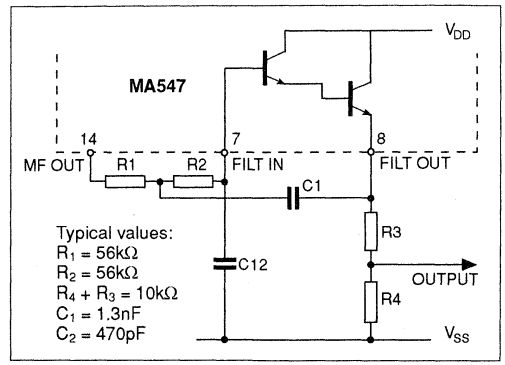


Figure 4: DTMF tone filtering

The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission .

The IMP output remains low during tone transmission. The MF OUT output rises to its DC level of 0.9 VDD at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and then sent lo line at the maximum rate. Dialling from the LNR store occurs at the maximum rate.

If a key is held down for longer than 100ms, the tone output will continue until the key is released.

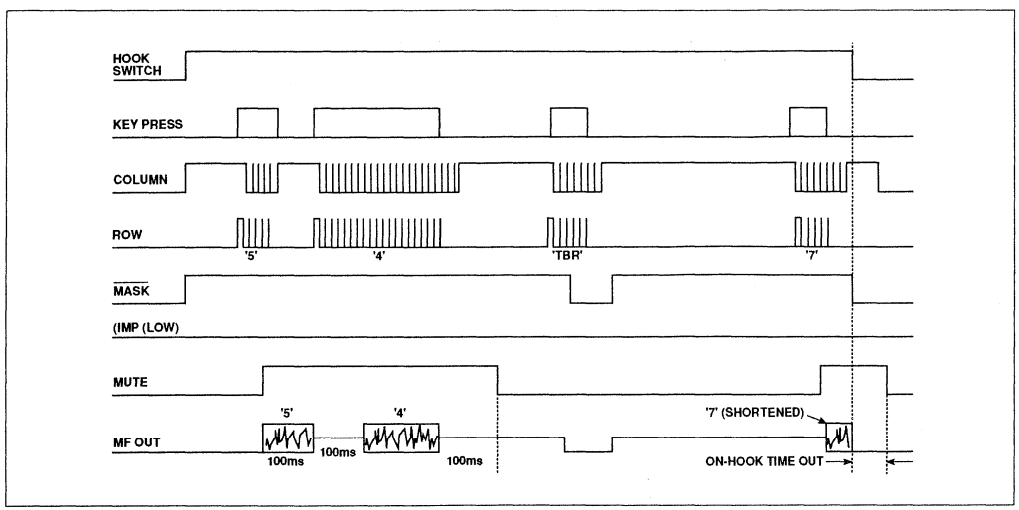


Figure 5: DTMF mode timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	-0.07	-0.10	+0.19	-0.15	-0.17	-0.20	-0.22	-0.31

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

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LOOP-DISCONNECT DIALLING

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic 0 during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

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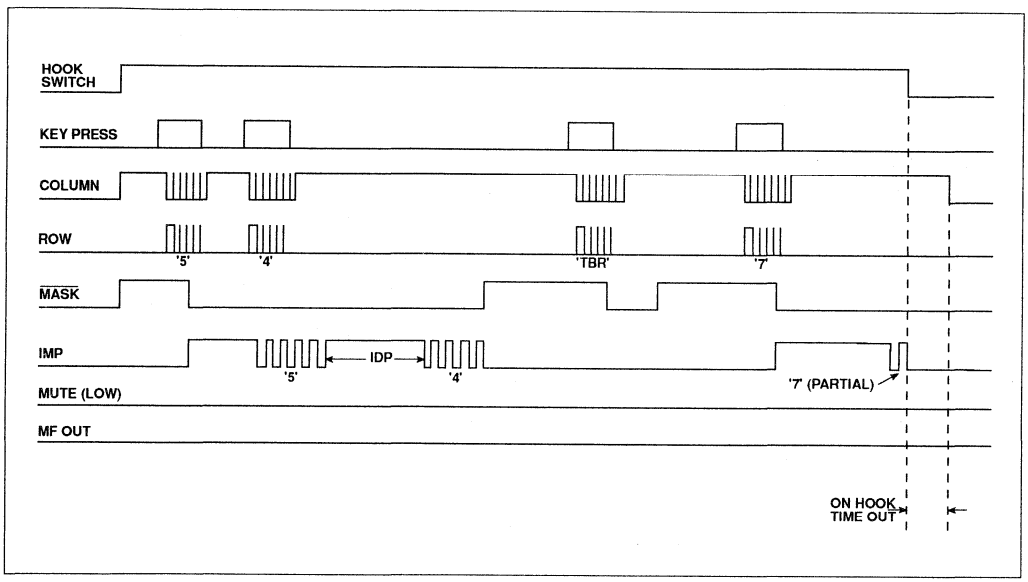

Figure 6: LD mode timing diagram

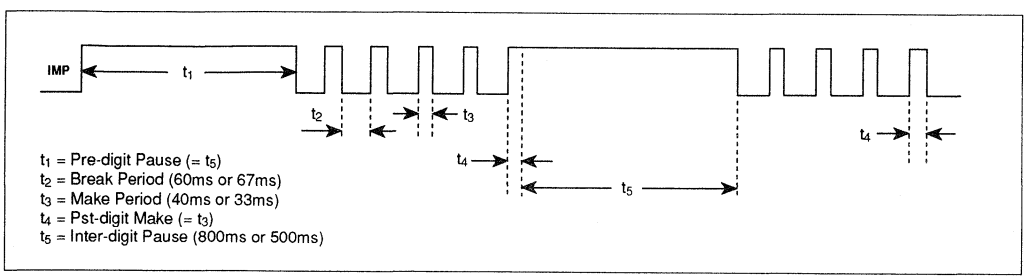

Figure 7: Timing data

MASK OPTIONS

The MA547 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufactute. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit. The options, listed below, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

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a. 100 ms
b. 200 ms
c. 300 ms
d. 400 ms
e. 500 ms
f. 600 ms

2. LD to DTMF Keypad Switching
a. *and ,# keys
b. TONE key
c, * key

3. Retention of Post - */# Digits in LNR Store (DTMF mode)
a. All digits retained
b. Digits before * or # retained
c. Digits before * and # retained (except when * or # is first digit

4. LD dialling options
a. Standard (n = N pulses, except 0 = 10 pulses)
b. Swedish (n = (n + 1) pulses)
c. Norwegian (n = (11 - n) pulses)
d. New Zealand (n = (10 - n) pulses)

5. Recall (Flash) / LNR Protocol
a. Digits dialled after Recall retained
b. Digits dialled before Recall retained
c. Recall inhibits LNR
d. For Danish PABX requirements

6. DTMF Minimum Timings
a. 100ms on, 100ms off
b. 73ms on, 73ms off
c. 73ms on, 147ms off

7. Pin 4
a. $\overline{MASK}$
b. MASK

8. Pin 2
a. IMP
b. $\overline{IMP}$
c. [IMP + $\overline{MASK}$]
d. [$\overline{IMP}$ + MASK]

9. Pin 15
a. $\overline{MUTE}$
b. $\overline{MUTE}$

APPLICATION CIRCUITS

Refer to the MA541 data sheet, Figs. 8 and 9, on pages 1-29 and 1-30

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Supply current:	On-hook		<1	5.0	µA	V_{DD} = 2.0V
	Off-hook		1.5		µA	MF OUT low
	MFtone sending			1.0	mA	
	LD impulsing				µA	
Output high voltage ($\overline{MASK}$ and MUTE outputs)		2.2			V	I = -1mA
Output low voltage ($\overline{MASK}$ and MUTE outputs)				0.3	V	I = +1mA
MF OUT DC level during tone sending			$0.9V_{DD}$		V	
MF OUT output resistance			3		kΩ	
'Key Pressed' resistance				2	kΩ	2.5V < V_{DD} < 5.7V
'Key Not Pressed' resistance		500			kΩ	2.5V < V_{DD} < 5.7V
Darlington pair current gain (see fig 4)		600	50,000			I_E = 100µA, V_{CE} = 2V

NOTE 1. Specially tested versions with guaranteed lower on-hook supply current are available.

AC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Tone output:	low group	57	64		mV rms	No load.
	high group		81	91	mV rms	No load.
High-to-Low group amplitude ratio (pre emphasis)		1.5	2	2.5	dB	See note 2
Total harmonic distortion:	0-4 kHz		1.5		%	
	0-10 kHz		2.5		%	
	0-50 kHz		5.0		%	
	0-200 kHz		6.5	10	%	
Oscillator start-up time			<0.1	1	ms	

NOTE 2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition		Min.	Typ.	Max.	Units	Notes
Supply Voltage:	On-hook	2.0		5.7	V	For memory retention
	Off-hook	2.4		5.7	V	
Hookswitch input:	On-hook			$0.2V_{DD}$	V	
	Off-hook	$0.8V_{DD}$			V	
Oscillating frequency			560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}-V_{SS} - 0.3 to + 6 5V
Voltage on any pin (except HSW) V_{SS} - 0.3V to V_{DD} + 0 3V
Voltage on HSW pin (See note 1) V_{SS} - 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN) ±1 mA
Current at FILTOUT pin 0 to 0.1mA
Current at FILTIN pin -5 to 0mA
Storage temperature -55°C to + 125°C
Operating temperature range -10°C to + 55°C

NOTES

1. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300µA max. no damage will occur.

2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

MA548 FAMILY

10-MEMORY LD/DTMF SWITCHABLE DIALLER CHIPS

The MA548 family is a range of keypad switchable LD/DTMF dialler devices with Last Number Redial facility and ten 24-digit memories accessible via 10 dedicated keys.

Three operating modes are available: LD mode, with the ability to temporarily switch to DTMF mode from the keypad during a call, LD only mode and DTMF mode. The former mode enables users to access services such as home banking. Mixed LD and DTMF numbers can also be stored in memory.

The MA548 family is pin compatible with the GPS switchable dialler families MA544, MA545, MA547, MA541, MA585, MA587, MA588 and MA589 – providing a complete range of telephone features with a single PCB design.

Metal mask and pin selectable options are available to service the specific technical requirements of particular countries and for customers' preferred features and circuit configurations.

FEATURES

- Selectable Loop-Disconnect or DTMF Dialling Modes.
- Keypad Switchable LD to DTMF.
- 24 digit Last Number Redial.
- 10 x 24 Digit Memories (10 Dedicated Keys).
- Selectable Break/Make Ratios 2:1 and 3:2.
- Uses Inexpensive 560 kHz Ceramic Resonator.
- Batteryless Operation: Low Power CMOS.
- Standard DTMF timings: 100 ms ON, 100 ms OFF (minimum), Other Options Available
- PIN Confidentiality Feature.
- Timed Break Recall (Flash) and Earth Recall.
- Timed Pause Release.

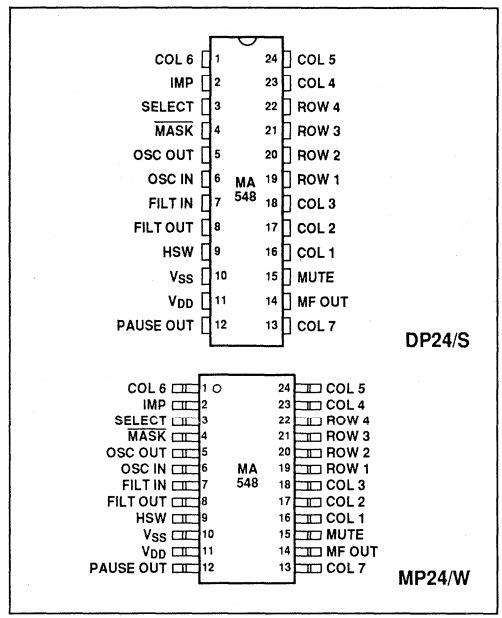


Fig. 1 Pin connections - top view (not to scale)

PIN FUNCTIONS

Pin Number	Pin Name	Function
2	IMP	'Loop disconnect' dialling output
3	SELECT	LD/DTMF selection, IDP and B/M ratio programming
4	$\overline{\text{MASK}}$	Output to disable speech circuit during pulse dialling and recall (see note 1)
5, 6	OSC OUT, OSC IN	Connections for 560 kHz ceramic resonator
7, 8	FILT IN, FILT OUT	Unity gain amplifier input and output for DTMF tone filtering
9	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-hook'
10	V_{SS}	Negative supply
11	V_{DD}	Positive supply
12	PAUSE OUT	Active high output indicating a pause when dialling from memory
14	MF OUT	Unfiltered DTMF output
15	MUTE	Output active during keying and tone transmission (see note 2)
16	COL1	Connections for 28 key single contact keypad
17	COL2	
18	COL3	
23	COL4	
24	COL5	
1	COL6	
13	COL7	
19	ROW1	
20	ROW2	
21	ROW3	
22	ROW4	

Note 1. The $\overline{\text{MASK}}$ output may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook, during a TBR (Timed Break Recall) operation or for LD dialling.

Note 2. The MUTE output is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1

OPERATION

Power-On

When power is applied to the chip, a power-on reset circuit operates and ensures that the stores are cleared and all logic is reset. On power-up the dialling mode is set to LD until a key is pressed. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the the stores may be corrupted, it will always, under all conditions, clear the stores so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA548 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the on-hook state is not recognised for 200-300 ms. On a device with Spanish DTMF (see page 6), the on-hook recognition time becomes 147-220ms when tones are being transmitted. This is so that short line breaks, such as line reversals applied by the exchange, are ignored. In this case the $\overline{\text{MASK}}$ and IMP outputs will go low immediately the HSW input goes low in order to conserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted. This conserves supply current so that the memory contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to logic '1' and remains there until dialling starts, a TBR (Flash) occurs or the HSW input goes low (see Figs. 4 and 5). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7 ms intervals on each output in sequence. A key is accepted as valid when two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minumum bounce-free key closure period which is necessary to guarantee detection is 14 ms (plus the oscillator start up time if it was not already running).

Keypad layout and connections

	COL1	COL2	COL3	COL4	COL5	COL6	COL7
ROW1	1	2	3	TBR	S1	S2	S3
ROW2	4	5	6	LNR	S4	S5	S6
ROW3	7	8	9	STORE	S7	S8	S9
ROW4	*	0	#	PAUSE /CONT	MUTE	S0	LNR

Table 2

The keys * and # are used to change from LD to DTMF dialling and are available as digits when in DTMF mode.

TBR:	Timed Break Recall (Flash).
LNR:	Last Number Redial.
STORE:	Memory Programming.
PAUSE/CONT:	Insert pause in memory/continue dialling.
S0-S9:	Dedicated memory keys.
MUTE:	Activate MUTE output.

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

SELECT pin to:	Dialling Mode	IDP (ms)	B/M Ratio
V_{SS}	LD + DTMF	800	2:1
COL1	LD + DTMF	500	2:1
COL2	LD + DTMF	500	3:2
COL3	LD + DTMF	800	3:2
COL4	LD ONLY	800	2:1
COL5	LD ONLY	500	2:1
COL6	LD ONLY	500	3:2
COL7	LD ONLY	800	3:2
V_{DD}	DTMF	-	-

Table 3

The dialling mode may be selected via the SELECT pin (pin 3) as detailed in Table 3. Four 'Loop-Disconnect + DTMF' options and four 'Loop-Disconnect only' options with different Inter-digit pauses and Make/Break ratios are available and one DTMF mode.

If one of the 'LD only' modes or the DTMF mode is selected, then dialling will remain fixed in LD mode or DTMF mode respectively. However, if one of the 'LD + DTMF' modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing the */# key provided that dialling is not in progress. If either of these keys are pressed during LD dialling they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

Keying PAUSE while dialling, or changing to DTMF mode will cause a delay of 3.5 seconds before the next digit is output.

Last Number Redial (LNR)

The function of the on-chip LNR store is to automatically retain a manually dialled number for redialling later. The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. To redial a number in the LNR store, the LNR key must be pressed once.

The last number redial store has several features designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the LNR key. In this case, the remainder of the number will be dialled when the LNR key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode calls

In the case of a call which starts in LD mode and is switched by the user (via the */# key) to DTMF mode, only the digits dialled in LD mode will be retained. Providing that the number of digits dialled in LD mode does not exceed 24, they will be retained regardless of the number of DTMF digits entered subsequently. This feature is provided to ensure security of PIN (Personal Identification Number) codes.

DTMF calls

If a call contains the characters * or #, only those digits dialled prior to the first press of either * or # will be retained in the LNR store. The exception to this is when either * or # is the first character dialled in a call, in which case all digits dialled (including further * or # characters) will be retained. This feature also ensures security for PIN codes whilst allowing exchange facility codes (for example) to be retained.

Memory Dialling

The MA548 provides 10 memories, each of which has a capacity of 24 digits. There are 10 dedicated memory keys. The memories can store pauses and digits to be dialled in LD, DTMF or mixed modes.

Programming memories

The MA548 must be 'off-hook' and idle:

1. Press the STORE key.
2. Press S0-S9 indicating the memory to be programmed.
3. Enter digits to be stored (no digits will be dialled whilst programming.
4. To finish programming the memory either press the STORE key again or go 'on-hook'.
5. Repeat to programme other memories.

If more than 24 digits are entered while programming a memory, then the memory will be cleared until reprogrammed. If any 'non-valid' keys are pressed during programming (e.g. LNR, TBR) they will be ignored.

Mixed Mode Numbers and Pauses in Memory

Mixed mode (i.e. LD + DTMF) numbers are easily programmed into memory. The SELECT pin must be set to one of the 'LD + DTMF' modes (as it would be when dialling a mixed mode number), then the store is programmed using the same procedure as above. The first press of */# will be stored as a 'change to DTMF' and this will cause all subsequent digits to be sent in DTMF when redialling from memory.

Similarly, pauses can be stored in memory by pressing the PAUSE key in the appropriate position when programming.

When dialling from memory both pauses and LD to DTMF changeovers will cause dialling to halt for 3.5 seconds. The exception to this rule is when a changeover is stored in the first memory location: In this case, DTMF dialling will occur immediately when memory dialling is invoked - this allows DTMF codes to be easily stored and sent even in a telephone where the normal dialling mode is LD.

It should be noted that a pause or an LD to DTMF changeover each require one memory location.

Dialling from Memories

The MA548 must be 'off-hook' and idle:

1. Press the appropriate memory key S0-S9. Dialling will now start.
2. If dialling halts due to a pause or an LD to DTMF changeover in the memory, the PAUSE OUT pin will go high (logic '1'). Further dialling will be resumed after 3.5 seconds. The PAUSE OUT output is reset when dialling resumes.

All keypad positions are disabled whilst memory dialling is in progress.

Timed Break and Earth Loop Recall (Flash)

The MA548 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the dialling mode selected via the SELECT pin will be restored. Also, only the digits dialled before the ELR/TBR operation will be retained in the LNR store.

A TBR (Flash) of 100 ms [1] is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the COLUMN 3 pin. If this pin is connected to ground for a minimum of 20 ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown in Fig. 2, or by use of a double contact switch.

Grounding COLUMN 3 will not directly affect the chip outputs. However, in order to prevent misoperation, the HSW timeout will be disabled during ELR. This is so that the MA548 cannot go into the on-hook state if the HSW input goes low as a result of ELR signalling (i.e whilst the telephone is, in reality, still off-hook). The $\overline{\text{MASK}}$ and IMP outputs will respond as normal to the status of the HSW input.

(1) Other TBR (Flash) periods are available as mask options (see page 6).

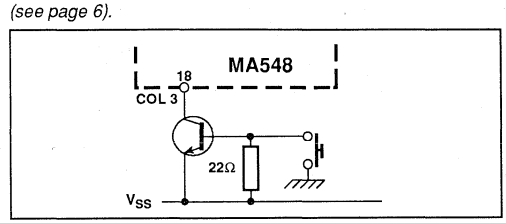


Fig. 2 Earth loop recall

Mute Facility

A Mute facility is provided to allow the user to mute the transmit path (i.e. the microphone) while still being able to hear the receive path.

A keypad postion is provided for this facility, whenever, and for as long as, the Mute key is pressed, the MUTE output will be active (logic '1') in order to disable the transmit path of the speech circuit. This is the same action as during DTMF transmission.

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 7 & 8) for use in a low pass active filter.

Fig. 3 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5 dB.

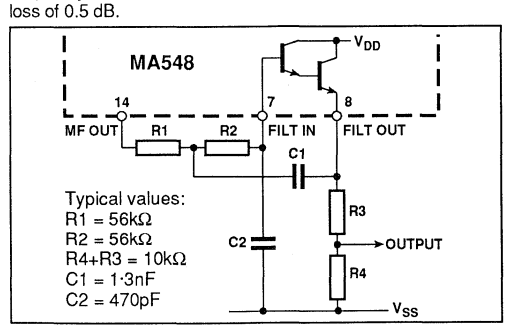


Fig. 3 DTMF tone filtering

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the 'single pin' type. Internally, the OSC IN pin is connected to V_{SS} and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

DTMF Dialling

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission. The IMP output remains low during tone transmission. The MF OUT output rises to its DC level of 0.9 V_{DD} at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100 ms on, followed by 100 ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate. Dialling from the LNR store and memories occurs at the maximum rate.

If a key is held down for longer than 100 ms, the tone output will continue until the key is released.

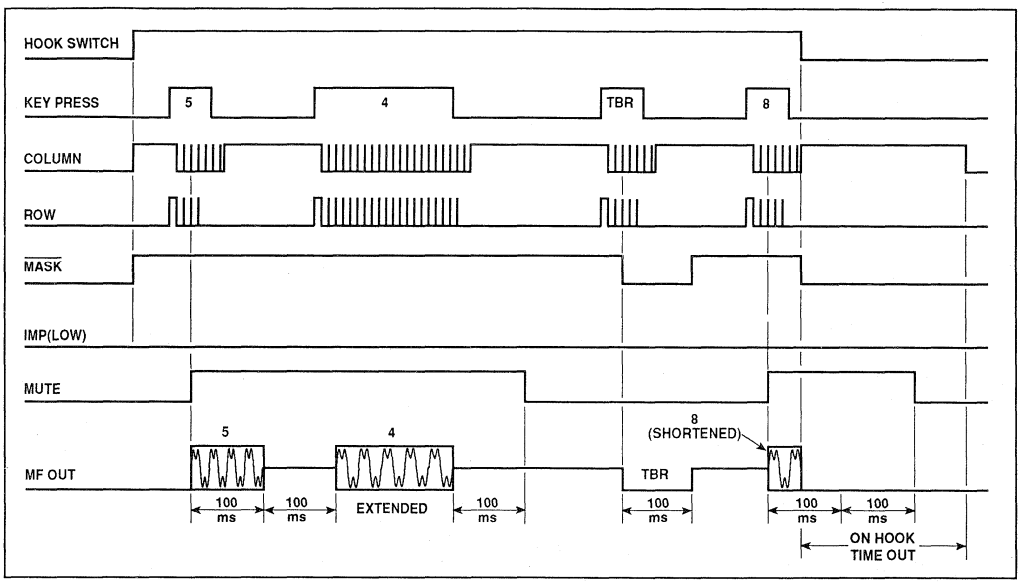


Fig. 4 DTMF mode timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477
Deviation from nominal (%)	-0.07	-0.10	+0.19	-0.15	-0.17	-0.20	-0.22

There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560 kHz.

Table 4 Tone frequencies

Loop-Disconnect Dialling

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic '0' during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling.

LD dialling is signalled on the IMP output: a break is signalled by a logic '0'; make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

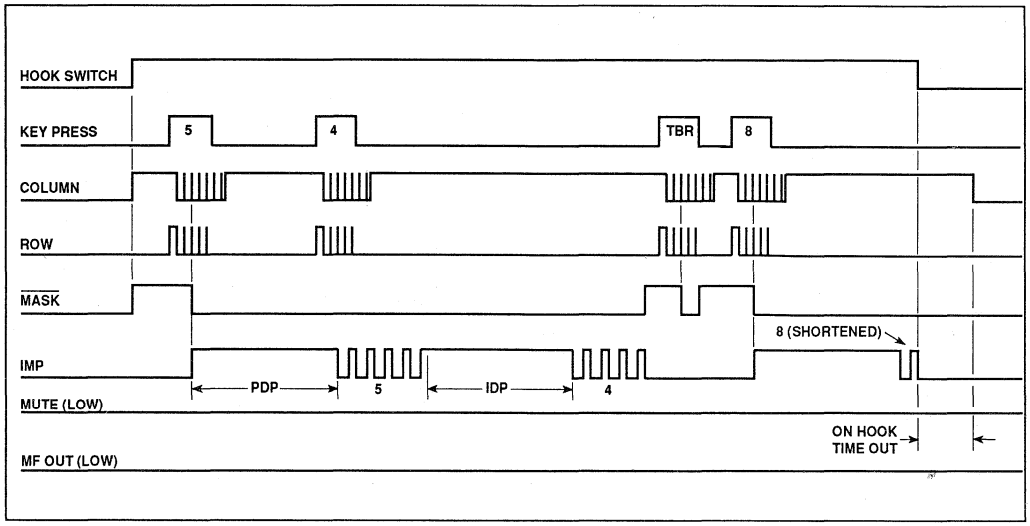
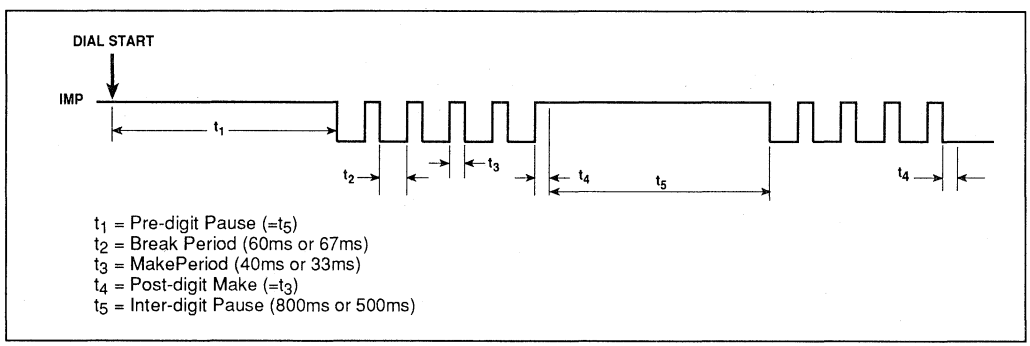


Fig. 5 LD mode timing diagram



t_1 = Pre-digit Pause (=t_5)
t_2 = Break Period (60ms or 67ms)
t_3 = MakePeriod (40ms or 33ms)
t_4 = Post-digit Make (=t_3)
t_5 = Inter-digit Pause (800ms or 500ms)

Fig. 6 Timing data

MASK OPTIONS

The MA548 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufacture. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit.

The options, listed below, are possible in any combination. Standard options are listed first in italics at 'a'. Other options may be produced by arrangement.

1. TBR (Flash) Period:
a. 100 ms
b. 200 ms
c. 300 ms
d. 400 ms
e. 500 ms
f. 600 ms

2. LD to DTMF Keypad Switching:
*a. * and # keys*
b. * key
c. No keypad switching

3. Retention of Post-*/# digits in LNR store (DTMF mode):
*a. Digits before * or # retained (except when * or # is first digit).*
b. Digits before * or # retained.
c. All digits retained.

4. LD dialling options:
a. Standard (n = n pulses, where 0 = 10)
b. Swedish (n = n + 1 pulses)
c. Norwegian (n = (11-n) pulses)
d. New Zealand (n = (10-n) pulses)

5. Recall (Flash)/LNR Protocol:
a. Digits after recall retained in LNR store
b. Digits before recall retained in LNR store
c. Recall inhibits LNR
d. For Danish PABX requirements

6. DTMF Minimum Timings:
a. 100 ms on, 100 ms off (UK PTT preferred)
b. 73.3 ms on, 73.3 ms off
c. 73.3 ms on, 146.7 ms off (Spanish PTT preferred)
d. 80 ms on, 80 ms off (German PTT preferred)

7. Pin 4:
a. $\overline{MASK}$
b. MASK

8. Pin 2:
a. IMP
b. $\overline{IMP}$
c. [IMP+$\overline{MASK}$]
d. $\overline{[IMP+\overline{MASK}]}$

9. Pin 15:
a. MUTE
b. $\overline{MUTE}$
c. $\overline{MUTE}$ (Open-drain)

10. Timed Pause Release
a. 3.5 sec.
b. 0.5 to 7.0 sec in 0.5 steps

11. TBR Availability
a. LD and DTMF mode
b. DTMF mode only

ABSOLUTE MAXIMUM RATINGS

Parameter	Min.	Typ.	Max.	Units	Notes
Supply voltage V_{DD}-V_{SS}	-0.3	-	6.5	V	-
Voltage on any pin (except HSW)	V_{SS}-0.3	-	V_{DD}+0.3	V	-
Voltage on pin HSW	V_{SS}-0.3	-	-	V	See Note 1
Current at any pin (except HSW. FILTOUT and FILTIN)	-1	-	1	mA	
Current at pin FILTOUT	0	-	0.1	mA	-
Current at pin FILTIN	-5	-	0	mA	-
Operating temperature	-25	-	70	°C	-
Storage temperature	-55	-	125	°C	-

Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress ratingonly and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not Implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note 1. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300µA max. no damage will occur.
Note 2. These temperature ranges do not apply to all package types. Many package types are available and these may have limited temperature ranges. Further information is available on request.

Table 5

DC OPERATING CONDITIONS AND CHARACTERISTICS (Note 4)

Condition		Min.	Typ.	Max.	Units	Notes
Supply voltage:	On-hook	1.8	-	5.7	V	For memory retention
	Off-hook	2.4		5.7	V	
Hookswitch input:	On-hook	-	-	0.2 V_{DD}	-	-
	Off-hook	0.8 V_{DD}		-		

Characteristic		Min.	Typ.	Max.	Units	Notes
Supply current:	On-hook	-	0.1	5	µA	At V_{DD} = 2.0 V
	Off-hook		1.5		µA	True only if MF OUT is low
	MF tone sending			1.0	mA	-
	LD impulsing			200	µA	-
Output high voltage ($\overline{MASK}$,IMPand PAUSE outputs)		2.2	-		V	I = −1 mA
Output off leakage (MUTE)		-	< 0.1	1	µA	$V_{MUTE} \leq V_{DD}$. Note 5.
Output low voltage ($\overline{MASK}$, MUTE, IMP and PAUSE outputs)		-	-	0.3	V	I = +1 mA
MF OUT DC level during tone sending		-	0.9 V_{DD}	-	V	-
MF OUT output resistance		-	3	5	kΩ	-
'Key Pressed' resistance		-	-	2	kΩ	2.5 V < V_{DD}< 5.7 V
'Key Not Pressed' resistance		500	-	-	kΩ	2.5 V < V_{DD}< 5.7 V
Darlington pair current gain		600	50,000	-	-	I_e = 100µA, V_{ce} = 2 V

Note 4. V_{DD} = 2.5 V at 25°C unless otherwise specified.
Note 5. A diode is internally connected between this pin and V_{DD}. The MUTE output may he held at a voltage above V_{DD} provided that current is externally limited to 300 µA max.

Table 6

AC OPERATING CONDITIONS AND CHARACTERISTICS

Condition	Min.	Typ.	Max.	Units	Notes
Oscillating Frequency	-	560	-	kHz	-

Characteristic		Min.	Typ.	Max.	Units	Notes
Tone Output:	Low Group	57	64	-	mV r.m.s.	No load. V_{DD} = 2.5V
	High Group		81	91	mV r.m.s.	No load. V_{DD} = 2.5V
High-to-low Group Amplitude ratio (pre-emphasis)		1.5	2	2.5	dB	See Note 6
Total Harmonic Distortion:	0-4 kHz	-	1.5	-	%	-
	0-10 kHz	-	2.5	-	%	-
	0-50 kHz	-	5.0	-	%	-
	0-200 kHz	-	6.5	10	%	-
Oscilllator Start-up Time		-	< 0.1	1	ms	-

Note 6. Typical value varies slightly dependent upon particular tone pair.

Table 7

MA585 FAMILY

LD/DTMF SWITCHABLE DIALLERS WITH 20 MEMORIES

The MA585 family are keypad switchable LD/DTMF dialler devices with a last number redial facility and twenty 24-digit memories.

Two operating modes are available: LD mode, with the ability to temporarily switch to DTMF mode from the keypad during a call, and DTMF only mode. The former mode enables subscribers to access such services as home banking. Mixed LD and DTMF numbers can also be stored in memory.

The MA585 devices are pin compatible with the GPS switchable dialler families MA526, MA527, MA541, MA545, MA547. MA587 and MA589 - providing a complete range of telephone features within a single PCB and circuit design.

Metal mask and pin selectable options are available to service specific requirements of particular countries and customers.

FEATURES

- Selectable Loop-Disconnect or DTMF Modes
- Keypad Switchable LD to DTMF
- 24 Digit Last Number Redial
- 20 x 24-Digit Memories
- Selectable Make/Break Ratios 2:1 and 3:2
- Uses Inexpensive 560kHz Ceramic Resonator
- Battery-less operation - Low Power CMOS
- Mask Programmable Options to suit Application
- Timed Break Recall (Flash) and Earth Recall

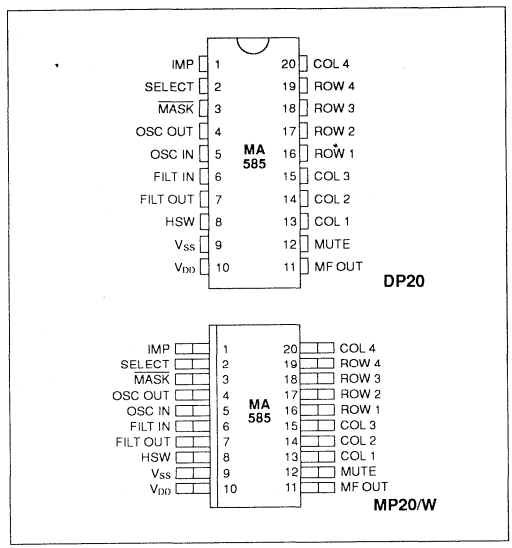


Figure 1: Pin connections - top view (not to scale)

PIN FUNCTIONS

Pin number	Pin name	Function
1	IMP	'Loop disconnect' dialling output
2	SELECT	LD/DTMF selection, IDP and B/M radio programming
3	MASK	Output to disable speech circuit during pulse dialling and recall (see note 1)
4	OSC OUT	Connections for 560kHz ceramic resonator
5	OSC IN	
6	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
7	FILT OUT	
8	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-hook'
9	V_{SS}	Negative supply
10	V_{DD}	Positive supply
11	MF OUT	Unfiltered DTMF output
12	MUTE	Output active during keying and tone transmission (see note 2)
13	COL1	Connections for 16 button single contact keypad
14	COL2	
15	COL3	
16	ROW1	
17	ROW2	
18	ROW3	
19	ROW4	
20	COL4	

1. MASK may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.
2. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1: Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA585 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from 0 to 1 the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from 1 to 0 the onhook state is not recognised for 200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied bv the exchange, are ignored. In this case the IMP and $\overline{\text{MASK}}$ outputs will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted.This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic 1 level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

	COL 1	COL 2	COL 3	COL 4
ROW 1	1	2	3	TBR
ROW 2	4	5	6	REDIAL
ROW 3	7	8	9	STORE
ROW 4	*	0	#	PAUSE

TBR: Timed Break Recall (Flash)
REDIAL: Last Number and Memory Redial
STORE: Memory programming
PAUSE: Insert pause in memory
TONE: (1) Change dialling mode from LD to DTMF

(1) *Only available as a mask option, replacing the PAUSE key. TONE can be used to insert pauses in memory but only during DTMF dialling.*

Figure 2: Keypad layout and connections

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start-up time if it was not already running).

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

The dialling mode may be selected via the SELECT pin (pin 2) as detailed in Table 2. Four Loop-Disconnect options are available with different Interdigit pauses and Break/Make ratios, and one DTMF mode. If the DTMF mode is selected then dialling will remain fixed in the DTMF mode. However, if one of the LD modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing either the *, */# or TONE key (depending on the mask variant - see Fig. 2 and page 1-36), provided that dialling is not in progress. If any of these keys are pressed during LD dialling, they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

SELECT pin to	Dialling mode	IDP (ms)	B/M ratio
V_{SS}	LD	800	2:1
COL 1	LD	500	2:1
COL 2	LD	500	3:2
COL 3	LD	800	3:2
V_{DD}	DTMF	-	-

Table 2: Dialling mode selection

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. To redial a number in the LNR store, the REDIAL key must be pressed twice.

The last number redial store has several features designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the REDIAL key; the remainder of the number will be dialled when the REDIAL key is pressed.

•If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of

the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and is switched by the user (via the *, */#, or TONE key) to DTMF mode, only the digits dialled in LD mode will be retained. This feature is provided to ensure security of PIN (Personal Identificabon Number) codes. Provided that the number of digits dialled in LD mode does not exceed 24, they will be retained regardless of the number of DTMF digits entered subsequently.

Memory Dialling

The MA585 provides 20 memories, each of which has a capacity of 24 digits. The memories can store digits to be dialled in LD, DTMF or Mixed modes and also pauses.

Programming Memories

The MA585 must be off-hook and idle:

1. Press the STORE key.
2. Press the number (00-19) of the memory to be programmed.
3. Enter digits to be stored (no digits will be dialled whilst programming)
4. To finish programming the memory ei!her press the STORE key again or go on-hook .
5. Repeat to programme other memories.

If more than 24 digits are entered while programming a memory, then the memory will be cleared until reprogrammed. If any non-valid keys are pressed during programming (e.g. REDIAL,TBR) they will be ignored.

Mixed mode numbers and pauses In memory

Mixed mode (i.e LD + DTMF) numbers are easily programmed into memory. The SELECT pin should be set to one of the LD plus DTMF modes (as it would be when dialling a mixed mode number), then the number entered using the same procedure as if programming normally. The first press of *, */# or TONE (according to the mask variant) will be stored as a change to DTMF, and this will cause all subsequent digits to be sent in DTMF when redialling from memory.

Similarly, pauses can be stored in memory by pressing the PAUSE key in the appropriate position when programming.

When redialling from memory, both pauses and LD to DTMF changeovers will cause dialling to halt temporarily until the user presses either the REDIAL or PAUSE key. The exception to this rule is when an LD to DTMF changeover is stored in the first memory location: In this case DTMF dialling will occur immediately when memory dialling is invoked - this allows DTMF codes to be easily stored and sent even in a telephone where the normal dialling mode is LD.

It should be noted that a pause or an LD to DTMF changeover each require one memory location.

Dialling from memories

The MA585 must be off-hook and idle:

1. Press the REDIAL key once.
2. Press the number (00-19) of the memory to be dialled. Dialling will now start.
3. If dialling halts due to a pause or an LD to DTMF changeover in the memory, further dialling can be resumed by pressing the REDIAL or the PAUSE key. Alternatively, the Column 4 pin can be pulled low (for a minimum of 14 ms) in order to achieve the same result, thus allowing an external timer circuit to be used.

All keypad positions are disabled whilst memory dialling is in progress.

Timed Break & Earth Loop Recall (Flash)

The MA585 supports both TBR and ELR and offers a common operating protocol in both cases.

Afler a recall (Flash) operation, the dialling mode selected via the SELECT pin will be restored. Also, only the digits dialled afler the ELR/TBR operation will be retained in the LNR store [1].

A TBR (Flash) of 100ms [2] is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin. If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fiy. 3, or by use of a double contact switch.

[1] Other options are available, including an option for Danish requirements (see page 1-50). In Denmark, TBR (or ELR) is used to obtain an outside line in PABX use. Under these conditions the LNR store contents will be retained and can be redialled after a TBR or ELR. Digits manually entered afler a TBR or ELR will become the new LNR store contents.

[2] Other TBR (Flash) periods are available as mask options (see page 1-50).

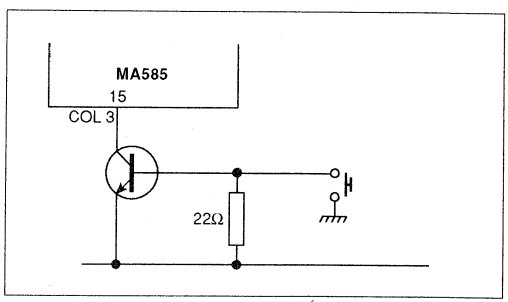


Figure 3: Earth loop recall

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the single pin type. Internally, the OSC IN pin is connected to V_{SS} and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

Tone Filtering

The spectral purity ot the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 6 & 7) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

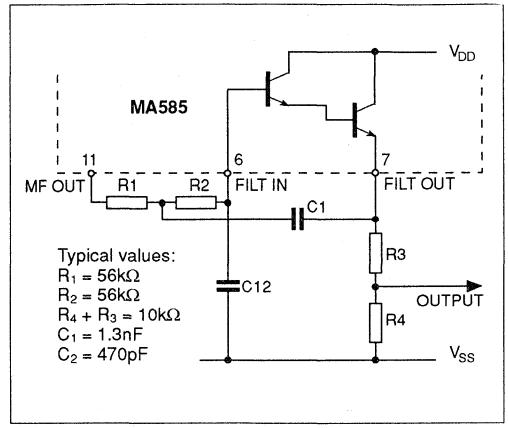


Figure 4: DTMF tone filtering

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic 1 and remains there for the duration of the tone transmission. The IMP output remains low duling tone transmission The MF OUT output rises to its DC level of 0.9 V_{DD} at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate.

If a key as held down for longer than 100ms, the tone output will continue until the key is released.

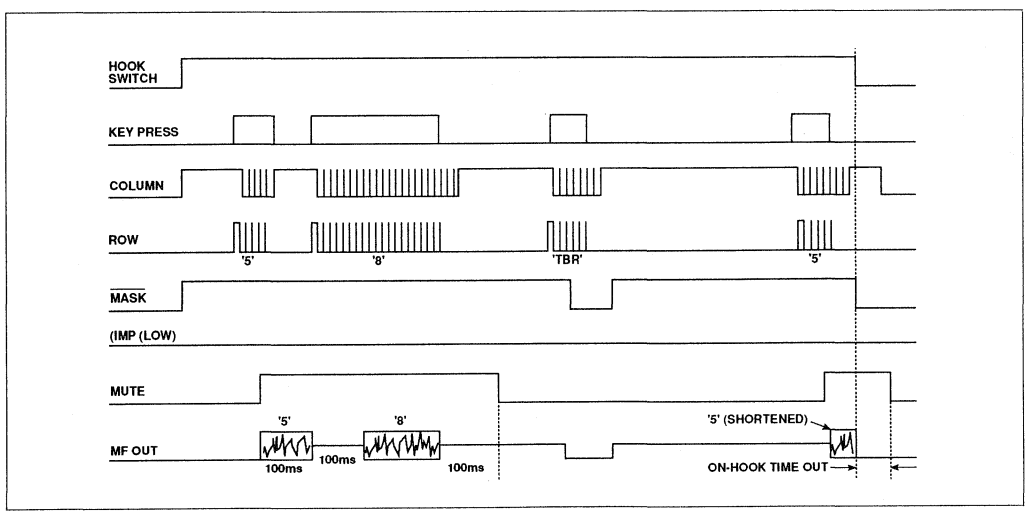


Figure 5: DTMF timing diagram

LOOP-DISCONNECT DIALLING

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic 0 during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling. LD dialling is signalled on the IMP output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	-0.07	-0.10	+0.19	-0.15	-0.17	-0.20	-0.22	-0.31

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 3: Tone frequencies

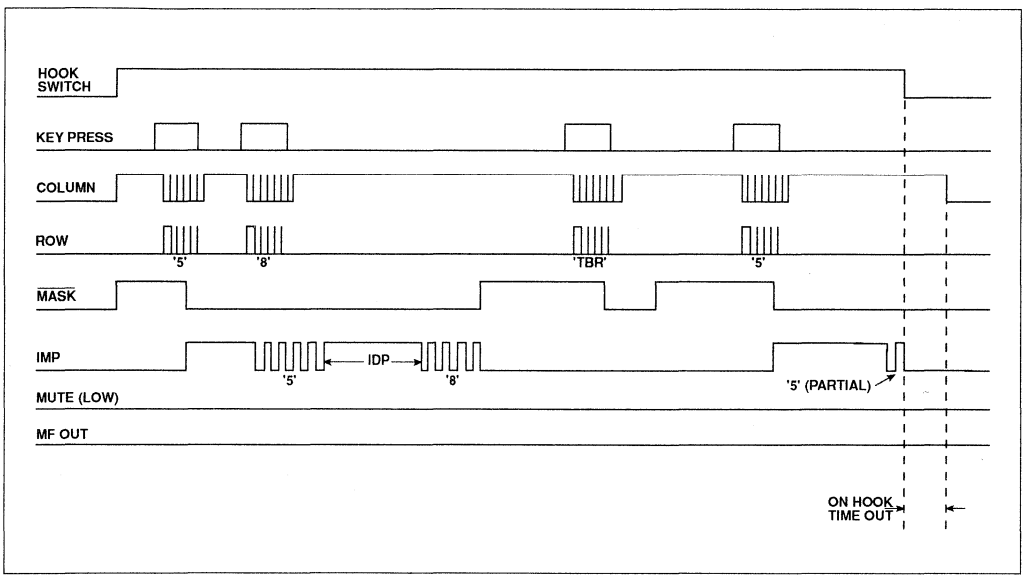


Figure 6: LD mode timing diagram

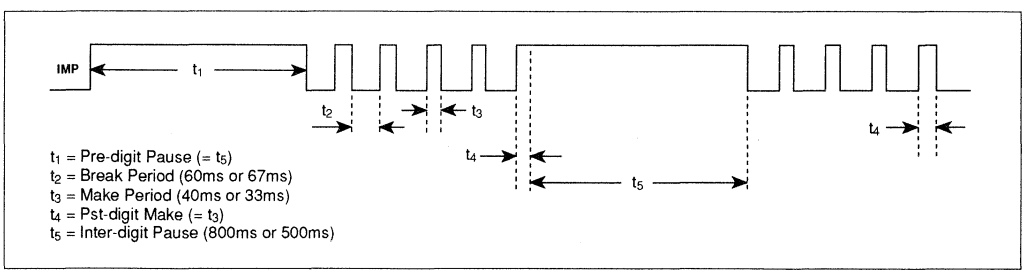


Figure 7: Timing data

MASK OPTIONS

The MA585 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufactute. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit. The options, listed below, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

1. TBR (Flash) Period
a. 100 ms
b. 200 ms
c. 300 ms
d. 400 ms
e. 500 ms
f. 600 ms

2. LD to DTMF Keypad Switching
a. *and ,# keys
b. TONE key
c, * key

3. Retention of Post - */# Digits in LNR Store (DTMF mode)
a. All digits retained
b. Digits before * or # retained
c. Digits before * and # retained (except when * or # is first digit

4. LD dialling options
a. Standard (n = N pulses, except 0 = 10 pulses)
b. Swedish (n = (n + 1) pulses)
c. Norwegian (n = (11 - n) pulses)
d. New Zealand (n = (10 - n) pulses)

5. Recall (Flash) / LNR Protocol
a. Digits dialled after Recall retained
b. Digits dialled before Recall retained
c. Recall inhibits LNR
d. For Danish PABX requirements

6. DTMF Minimum Timings
a. 100ms on, 100ms off
b. 73ms on, 73ms off
c. 73ms on, 147ms off

7. Keyboard Options (Key Position COL4, ROW4)
a. PAUSE key
b. TONE key (see option 2b)\
c. LNR key (single press, replaces double press of REDIAL)

8. Pin 3
a. $\overline{MASK}$
b. MASK

9. Pin 1
a. IMP
b. $\overline{IMP}$
c. [IMP + $\overline{MASK}$]
d. [$\overline{IMP}$ + MASK]

10. Pin 12
a. MUTE
b. $\overline{MUTE}$

APPLICATION CIRCUITS

Refer to the MA541 data sheet, Figs. 8 and 9, on pages 1-29 and 1-30

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Supply current:	On-hook		<1	5.0	µA	V_{DD} = 2.0V
	Off-hook		1.5		µA	MF OUT low
	MFtone sending			1.0	mA	
	LD impulsing				µA	
Output high voltage ($\overline{MASK}$ and MUTE outputs)		2.2			V	I = -1mA
Output low voltage ($\overline{MASK}$ and MUTE outputs)				0.3	V	I = +1mA
MF OUT DC level during tone sending			$0.9V_{DD}$		V	
MF OUT output resistance			3		kΩ	
'Key Pressed' resistance				2	kΩ	2.5V < V_{DD} < 5.7V
'Key Not Pressed' resistance		500			kΩ	2.5V < V_{DD} < 5.7V
Darlington pair current gain (see fig 4)		600	50,000			I_E = 100µA, V_{CE} = 2V

NOTE 1. Specially tested versions with guaranteed lower on-hook supply current are available.

AC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Tone output:	low group	57	64		mV rms	No load.
	high group		81	91	mV rms	No load.
High-to-Low group amplitude ratio (pre emphasis)		1.5	2	2.5	dB	See note 2
Total harmonic distortion:	0-4 kHz		1.5		%	
	0-10 kHz		2.5		%	
	0-50 kHz		5.0		%	
	0-200 kHz		6.5	10	%	
Oscillator start-up time			<0.1	1	ms	

NOTE 2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition		Min.	Typ.	Max.	Units	Notes
Supply Voltage:	On-hook	1.8		5.7	V	For memory retention
	Off-hook	2.4		5.7	V	
Hookswitch input:	On-hook			$0.2V_{DD}$	V	
	Off-hook	$0.8V_{DD}$			V	
Oscillating frequency			560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}-V_{SS}	- 0.3 to + 6 5V
Voltage on any pin (except HSW)	V_{SS} - 0.3V to V_{DD} + 0 3V
Voltage on HSW pin (See note 1)	V_{SS} - 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	±1 mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	-5 to 0mA
Storage temperature	-55°C to + 125°C
Operating temperature range	-10°C to + 55°C

NOTES

1. A diode is internally connected between this pin and VDD. Provided current is externally limited to 300/1A max. no damage will occur.

2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

MA587 FAMILY

LD/DTMF SWITCHABLE DIALLERS WITH 20 MEMORIES (10 DEDICATED MEMORY KEYS)

The MA587 family are keypad switchable LD/DTMF dialler devices with a last number redial facility and twenty 24-digit memories, accessible via 10 dedicated dialling keys. Three operating modes are available: LD only mode, DTMF only mode and LD mode with the ability to switch temporarily to DTMF mode from the keypad during a call This last mode enables subscribers to access such services as home banking Mixed LD and DTMF numbers can also be stored in memory. The MA587 devices are pin compatible with the GPS switchable dialler families MA526 MA527, MA541, MA545 MA547, MA585 and MA589.

Providing a complete range of telephone features within a single PCB and circuit design. Metal mask and pin selectable options are available to service specific requirements of particular countries and customers.

FEATURES

- Selectable Loop-Disconnect or DTMF Modes
- Keypad Switchable LD to DTMF
- 20x24-Digit Memories, (10 Dedlcated Keys)
- 24 Digit Last Number Redial
- Selectable Make/Break Ratios 2:1 and 3:2
- Uses Inexpensive 560kHz Cerarnic Resonator
- Battery-less operation - Low Power CMOS
- Mask Programmable Options to suit Application
- Timed Break Recall (Flash) and Earth Recall

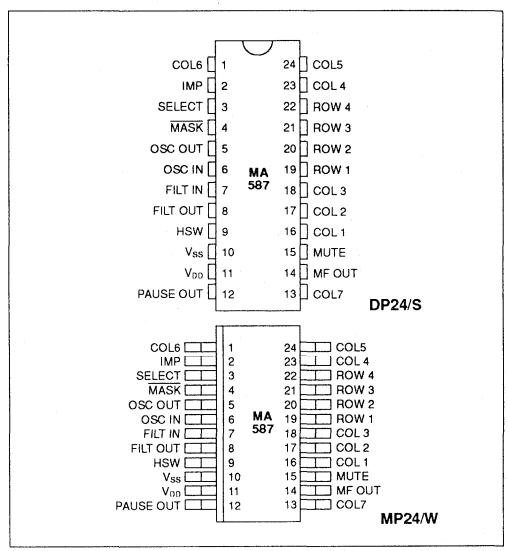


Figure 1: Pin connections - top view. DP24/S: 0.3in 'skinnydip' plastic DIL; MP24/W: wide-bodied Small Outline package

PIN FUNCTIONS

Pin number	Pin name	Function
2	IMP	'Loop disconnect' dialling output
3	SELECT	LD/DTMF selection, IDP and B/M radio programming
4	MASK	Output to disable speech circuit during pulse dialling and recall (see note 1)
5	OSC OUT	Connections for 560kHz ceramic resonator
6	OSC IN	
7	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
8	FILT OUT	
9	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-hook'
10	V_{SS}	Negative supply
11	V_{DD}	Positive supply
12	PAUSE OUT	Active high output indicating a pause when dialling from memory
14	MF OUT	Unfiltered DTMF output
15	MUTE	Output active during keying and tone transmission (see note 2)
16	COL1	Connections for 28 key single contact keypad
17	COL2	
18	COL3	
23	COL4	
24	COL5	
1	COL6	
13	COL7	
19	ROW1	
20	ROW2	
21	ROW3	
22	ROW4	

1. MASK may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.
2. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1: Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA587 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the on-hook state is not recognised for 200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied bv the exchange, are ignored. In this case the IMP and $\overline{\text{MASK}}$ outputs will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted.This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic '1' level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start-up time if it was not already running).

Simultaneous key depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has beell verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

The dialling mode may be selected via the SELECT pin (pin 3) as detailed in Table 2. Four 'Loop-Disconnect + DTMF options and tour 'Loop-Disconnect only' options with different Interdigit pauses and Break/Make ratios are available and one DTMF mode If one of the 'LD only' modes or the DTMF mode is selected then dialling will remain fixed in LD mode or DTMF mode respectively .

	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7
ROW 1	1	2	3	TBR	S1	S2	S3
ROW 2	4	5	6	LNR	S4	S5	S6
ROW 3	7	8	9	STORE	S7	S8	S9
ROW 4	*	0	#	PAUSE/ CONT	SHIFT	S0	

* or */# are used to change from LD to DTMF dialling and are available as digits when in DTMF mode

TBR: Timed Break Recall (Flash)
LNR: Last Number Redial
STORE: Memory programming
PAUSE/CONT: Insert pause in memory/continue dialling
SHIFT: Used in conjunction with the 10 dedicated memory keys, allows all 20 memories to be addressed
S0-S9: Dedicated memory dialling keys
TONE: Change dialling mode from LD to DTMF

	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7
ROW 1	1	2	3	TBR	S1	S2	S3
ROW 2	4	5	6	LNR	S4	S5	S6
ROW 3	7	8	9	STORE	S7	S8	S9
ROW 4	*	0	#	TONE	SHIFT	S0	PAUSE/ CONT

Figure 2: Keypad layout and connections

SELECT pin to	Dialling mode	IDP (ms)	B/M ratio
V_{SS}	LD + DTMF	800	2:1
COL 1	LD + DTMF	500	2:1
COL 2	LD + DTMF	500	3:2
COL 3	LD + DTMF	800	3:2
COL 4	LD only	800	2:1
COL 5	LD only	500	2:1
COL 6	LD only	500	3:2
COL 7	LD only	800	3:2
V_{DD}	DTMF	-	-

Table 2: Dialling mode selection

However, if one of the 'LD + DTMF' modes is selected, the chip will lie in LD mode inilially in the off-hook condition but may be switched lo DTMF by pressing either the *, */# or TONE key (depending on the mask variant - see Fig. 2 and page 1-57), provided that dialling is not in progress. If any of these keys are pressed during LD dialling, they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialllng later The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. To redial a number in the LNR store, the LNR key must be pressed once.

The last number redial store has several features designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the LNR key; the remainder of the number will be dialled when the LNR key is pressed.

If the digit(s) dialled manually do not match those in the LNR store. Then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and IS switched by the user (via the *, */#. or TONE key) to DTMF mode, only the digits dialied in LD rnode will be retained. This feature is provided to ensure security of PIN (Personal Identification Nurnber) codes. Provided that the number of digits dialled in LD mode does not exceed 24, they will be retained regardless of the number of DTMF digits entered subsequently.

Memory Dialling

The MA587 provides 20 memories, each of which has a capacity of 24 digits There are 10 dedicated memory keys and a SHIFT key which allows all 20 memories to be addressed by the 10 memory keys The memories can store digits to be dialled in LD, DTMF or mixed modes and also pauses.

Programming Memories

The MA587 must be 'off-hook' and idle:

1. Press the STORE key
2. Press key S0-S9 or SHIFT + S0-S9 indicating the memory to be programmed
3. Enter digits to be stored (no digits will be dialled whilst programming)
4. To finish programming the memory either press the STORE key again or go 'on-hook'.
5. Repeat to programme other memories.

If more than 24 digits are entered while programming a memory, then the memory will be cleared until reprogrammed If any non-valid keys are pressed during programming (e.g. LNR,TBR) they will be ignored Mixed mode numbers and pauses in memory.

Mixed mode (i.e LD + DTMF) numbers are easily programmed into memory. The SELECT pin should be set to one of the 'LD + DTMF' modes (as it would be when dialling a mixed mode number), then the number entered using the same procedure as if dialling normally The first press of *, * '# or TONE (according to the mask variant) will be stored as a 'change to DTMF', and this wlll cause all subsequent digits to be sent in DTMF when redialling from memory.

Similarly, pauses can be stored in memory by pressing the PAUSE key in the appropriate position when programming .

When redialllng from memory, both pauses and LD to DTMF changeovers will cause dialling to halt temporarily until the user presses the PAUSE/CONT key. The exception to this rule is when an LD to DTMF changeover is stored in the first memory location: in this case, DTMF dialling will occur immediately when memory dialling is invoked - this allows DTMF codes to be easily stored and sent even in a telephone where the normal dialling mode is LD.

It should be noted that a pause or an LD to DTMF changeover each require one memory location

Dialling from memories

The MA587 must be 'off-hook' and idle:

1. Press the appropriate memory key S0-S9 or SHIFT + S0-S9. Dialling will now start.
2. If dialling halts due to a pause or an LD to DTMF changeover in the memory, the PAUSE OUT pin will go high (logic '1'). Further dialling can be resumed either by pressing the PAUSE/CONT key or, alternatively, the Column 4 pin can be pulled low (for a minimum of 14 ms) to achieve the same result, thus allowing an external timer circuit to be used. The PAUSE/OUT output is reset when dialling resumes.

All keypad positions are disabled whilst memory dialling is In progress

Timed Break & Earth Loop Recall (Flash)

The MA587 supports both TBR and ELR and offers a common operating protocol in both cases

After a recall (Flash) operation. the dialling mode selected via the SELECT pin will be restored Also, only the digits dialled after the ELR TBR operation will be retained in the LNR store [1].

A TBR (Flash) of 100ms [2] is generated when the TBR key IS pressed The MASK output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break

ELR is supported via the column 3 pin If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will ofter the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fig 3, or by use of a double contact switch.

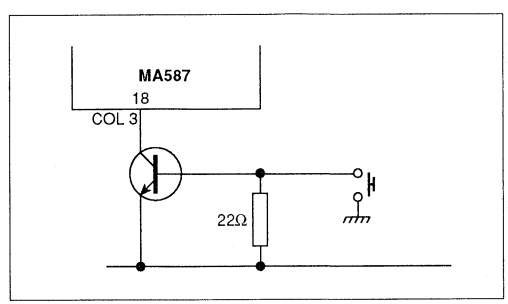


Figure 3: Earth loop recall

(1) Other options are available including an option for Danish requirements (see page 1-57). In Denmark TBR (or ELR) is used to obtain an outside line in PABX use. Under these conditions the LNR store contents will be retained and can be redialled after a TBR or ELR. Digits manually entered after a TBR or ELR will become the new LNR store contents.

(2) Other TBR (Flash) periods are available as mask options (see page 1-57).

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the 'single pin' type. Internally, the OSC IN pin is connected to V_{SS} and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 7 & 8) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

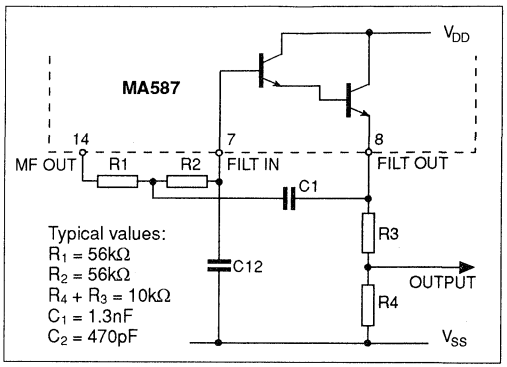


Figure 4: DTMF tone filtering

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission .

The IMP output remains low during tone transmission. The MF OUT output rises to its DC level of 0.9 V_{DD} at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate al which tones are sent to line is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate. Dialling from the LNR store occurs at the maximum rate.

If a key is held down for longer than 100ms, the tone output will continue until the key is released.

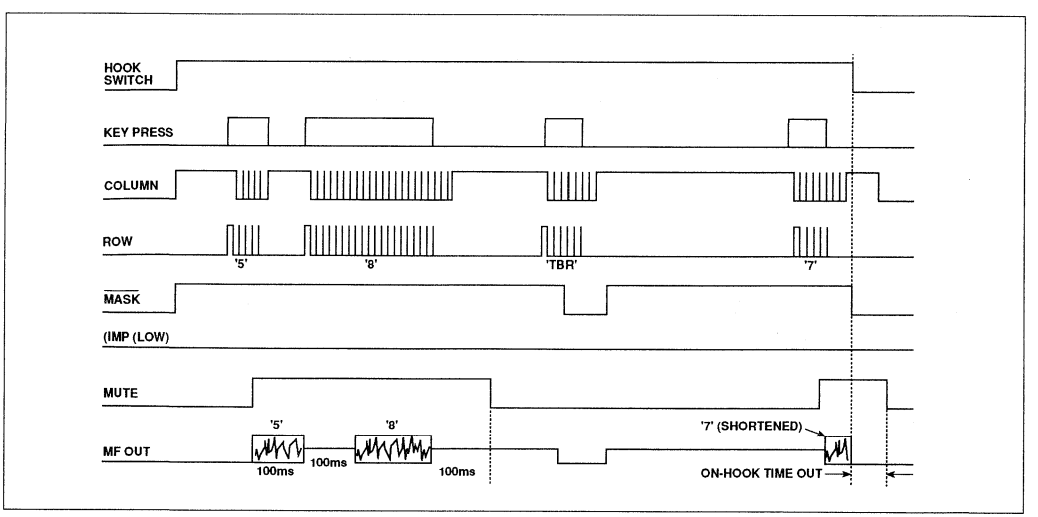


Figure 5: DTMF mode timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	-0.07	-0.10	+0.19	-0.15	-0.17	-0.20	-0.22	-0.31

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 3: Tone frequencies

LOOP-DISCONNECT DIALLING

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic 0 during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling. LD dialling is signalled on the IMP output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

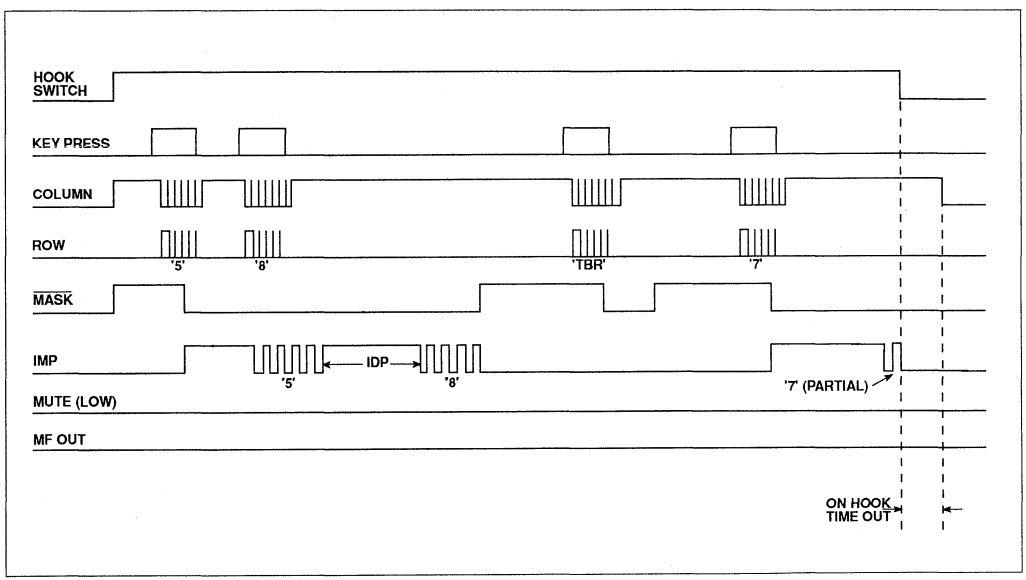


Figure 6: LD mode timing diagram

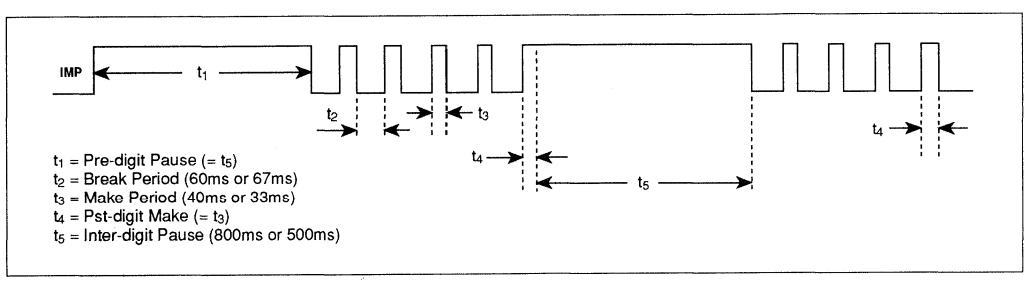


Figure 7: Timing data

MASK OPTIONS

The MA587 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufactute. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit. The options, listed below, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

1. TBR (Flash) Period
a. 100 ms
b. 200 ms
c. 300 ms
d. 400 ms
e. 500 ms
f. 600 ms

2. LD to DTMF Keypad Switching
a. *and ,# keys
b. TONE key
c, * key

3. Retention of Post - */# Digits in LNR Store (DTMF mode)
a. All digits retained
b. Digits before * or # retained
c. Digits before * and # retained (except when * or # is first digit

4. LD dialling options
a. Standard (n = N pulses, except 0 = 10 pulses)
b. Swedish (n = (n + 1) pulses)
c. Norwegian (n = (11 - n) pulses)
d. New Zealand (n = (10 - n) pulses)

5. Recall (Flash) / LNR Protocol
a. Digits dialled after Recall retained
b. Digits dialled before Recall retained
c. Recall inhibits LNR
d. For Danish PABX requirements

6. DTMF Minimum Timings
a. 100ms on, 100ms off
b. 73ms on, 73ms off
c. 73ms on, 147ms off

7. Pin 4
a. $\overline{MASK}$
b. MASK

8. Pin 2
a. IMP
b. $\overline{IMP}$
c. [IMP + $\overline{MASK}$]
d. [$\overline{IMP}$ + MASK]

9. Pin 15
a. MUTE
b. $\overline{MUTE}$

APPLICATION CIRCUITS

Refer to the MA541 data sheet, Figs. 8 and 9, on pages 1-29 and 1-30

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Supply current:	On-hook		<1	5.0	µA	V_{DD} = 2.0V
	Off-hook		1.5		µA	MF OUT low
	MFtone sending			1.0	mA	
	LD impulsing				µA	
Output high voltage ($\overline{MASK}$ and MUTE outputs)		2.2			V	I = -1mA
Output low voltage ($\overline{MASK}$ and MUTE outputs)				0.3	V	I = +1mA
MF OUT DC level during tone sending			$0.9V_{DD}$		V	
MF OUT output resistance			3		kΩ	
'Key Pressed' resistance				2	kΩ	2.5V < V_{DD} < 5.7V
'Key Not Pressed' resistance		500			kΩ	2.5V < V_{DD} < 5.7V
Darlington pair current gain (see fig 4)		600	50,000			I_E = 100µA, V_{CE} = 2V

NOTE 1. Specially tested versions with guaranteed lower on-hook supply current are available.

AC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Tone output:	low group	57	64		mV rms	No load.
	high group		81	91	mV rms	No load.
High-to-Low group amplitude ratio (pre emphasis)		1.5	2	2.5	dB	See note 2
Total harmonic distortion:	0-4 kHz		1.5		%	
	0-10 kHz		2.5		%	
	0-50 kHz		5.0		%	
	0-200 kHz		6.5	10	%	
Oscillator start-up time			<0.1	1	ms	

NOTE 2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition		Min.	Typ.	Max.	Units	Notes
Supply Voltage:	On-hook	1.8		5.7	V	For memory retention
	Off-hook	2.4		5.7	V	
Hookswitch input:	On-hook			$0.2V_{DD}$	V	
	Off-hook	$0.8V_{DD}$			V	
Oscillating frequency			560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}-V_{SS}	- 0.3 to + 6 5V
Voltage on any pin (except HSW)	V_{SS} - 0.3V to V_{DD} + 0 3V
Voltage on HSW pin (See note 1)	V_{SS} - 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	±1 mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	-5 to 0mA
Storage temperature	-55°C to + 125°C
Operating temperature range	-10°C to + 55°C

NOTES

1. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300µA max. no damage will occur.

2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

MA5883

20 MEMORY LD/DTMF SWITCHABLE DIALLER CHIP

The MA5883 is a keypad switchable LD/DTMF dialler device with Last Number Redial facility and 20, 24-digit memories, 10 accessible via dedicated keys.

Three operating modes are available: LD mode, with the ability to temporarily switch to DTMF mode from the keypad during a call, LD only mode and DTMF mode. The former mode enables users to access services such as home banking. Mixed LD and DTMF numbers can also be stored in memory.

The MA5883 is pin compatible with the MA5413, MA5453 and MA5473 LD/DTMF switchable diallers.

Metal mask and pin selectable options are available to service the specific technical requirements of particular countries and for customers preferred features and circuit configurations.

FEATURES

- Selectable Loop-Disconnect or DTMF dialling modes
- Keypad switchable LD to DTMF
- 24 digit Last Number Redial
- 20 x 24 digit Memories (10 dedicated keys)
- Selectable Break/Make Ratios 2:1 and 3:2
- Uses inexpensive 560 kHz ceramic resonator
- Battery-less operation: Low Power CMOS
- PIN (Personal Identification Number) confidentiality feature
- Timed Break Recall (Flash) and Earth Recall

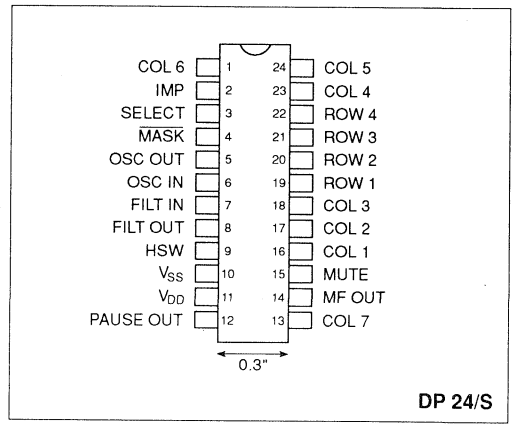


Figure 1. Pin connections - top view

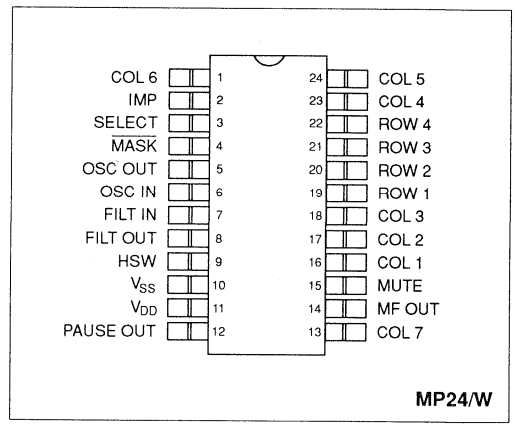


Figure 2. Pin connections - top view

PIN FUNCTIONS

Pin number (Figure 1)	Pin name	Function
2	IMP	'Loop disconnect' dialling output
3	SELECT	LD/DTMF selection, IDP and B/M ratio programming
4	$\overline{\text{MASK}}$	Output to disable speech circuit during pulse dialling and recall (see note 1)
5	OSC OUT	Connections for 560kHz ceramic resonator
6	OSC IN	
7	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
8	FILT OUT	
9	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-Hook'
10	V_{SS}	Negative supply
11	V_{DD}	Positive supply
12	PAUSE OUT	Active high output indicating a pause when dialling from memory
14	MF OUT	Unfiltered DTMF output
15	MUTE	Output active during keying and tone transmission (see note 2)
16	COL1	Connections for 28 key single contact keypad
17	COL2	
18	COL3	
23	COL4	
24	COL5	
1	COL6	
13	COL7	
19	ROW1	
20	ROW2	
21	ROW3	
22	ROW4	

Table 1. Pin functions

NOTES:
1. The $\overline{\text{MASK}}$ output may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook, during a TBR (Timed Flash) operation or for LD dialling.
2. The MUTE output is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

OPERATION

Power-On

When power is applied to the chip, a power-on reset circuit operates and ensures that the stores are cleared and all logic is reset. On power-up the dialling mode is set to LD until a key is pressed. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the stores may be corrupted, it will always, under all conditions, clear the stores when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA5883 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the on-hook state is not recognised for 200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied by the exchange, are ignored. In this case the $\overline{\text{MASK}}$ and IMP outputs will go low immediately the HSW input goes low in order to conserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted. This conserves supply current so that the memory contents may be retained.

Off-hook state

When the HSW input goes high, the $\overline{\text{MASK}}$ output immediately goes to the logic '1' level and remains there until dialling starts, a TBR (Flash) occurs or the HSW input goes low (see Figs 5 and 6). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A Key is accepted as valid when two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is 14ms (plus the oscillator start up time if it was not already running).

Simultaneous Key Depressions

If two keys are pressed simultaneously (i.e. a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Keypad Layout and Connections

	COL1	COL2	COL3	COL4	COL5	COL6	COL7
ROW1	1	2	3	TBR	S1	S2	S3
ROW2	4	5	6	REDIAL	S4	S5	S6
ROW3	7	8	9	STORE	S7	S8	S9
ROW4	*	0	#	PAUSE/ CONT		S0	LNR

Table 2.

* and # are used to change from LD to DTMF dialling and are available as digits when in DTMF mode.

TBR	Timed Break Recall (Flash)
LNR	Last Number Redial
STORE	Memory Programming
PAUSE/CONT	Insert pause in memory/continue dialling
S0 - S9	10 dedicated memory keys
REDIAL	For dialling the 10 memories not covered by dedicated keys. Can also be used for Last Number Redial.

Dialling Mode Selection

SELECT pin to:	Dialling mode	IDP (ms)	B/M Ratio
V_{SS}	LD + DTMF	800	2:1
COL1	LD + DTMF	500	2:1
COL2	LD + DTMF	500	3:2
COL3	LD + DTMF	800	3:2
COL4	LD ONLY	800	2:1
COL5	LD ONLY	500	2:1
COL6	LD ONLY	500	3:2
COL7	LD ONLY	800	3:2
V_{DD}	DTMF	-	-

Table 3. Dialling mode selection

The dialling mode may be selected via the SELECT pin (pin 3) as detailed in table 3. Four 'Loop-Disconnect + DTMF' options and four 'Loop-Disconnect only' options with different Inter-digit pauses and Make/Break ratios are available and one DTMF mode.

If one of the 'LD only" modes or the DTMF mode is selected, then dialling will remain fixed in LD mode or DTMF mode respectively. However, if one of the 'LD + DTMF' modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing the ★/# key provided that dialling is not in progress. If either of these keys are pressed during LD dialling they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

Last Number Redial

The function of the on-chip LNR store is to automatically retain a manually dialled number for redialling later. The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. To redial a number in the LNR store, either press the LNR key once or the REDIAL key twice.

The last number redial store has several features designed to assist the user:

Moving Cursor Facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the LNR key. In this case, the remainder of the number will be dialled when the LNR key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and is switched by the user (via the */# key) to DTMF mode, only the digits dialled in LD mode will be retained. This feature is provided to ensure security of PIN (Personal Identification Number) codes. Providing that the number of digits dialled in LD mode does not exceed 24, they will be retained regardless of the number of DTMF digits entered subsequently.

DTMF Calls

If a call contains the digits ★ or #, only those digits dialled prior to the first press of either ★ or # will be retained in the LNR store. This feature also ensures security for PIN codes whilst allowing exchange facility codes (for example) to be retained.

Memory Dialling

The MA5883 provides 20 memories, each of which has a capacity of 24 digits. There are 10 dedicated memory keys and a REDIAL key which allows the other 10 memories to be dialled. The memories can store pauses and digits to be dialled in LD, DTMF or mixed modes.

Programming Memories

The MA5883 must be "off-hook" and idle:

1. Press the STORE key.
2. Press key S0-S9 or REDIAL + digit 0-9 indicating the memory to be programmed.
3. Enter digits to be stored (no digits will be dialled whilst programming).
4. To finish programming the memory either press the STORE key again or go "on-hook".
5. Repeat to programme other memories.

If more than 24 digits are entered while programming a memory, then the memory will be cleared until re-programmed. If any "non-valid" keys are pressed during programming (e.g. LNR, TBR) they will be ignored.

Mixed Mode Numbers and Pauses in Memory

Mixed mode (i.e. LD + DTMF numbers are easily programmed into memory. The SELECT pin must be set to one of the 'LD + DTMF' modes (as it would be when dialling a mixed mode number), then the store is programmed using the same procedure as above. The first press of */# will be stored as a 'change to DTMF' and this will cause all subsequent digits to be sent in DTMF when redialling from memory.

Similarly pauses can be stored in memory by pressing the PAUSE key in the appropriate position when programming.

When redialling from memory, both pauses and LD to DTMF changeovers will cause dialling to halt temporarily until the user presses either the PAUSE/CONT key or the REDIAL key. The exception to this rule is when an LD to DTMF changeover is stored in the first memory location: In this case, DTMF dialling will occur immediately when memory dialling is invoked - this allows DTMF codes to be easily stored and sent, even in a telephone where the normal dialling mode is LD.

It should be noted that a pause or an LD to DTMF changeover each require one memory location.

Dialling from Memories

The MA5883 must be "off-hook" and idle:

1. Press the appropriate memory key S0-S9 or REDIAL + digit 0-9. Dialling will now start.

2. If dialling halts due to a pause or an LD to DTMF changeover in the memory, the PAUSE OUT pin will go high (logic '1'). Further dialling can be resumed either by pressing the PAUSE/CONT key, or, alternatively the COLUMN 4 pin can be pulled low (for a minimum of 14ms) to achieve the same result, thus allowing an external timer circuit to be used. The PAUSE OUT output is reset when dialling resumes.

All Keypad positions are disabled whilst memory dialling is in progress.

Timed Break & Earth Loop Recall (Flash)

The MA5883 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation, the dialling mode selected via the SELECT pin will be restored. Also, only the digits dialled after the ELR/TBR operation will be retained in the LNR store.

A TBR (Flash) of 100ms(1) is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the COLUMN 3 pin. If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in figure 3, or by use of a double contact switch.

Grounding COLUMN 3 will not directly affect the chip outputs. However, in order to prevent misoperation, the HSW timeout will be disabled during ELR. This is so that the MA5883 cannot go into the on-hook state if the HSW input goes low as a result of ELR signalling (i.e. whilst the telephone is, in reality, still Off-hook). The $\overline{\text{MASK}}$ and IMP outputs will respond as normal to the status of the HSW input.

(1)Other TBR (Flash) periods are available as mask options (see page 7).

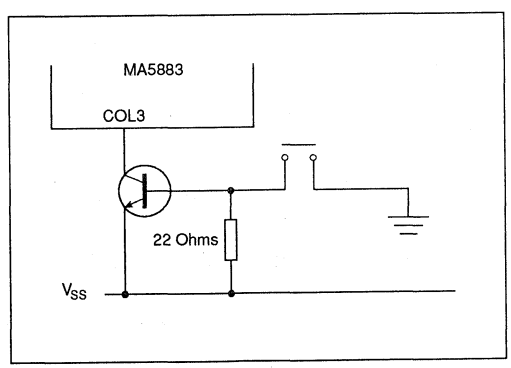


Figure 3. Earth loop recall

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 7 & 8) for use in a low pass active filter.

Figure 4, below, shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

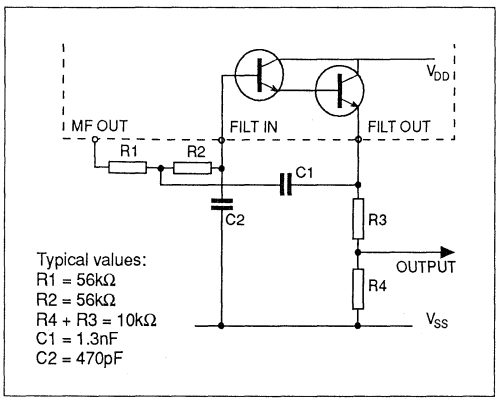


Figure 4. DTMF tone filtering

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the 'single pin' type. Internally, the OSC IN pin is connected to Vss and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

DTMF Dialling

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission. The IMP output remains low during tone transmission. The MF OUT output rises to its d.c. level of 0.9 Vdd at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate. Dialling from the LNR store occurs at the maximum rate.

If a key is held down for longer than 100ms, the tone output will continue until the key is released.

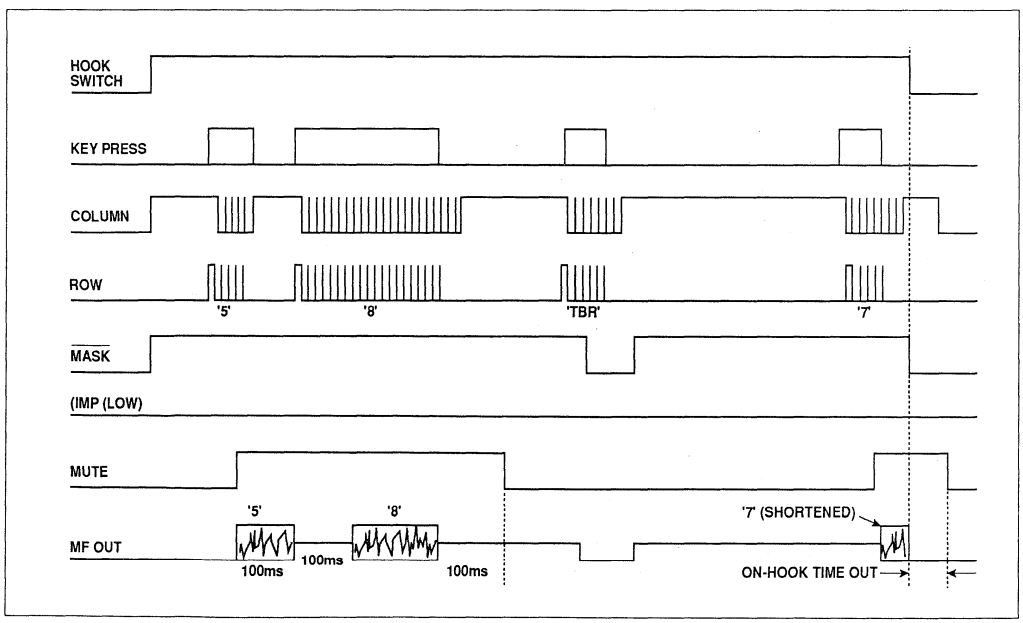


Figure 5. DTMF mode timing diagram

DTMF Dialling - Tone Frequencies

Keypad	R1	R2	R3	R4	C1	C2	C3
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477
Deviation from nominal (%)	-0.07	-0.10	+0.19	-0.15	-0.17	-0.20	-0.22

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 4 Tone frequencies

Loop-Disconnect Dialling

The $\overline{\text{MASK}}$ output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic '0' during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD Dialling. LD Dialling is signalled on the IMP output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

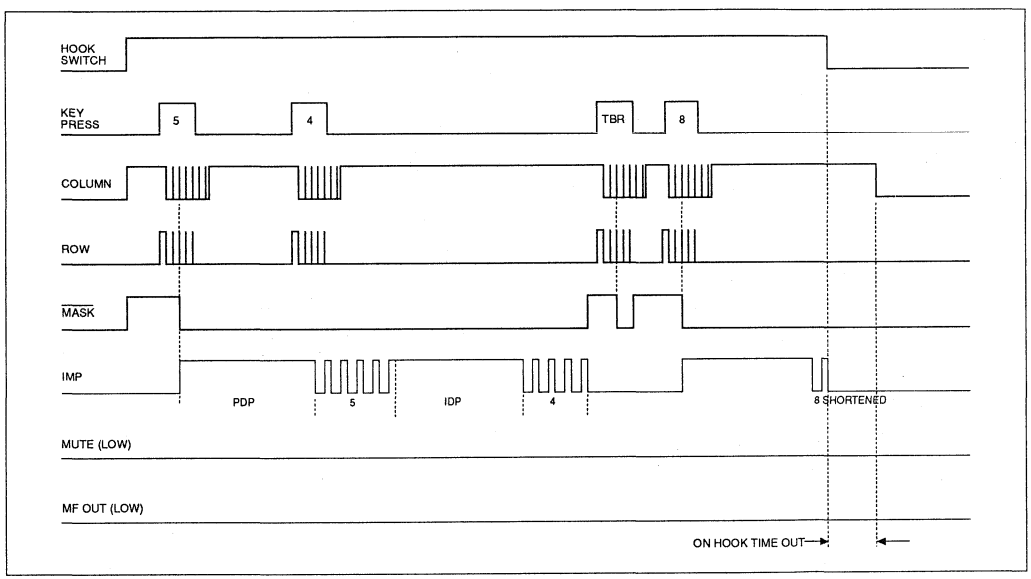


Figure 6. LD dialling

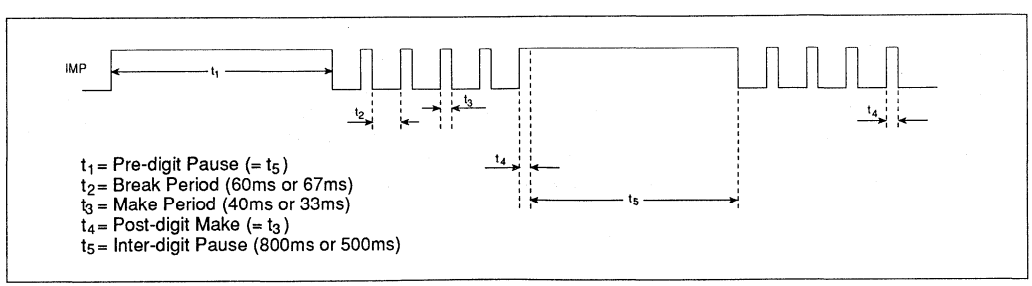


Figure 7. Timing data

Mask Options

The MA5883 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufacture. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit.

The options, listed below, are possible in any combination. Standard options are listed first in italics at 'a'. Other options may be produced by arrangement.

1. TBR (Flash) Period:

a.*100ms*
b.200ms
c.300ms
d.400ms
e.500ms
f.600ms

2. LD to DTMF Keypad switching:

a.* *and # keys*
b.* key
c. No keypad switching

3. Retention of post- */# digits in LNR store (DTMF mode)

a.*Digits before * or # retained.*
b.Digits before * or # retained (except when * or # is first digit).
c.All digits retained.

4. LD dialling options

a.*Standard (n = n pulses, when 0 = 10)*
b.Swedish (n = n + 1 pulses)
c.Norwegian (n = (11-n) pulses)
d.New Zealand (n = (10-n) pulses)

5. Recall (Flash) / LNR Protocol:

a.*Digits after recall retained in LNR store*
b.Digits before recall retained in LNR store
c.Recall inhibits LNR
d. For Danish PABX requirements

6. DTMF Minimum Timings:

a.*100ms on, 100ms off*
b.73.3ms on 73.3ms off
c.73.3ms on, 146.7ms off

7. Pin 4:

a.*$\overline{MASK}$*
b.MASK

8. Pin 2:

a.*IMP*
b.$\overline{IMP}$
c.[IMP + $\overline{MASK}$]

d.[IMP + $\overline{MASK}$]

9. Pin 15:

a.MUTE
b.$\overline{MUTE}$

ABSOLUTE MAXIMUM RATINGS

Parameter	Min.	Typ.	Max.	Units	Notes
Supply voltage V_{DD}-V_{SS}	-0.3	-	6.5	V	-
Voltage on any pin (except HSW)	V_{SS} -0.3	-	V_{DD} +0.3	V	-
Voltage on pin HSW	V_{SS} -0.3	-	-	V	See note 1 below
Current at any pin (except HSW, FILTOUT and FILTIN)	-1	-	1	mA	-
Current at pin FILTOUT	0	-	0.1	mA	-
Current at pin FILTIN	-5	-	0	mA	-
Operating temperature	-25	-	70	°C	-
Storage temperature	-55	-	125	°C	-

Table 5. Absolute maximum ratings.

NOTE 1: A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300µA max. no damage will occur.
NOTE 2: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to this device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
NOTE 3: These temperature ranges do not apply to all package types. Many package types are available and these may have limited temperature ranges. Further information is available on request.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Condition		Min.	Typ.	Max.	Units	Notes
Supply voltage:	On-hook	1.8	-	5.7	V	For memory retention
	Off-hook	2.4	-	5.7	V	
Hookswitch input:	On-hook	-	-	0.2 V_{DD}	-	-
	Off-hook	0.8 V_{DD}	-	-	-	

Table 6. Recommended DC operating conditions.

Parameter		Min.	Typ.	Max.	Units	Notes
Supply current:	On-hook	-	<0.1	5	µA	at V_{DD} = 2.0
	Off-hook	-	1.5		µA	True only if MF OUT is low
	MF tone sending	-		1.0	mA	-
	LD impulsing	-		200	µA	-
Output high voltage ($\overline{MASK}$, MUTE, IMP, PAUSE Outputs)		2.2	-		V	I = -1mA
Output low voltage ($\overline{MASK}$, MUTE, IMP, PAUSE Outputs)		-	-	0.3	V	I = +1mA
MF OUT d.c. level during tone sending			0.9V_{DD}	-	V	-
MF OUT output resistance		-	3	5	kΩ	-
'Key Pressed' resistance		-	-	2	kΩ	2.5V<V_{DD}<5.7V
'Key Not Pressed' resistance		500	-	-	kΩ	2.5V<V_{DD}<5.7V
Darlington pair current gain		600	50,000	-	-	I_e = 100µA, V_{ce} = 2V

Table 7. DC characteristics

NOTE: 1. V_{DD} = 2.5V at 25°C unless specified.

AC OPERATING CONDITIONS AND CHARACTERISTICS

Condition	Min.	Typ.	Max.	Units	Notes
Oscillating frequency	-	560	-	kHz	-

Table 8. Recommended AC operating conditions.

Condition		Min.	Typ.	Max.	Units	Notes
Tone output:	Low group	57	64	-	mV r.m.s.	No load
	High group		81	91	mV r.m.s.	No load
High-to-low group amplitude ratio (pre-emphasis)		1.5	2	2.5	dB	See note 2
Total harmonic distortion:	0 - 4 kHz	-	1.5	-	%	-
	0 - 10 kHz	-	2.5	-	%	-
	0 - 50 kHz	-	5.0	-	%	-
	0 - 200 kHz	-	6.5	10	%	-
Oscillator start up time		-	<0.1	1	ms	-

Table 9. AC characteristics.

NOTE 1: V_{DD} = 2.5V.
NOTE 2: Typical value varies slightly dependant upon particular tone pair.

MA589 FAMILY

LD/DTMF SWITCHABLE DIALLERS WITH DEDICATED KEYS FOR 20 MEMORIES

The MA589 family are keypad switchable LD/DTMF dialler devices with a last number redial facility and twenty 24-digit memories, each with its own dedicated dialling key.

Three operating modes are available: LD only mode, DTMF only mode and LD mode with the ability to switch temporarily to DTMF mode from the keypad during a call. This last mode enables subscribers to access such services as home banking Mixed LD and DTMF numbers can also be stored in memory.

The-MA589 devices are pin compatible with the GPS switchable dialler families MA526, MA527, MA541, MA545 MA547, MA585 and MA587 - providing a complete range of telephone features within a single PCB and circuit design. Metal mask and pin selectable options are available to service specific requirements of particular countries and customers.

FEATURES

- Selectable Loop-Disconnect or DTMF Modes
- Keypad Switchable LD to DTMF
- 20 X24-Digit Memories, each with Dedicated Key
- 24 Digit Last Number Redial
- Selectable Make/Break Ratios 2:1 and 3:2
- Uses Inexpensive 560kHz Ceramic Resonator
- Battery-less operation - Low Power CMOS
- Mask Programmable Options to suit Application
- Timed Break Recall (Flash) and Earth Recall

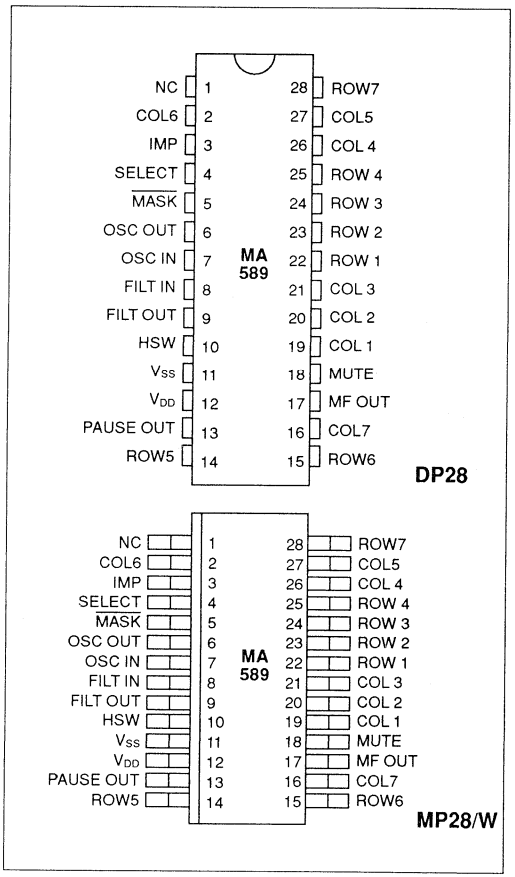


Figure 1: Pin connections - top view. (not to scale)

PIN FUNCTIONS

Pin number	Pin name	Function
1	NC	Not connected
3	IMP	'Loop disconnect' dialling output
4	SELECT	LD/DTMF selection, IDP and B/M radio programming
5	MASK	Output to disable speech circuit during pulse dialling and recall (see note 1)
6	OSC OUT	Connections for 560kHz ceramic resonator
7	OSC IN	
8	FILT IN	Unity gain amplifier input and output for DTMF tone filtering
9	FILT OUT	
10	HSW	Hookswitch input - a logic 1 at this pin is used to indicate 'Off-hook'
11	V_{SS}	Negative supply
12	V_{DD}	Positive supply
13	PAUSE OUT	Active high output indicating a pause when dialling from memory
17	MF OUT	Unfiltered DTMF output
18	MUTE	Output active during keying and tone transmission (see note 2)
19	COL1	Connections for 38 key single contact keypad
20	COL2	
21	COL3	
26	COL4	
27	COL5	
2	COL6	
16	COL7	
22	ROW1	
23	ROW2	
24	ROW3	
25	ROW4	
14	ROW5	
15	ROW6	
28	ROW7	

1. $\overline{\text{MASK}}$ may be used to disconnect the whole speech circuit in order to maintain the break condition whilst on-hook and during a TBR (Timed Flash) operation.
2. MUTE is provided to disable the microphone while maintaining the loop condition during DTMF transmission.

Table 1: Pin functions

OPERATION

Power-on

When power is applied to the chip, a power-on reset circuit operates and ensures that the last number redial store is cleared and all logic is reset. The power-on reset circuit is designed such that if the chip supply voltage drops to a level at which the LNR store may be corrupted, it will always, under all conditions, clear the store when power is restored, so that corrupt data is not retained.

Hookswitch Operation

The HSW input is used to inform the MA589 of whether the telephone is on or off hook. Logic '0' is recognised as on-hook, Logic '1' is recognised as off-hook. When the HSW input rises from '0' to '1' the off-hook state is recognised immediately and keypad inputs are accepted. However, when the HSW input falls from '1' to '0' the onhook state is not recognised for 200-300ms. This is so that short line breaks of less than 200ms, such as line reversals applied by the exchange, are ignored. In this case the IMP and $\overline{\text{MASK}}$ outputs will go low immediately the HSW input goes low in order to preserve current, but will resume normal operation immediately HSW goes high.

On-hook state

In the on-hook state all chip outputs are set low, the oscillator circuit is inhibited and no key inputs are accepted. This conserves supply current so that the LNR store contents may be retained.

Off-hook state

When the HSW input goes high, the MASK output immediately goes to the logic '1' level and remains there until going on-hook or signalling a TBR, (see timing diagram). COLUMN outputs also go high until a key is pressed. The oscillator circuit remains inactive until a key is pressed, and is normally off whenever timing functions are not required.

Keypad Operation

A single contact, normally open keypad is required. When off-hook the COLUMN outputs are normally held high and the ROW inputs are low. When a key is pressed this connects a COLUMN output to a ROW input and the ROW input is pulled high.

This action initiates keyboard scanning. During keyboard scanning, the COLUMN outputs are normally low but generate scanning pulses at 7ms intervals on each output in sequence. A key is accepted as valid when, two successive scanning pulses from the same COLUMN are seen on a ROW input. Hence, the minimum bounce-free key closure period which is necessary to guarantee detection is about 14ms (plus the oscillator start-up time if it was not already running).

Simultaneous key depressions

If two keys are pressed simultaneously (i.e a second key is pressed before the first has been verified) neither key will be accepted until both keys are released and the correct key is pressed again.

Dialling Mode Selection

The dialling mode may be selected via the SELECT pin (pin 4) as detailed in Table 2 Four 'LoopDisconnect + DTMF options and lour 'Loop-Disconnect only' options with different Interdigit pauses and Break/Make ratios are available and one DTMF mode If one of the 'LD only' modes or the DTMF mode is selected then dialling will remain fixed in LD mode or DTMF mode respectively .

	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7
ROW 1	1	2	3	TBR	S1	S2	S3
ROW 2	4	5	6	REDIAL	S4	S5	S6
ROW 3	7	8	9	STORE	S7	S8	S9
ROW 4	*	0	#	PAUSE/ CONT	SHIFT	S00	LNR
ROW 5					S11	S12	S13
ROW 6				S10	S14	S15	S16
ROW 7					S17	S18	S19

Figure 2a: Versions without TONE key

* or */# are used to change from LD to DTMF dialling and are available as digits when in DTMF mode

TBR: Timed Break Recall (Flash)
STORE: Memory Programming key. Use in conjunction with dedicated memory keys or a two-digit code representing the number of the memory to be programmed.
S00 - S19: 'Single-touch' dedicated memory dialling keys
LNR: Last Number Redial
REDIAL and SHIFT: These keys are clearly unnecessary where keypad positions are provided for all the dedicated memory keys but may be useful to access memories in applications where the telephone provides insufficient keys for all these functions. For a description of the function of the REDIAL and SHIFT keys, see the MA585 and MA587 datasheets, respectively. Do not fit keys in these positions if not required.
PAUSE/CONT: Insert pause in memory/continue dialling
TONE: Change dialling mode from LD to DTMF

	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7
ROW 1	1	2	3	TBR	S1	S2	S3
ROW 2	4	5	6	REDIAL	S4	S5	S6
ROW 3	7	8	9	STORE	S7	S8	S9
ROW 4	*	0	#	TONE	SHIFT	S00	LNR
ROW 5					S11	S12	S13
ROW 6				S10	S14	S15	S16
ROW 7					S17	S18	S19

Figure 2b: Versions with TONE key

Figure 2: Keypad layout and connections

However, if one of the 'LD + DTMF~ modes is selected, the chip will be in LD mode initially in the off-hook condition but may be switched to DTMF by pressing either the *, */# or TONE key (depending on the mask variant - see Fig 2 and page I-65), provided that dialling is not in progress If any of these keys are pressed during LD dialling, they will be ignored.

Only if * or # are pressed subsequent to switching to DTMF, will * or # be dialled. Only digits entered prior to a switch to DTMF will subsequently be available for redialling (see Last Number Redial operation).

Once switched to DTMF, dialling will remain in this mode until either a Recall (Flash) operation or until the chip returns to the on-hook state.

SELECT pin to	Dialling mode	IDP (ms)	B/M ratio
V_{SS}	LD + DTMF	800	2:1
COL 1	LD + DTMF	500	2:1
COL 2	LD + DTMF	500	3:2
COL 3	LD + DTMF	800	3:2
COL 4	LD only	800	2:1
COL 5	LD only	500	2:1
COL 6	LD only	500	3:2
COL 7	LD only	800	3:2
V_{DD}	DTMF	-	-

Table 2: Dialling mode selection

Last Number Redial (LNR)

The function of the on-chip LNR store is to retain automatically a manually dialled number for redialling later. The capacity of the store is 24 digits. If a number is dialled which is longer than this, redialling will not be allowed with this number. To redial a number in the LNR store, the LNR key must be pressed once.

The last number redial store has several features designed to assist the user:

Moving cursor facility

This allows a user to enter the first digit or digits of the number in the last number redial store manually before pressing the LNR key; the remainder of the number will be dialled when the LNR key is pressed.

If the digit(s) dialled manually do not match those in the LNR store, then redialling will be inhibited for the remainder of the call, and the numbers entered will be saved in the LNR store for redialling in a subsequent call.

If the user manually dials the first digit(s) in the LNR store, and then goes on-hook, the whole contents of the store will be retained.

This facility is provided to aid use in PABX applications, where the user must first dial an access digit, or digits, and then wait for a second dial tone before continuing dialling.

Mixed Mode Calls

In the case of a call which starts in LD mode and is switched by the user (via the *, */#, or TONE key) to DTMF mode, only the digits dialled in LD mode will be retained. This feature is provided to ensure security of PIN (Personal Identification Number) codes. Provided that the number of digits dialled in LD mode does not exceed 24, they will be retained regardless of the number of DTMF digits entered subsequently.

Memory Dialling

The MA589 provides 20 memories, each of which has a capacity of 24 digits and each of which has its own dedicated key. The memories can store digits to be dialled in LD, DTMF or mixed modes and also pauses.

Programming Memories

The MA589 must be 'off-hook' and idle:

1. Press the STORE key.
2. Press the key (S00-S19) of the memory to be programmed .
3. Enter digits to be stored (no digits will be dialled whilst programming)
4. To finish programming the memory either press the STORE key again or go 'on-hook'.
5. Repeat to programme other memories.

If more than 24 digits are entered while programming a memory, then the memory will be cleared until reprogrammed. If any non-valid keys are pressed during programming (e g. LNR,TBR) they will be ignored.

Mixed mode numbers and pauses in memory

Mixed mode (ie LD + DTMF) numbers are easily programmed into memory. The SELECT pin should be set to one of the 'LD + DTMF' modes (as it would be when dialling a mixed mode number), then the number entered using the same procedure as if dialling normally. The first press of *, */# or TONE (according to the mask variant) will be stored as a 'change to DTMF', and this will cause all subsequent digits to be sent in DTMF when redialling from memory .

Similarly, pauses can be stored in memory by pressing the PAUSE key in the appropriate position when programming.

When redialling from memory, both pauses and LD to DTMF changeovers will cause dialling to halt temporarily until the user presses the PAUSE/CONT key. The exception to this rule is when an LD to DTMF changeover is stored in the first memory location: in this case, DTMF dialling will occur immediately when memory dialling is invoked - this allows DTMF codes to be easily stored and sent even in a telephone where the normal dialling mode is LD.

It should be noted that a pause or an LD to DTMF changeover each require one memory location.

Dialling from memories

The MA589 must be 'off-hook' and idle:

1. Press the appropriate dedicated memory key (S00-S19). Dialling will now start.
2. If dialling halts due to a pause or an LD to DTMF changeover in the memory, the PAUSE OUT pin will go high (logic '1').
   Further dialling can be resumed either by pressing the PAUSE/CONT key or, alternatively, the Column 4 pin can be pulled low (for a minimum of 14 ms) to achieve the same result, thus allowing an external timer circuit to be used. The PAUSE/OUT output is reset when dialling resumes.

   All keypad positions are disabled whilst memory dialling is in progress.

Timed Break & Earth Loop Recall (Flash)

The MA589 supports both TBR and ELR and offers a common operating protocol in both cases.

After a recall (Flash) operation the dialling mode selected via the SELECT pin will be restored. Also, only the digits dialled after the ELR/TBR operation will be retained in the LNR store [1].

A TBR (Flash) of 100ms [2] is generated when the TBR key is pressed. The $\overline{\text{MASK}}$ output goes low in order to produce the line break. When in DTMF mode, the MF OUT output also goes low for the duration of the break.

ELR is supported via the column 3 pin. If this pin is connected to ground for a minimum of 20ms during an ELR operation, the chip will offer the same operating protocol as for TBR.

This may be achieved by use of the circuit shown below in Fig 3, or by use of a double contact switch.

[1] Other options are available including an option for Danish rrquirements (see page 1-65). In Denmark TBR (or ELR) is used to obtain an outside line in PABX use. Under these conditions the LNR store contents will be retained and can be redialled after a TBR or ELR. Digits manually entered atter a TBR or ELR will become the new LNR store contents.

[2] Other TBR (Flash) periods are available as mask options (see page 1-65).

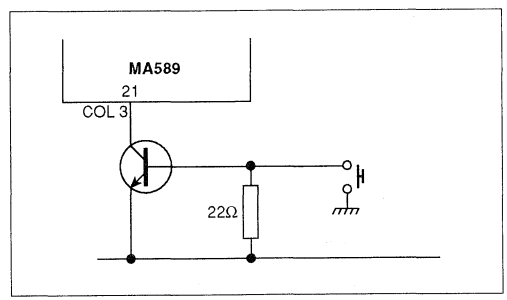


Figure 3: Earth loop recall

Oscillator Circuit

This requires an external 560kHz ceramic resonator connected between OSC IN and OSC OUT to provide a timing reference for all chip functions. No other components are required or should be used.

The oscillator circuit is of the 'single pin' type. Internally. the OSC IN pin is connected to V_{SS} and therefore the resonator may alternatively be connected externally between OSC OUT and V_{SS} if desired.

Please consult your resonator supplier who will recommend a suitable resonator type.

Tone Filtering

The spectral purity of the DTMF output is sufficient for most applications. However, where lower distortion DTMF tones are required, an on-chip darlington pair is provided (accessible via pins 7 & 8) for use in a low pass active filter.

Fig. 4 shows how a 2-pole Sallen and Key filter can be implemented. The typical component values have been chosen to give a second order Butterworth response with a cut-off frequency of about 3.5kHz and a nominal pass-band insertion loss of 0.5dB.

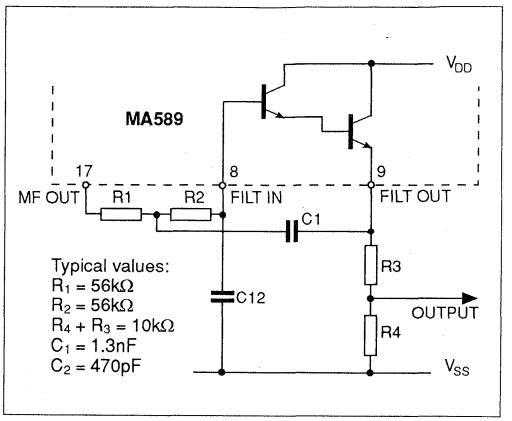


Figure 4: DTMF tone filtering

DTMF DIALLING

During DTMF dialling the MUTE output goes to logic ' 1 ' and remains there for the duration of the tone transmission .

The IMP output remains low during tone transmission. The MF OUT output rises to its DC level of 0 9 VDD at the start of the tone transmission and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

The maximum rate at which tones are sent to line is 100ms on, followed by 100ms off. If keys are activated faster than this they are placed in a temporary store and then sent to line at the maximum rate. Dialling from the LNR store occurs at the maximum rate.

If a key is held down for longer than 100ms, the tone output will continue until the key is released.

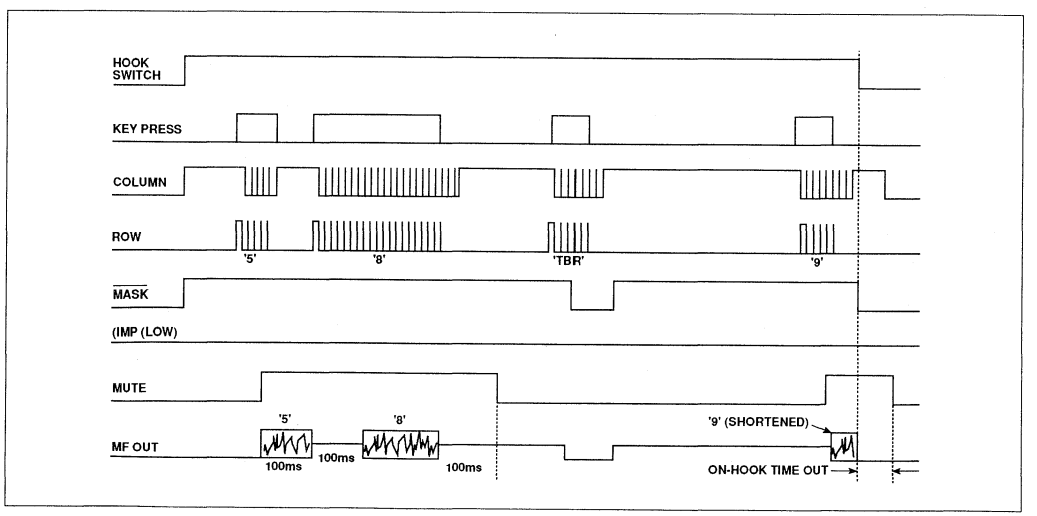


Figure 5: DTMF mode timing diagram

Keypad	R1	R2	R3	R4	C1	C2	C3	C4
Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	-0.07	-0.10	+0.19	-0.15	-0.17	-0.20	-0.22	-0.31

NOTE: There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 3: Tone frequencies

LOOP-DISCONNECT DIALLING

The MASK output is provided in order to disable the speech circuit during LD dialling. Consequently, the $\overline{\text{MASK}}$ output is normally at logic '1' in the off-hook condition, but changes to logic '0' during LD dialling. $\overline{\text{MASK}}$ also changes to logic '0' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and MF OUT remain low during LD dialling. LD dialling is signalled on the IMP output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the IMP output sits at logic '0'.

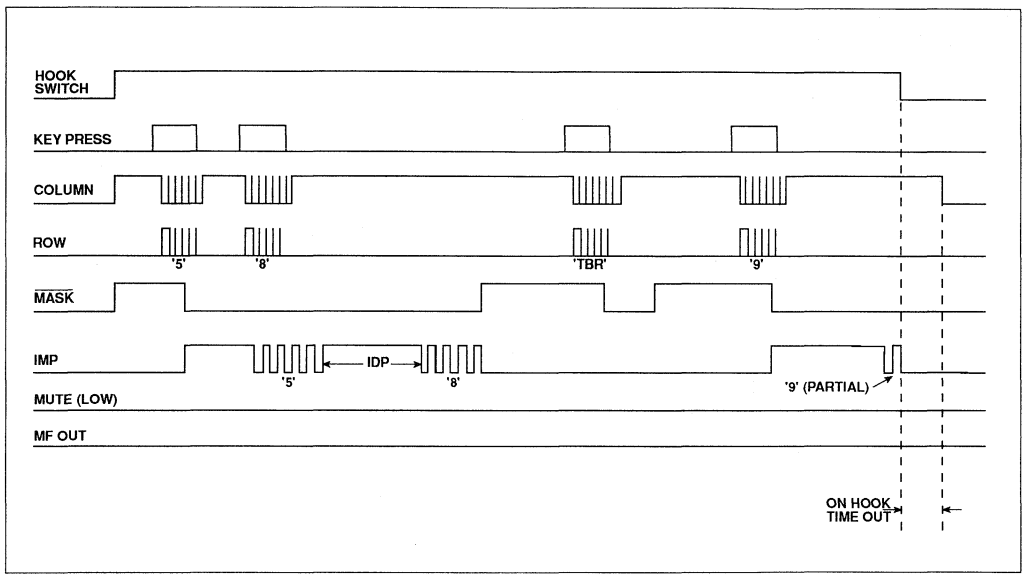


Figure 6: LD mode timing diagram

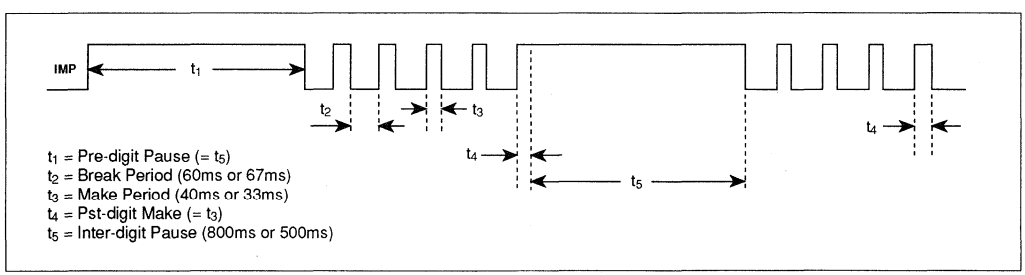


Figure 7: Timing data

MASK OPTIONS

The MA589 has been designed so that many features can be altered quickly and inexpensively at the final stage of manufactute. These options allow the telephone manufacturer to cater for different market requirements throughout the world without changing the telephone circuit. The options, listed below, are possible in any combination. Standard options are listed first in bold italics at 'a.' Other options may be produced by arrangement.

1. TBR (Flash) Period
a. 100 ms
b. 200 ms
c. 300 ms
d. 400 ms
e. 500 ms
f. 600 ms

2. LD to DTMF Keypad Switching
a. *and ,# keys
b. TONE key
c, * key

3. Retention of Post - */# Digits in LNR Store (DTMF mode)
a. All digits retained
b. Digits before * or # retained
c. Digits before * and # retained (except when * or # is first digit

4. LD dialling options
a. Standard (n = N pulses, except 0 = 10 pulses)
b. Swedish (n = (n + 1) pulses)
c. Norwegian (n = (11 - n) pulses)
d. New Zealand (n = (10 - n) pulses)

5. Recall (Flash) / LNR Protocol
a. Digits dialled after Recall retained
b. Digits dialled before Recall retained
c. Recall inhibits LNR
d. For Danish PABX requirements

6. DTMF Minimum Timings
a. 100ms on, 100ms off
b. 73ms on, 73ms off
c. 73ms on, 147ms off

7. Pin 5
a. $\overline{MASK}$
b. MASK

8. Pin 3
a. IMP
b. $\overline{IMP}$
c. [IMP + $\overline{MASK}$]
d. [$\overline{IMP}$ + MASK]

9. Pin 18
a. MUTE
b. $\overline{MUTE}$

APPLICATION CIRCUITS

Refer to the MA541 data sheet, Figs. 8 and 9, on pages 1-29 and 1-30

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{DD} = 2.5V T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Supply current:	On-hook		<1	5.0	µA	V_{DD} = 2.0V. See note 1.
	Off-hook		1.5		µA	MF OUT low
	MFtone sending			1.0	mA	
	LD impulsing			200	µA	
Output high voltage ($\overline{MASK}$ and MUTE and IMP outputs)		2.2			V	I = -1mA
Output low voltage ($\overline{MASK}$ and MUTE and IMP outputs)				0.3	V	I = +1mA
MF OUT DC level during tone sending			$0.9V_{DD}$		V	
MF OUT output resistance			3		kΩ	
'Key Pressed' resistance				2	kΩ	2.5V < V_{DD} < 5.7V
'Key Not Pressed' resistance		500			kΩ	2.5V < V_{DD} < 5.7V
Darlington pair current gain (see fig 4)		600	50,000			I_E = 100µA, V_{CE} = 2V

NOTE 1. Specially tested versions with guaranteed lower on-hook supply current are available.

AC CHARACTERISTICS

Characteristic		Min.	Typ.	Max.	Units	Condition
Tone output:	low group	57	64		mV rms	No load.
	high group		81	91	mV rms	No load.
High-to-Low group amplitude ratio (pre emphasis)		1.5	2	2.5	dB	See note 2
Total harmonic distortion:	0-4 kHz		1.5		%	
	0-10 kHz		2.5		%	
	0-50 kHz		5.0		%	
	0-200 kHz		6.5	10	%	
Oscillator start-up time			<0.1	1	ms	

NOTE 2. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING CONDITIONS

Condition		Min.	Typ.	Max.	Units	Notes
Supply Voltage:	On-hook	1.8		5.7	V	For memory retention
	Off-hook	2.4		5.7	V	
Hookswitch input:	On-hook			$0.2V_{DD}$	V	
	Off-hook	$0.8V_{DD}$			V	
Oscillating frequency			560		kHz	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}-V_{SS}	- 0.3 to + 6 5V
Voltage on any pin (except HSW)	V_{SS} - 0.3V to V_{DD} + 0 3V
Voltage on HSW pin (See note 1)	V_{SS} - 0.3V min.
Current at any I/O pin (except HSW, FILTOUT and FILTIN)	±1 mA
Current at FILTOUT pin	0 to 0.1mA
Current at FILTIN pin	-5 to 0mA
Storage temperature	-55°C to + 125°C
Operating temperature range	-10°C to + 55°C

NOTES

1. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300µA max. no damage will occur.

2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

MA525

MICROPROCESSOR CONTROLLED LD/DTMF DIALLER

The MA525 is a microprocessor controlled Loop Disconnect (LD) and Dual Tone Multi-Frequency (DTMF) dialler device with a last number redial facility.

The MA525 is directly controlled via a MOTEL™ interface which automatically adapts to either Motorola or Intel format, thereby allowing interfacing to most common microprocessors and microcontrollers. The bus design allows both 4 and 8-bit bus systems to be used and the device is designed to allow the bus to be shared with other peripheral devices.

All dialling conditions and timings are programmable via on-chip registers in order to allow the device to meet the specifications of virtually any telephone network with one standard product. Blocks of up to 21 digits at a time (including TBR and Pause) can be loaded for dialling. The device will retain the last number dialled for redialling if required.

Dialling and associated control signals are generated by the device in both LD and DTMF modes using a low-cost 560kHz ceramic resonator as an accurate timing reference.The A,B,C,D tone pairs are available in DTMF mode. In addition, a 'single tone' output is provided.

The MA525 can be operated in either 'Phone' or 'Modem' mode, generating appropriate control signals for the application.

The polarity of all output signals may be inverted, making the MA525 suitable for use with virtually any line interfacing technique.

A chip select (CS) input is also provided, allowing the MA525 to share a common microprocessor bus with other microprocessor peripherals.

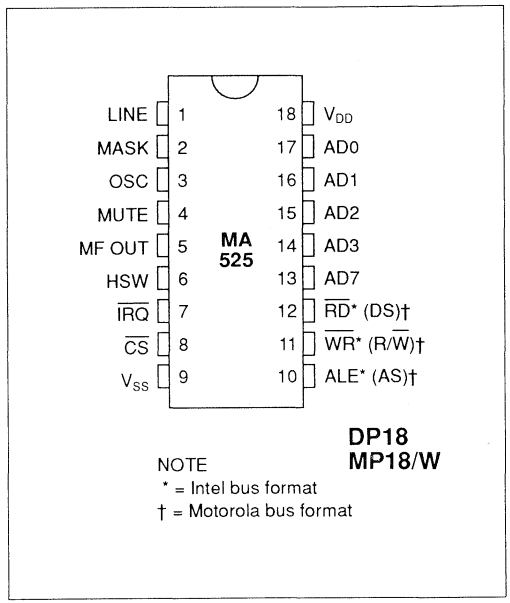


Figure 1: Pin connections - top view

APPLICATIONS

- Feature Telephones
- Auto-Dialling Modems
- Auto-Dialling Telephones
- Pay Phones
- Security Products
- Cordless Telephone Base Stations
- Banking Facilities

FEATURES

- MOTEL™ Microprocessor Interface for Direct Connection to Motorola or Intel Derived Buses
- Loop-Disconnect and DTMF dialling.
- Modem and Phone Modes.
- Last Number Redial Facility.
- All Timing Parameters Programmable to meet International Signalling Requirements
- Reloadable 21-digit Store Including Access Pause and Timed Break Recall (Flash).
- Reliable Power-on Reset.
- Uses a Low-cost 560kHz Ceramic Resonator

PIN FUNCTIONS

Pin no.	Name	Type	Function
1	LINE	O	Dialling pulse output and modem line control.
2	MASK	O	Output to disable speech circuit during LD dialling and TBR.
3	OSC	I/O	Connection for 560kHz ceramic resonator.
4	MUTE	O	Output to inhibit microphone during DTMF dialling. In Modem mode it can be used to switch DTMF tones or the modem to the line
5	MF OUT	O	DTMF tone output.
6	HSW	I	Hookswitch sense input. '1' = Off-hook. No direct control for modem use but status still available.
7	$\overline{IRQ}$	O	Interrupt request. N-channel open-drain output.
8	$\overline{CS}$	I	Chip select input. Used to activate MOTEL interface.
9	V_{SS}	SUPPLY	Negative supply
10	AS ALE	I	Motorola Mode: Address Strobe Intel Mode: Address Latch Enable
11	R/$\overline{W}$ $\overline{WR}$	I	Motorola Mode: Read/Write Intel Mode: Write Strobe
12	DS RD	I	Motorola Mode: Data Strobe Intel Mode: Read Strobe
13	AD7	I/O	Available for servicing interrupt request
14	AD3	I/O	Multiplexed address/data bi-directional bus. MSB.
15	AD2	I/O	Multiplexed address/data bi-directional bus.
16	AD1	I/O	Multiplexed address/data bi-directional bus.
17	AD0	I/O	Multiplexed address/data bi-directional bus. LSB.
18	V_{DD}	SUPPLY	Positive supply.

Table 1: Pin functions

MICROPROCESSOR INTERFACE

The MA525 interfaces to the controlling microprocessor by means of a multiplexed bus of the MOTEL format. This interface bus has the ability to adapt itself automatically to the format and timing of both MOTorola and IntEL interface busses (hence MOTEL). Internally, the detection circuitry latches the status of the DS/$\overline{RD}$ line when AS/ALE goes high. If the result is high, then the Intel mode is used; if the result is low then the Motorola mode is used. This procedure is carried out each time that AS/ALE goes high. Note that the MA525 defaults to Intel mode on power up and is reconfigured to the relevant mode after the first DS/ALE positive going edge.

In practice the MOTEL interface is transparent to the user. For bus connection and timing information simply refer to the description relevant to the particular microprocessor/ microcontroller used.

Industry standard microprocessors such as the 8085,8088 etc and microcontrollers such as the 8051 or 6805 are all compatible with the interface on the MA525. It is also possible to drive the microprocessor interface pins on the MA525 directly using port pins .

It should be noted that all bus timings are derived from the microprocessor and are independent of the MA525 clock input.

Registers 0 to 9 are write only whereas Register 10 is a read-only Status Register. An interrupt pin is provided ($\overline{IRQ}$) to speed microprocessor interfacing. This may be disabled at any point if necessary. In addition, an Interrupt Request Flag Register 10 operates in exactly the same way as the $\overline{IRQ}$ pin (but is active high).

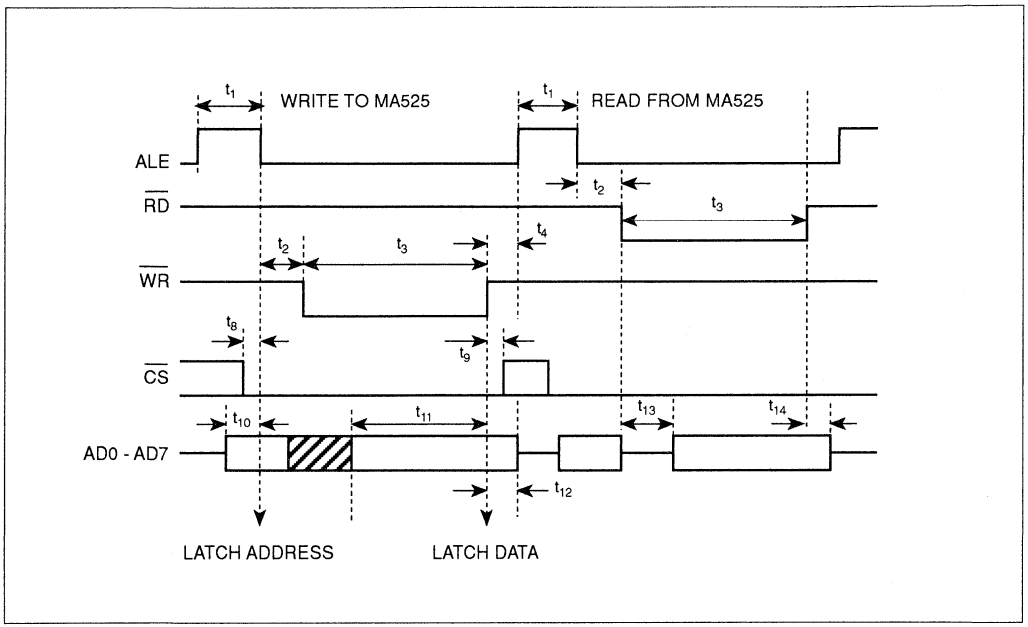


Figure 2: Intel bus timing diagram

Parameter	Symbol	Min.	Typ.	Max.	Units
ALE high period	t_1	70			ns
Delay time, ALE to $\overline{WR}$	t_2	40			ns
$\overline{WR}$ low period	t_3	50			ns
Delay time, WR high to ALE high	t_4	10		50µs	ns
$\overline{CS}$ setup time	t_8	40			ns
$\overline{CS}$ hold time	t_9	0			ns
Address setup time	t_{10}	30			ns
Address hold time	t_{15}	10			ns
Data setup time	t_{11}	50			ns
Data hold time	t_{12}	0			ns
Output data response time	t_{13}		60	85	ns
Output data removal time	t_{14}		30	50	ns

The address is latched by the falling edge of ALE. Data is written from the bus into the MA525 on the rising edge of $\overline{WR}$. Data can be read from the MA525 on the rising edge of $\overline{RD}$ providing that this follows the falling edge of $\overline{RD}$ by the minimum period, t_3. All bus timings are quoted with 30pF capacitance to V_{SS}.

Table 2: Intel bus timings at V_{DD} = 5V, T_{amb} = +25°C

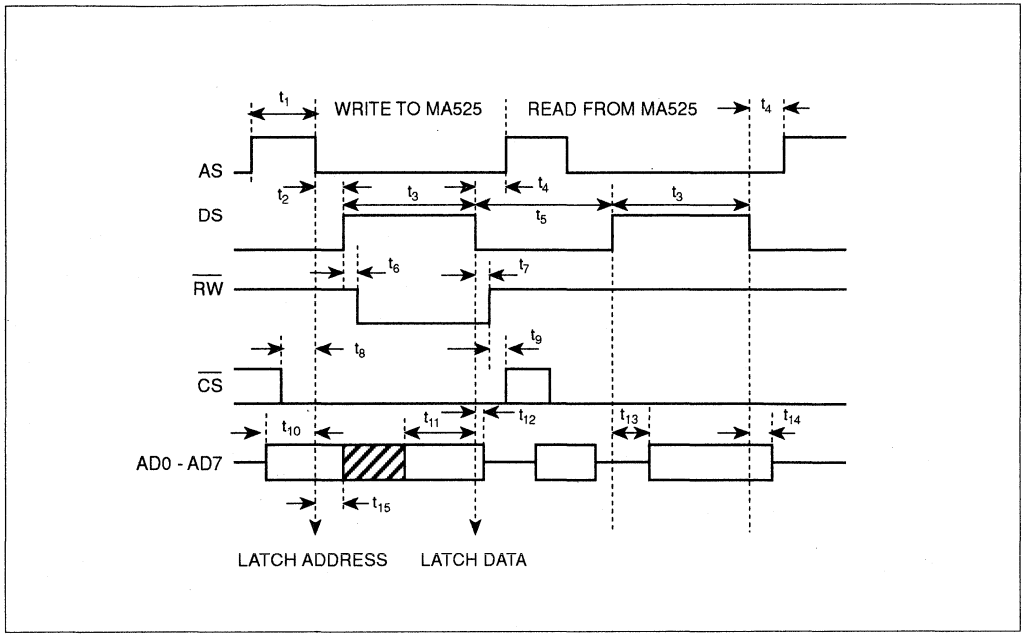


Figure 3: Motorola bus timing diagram

Parameter	Symbol	Min.	Typ.	Max.	Units
AS high period	t_1	50			ns
Delay time, AS low to DS high	t_2	40			ns
DS high period	t_3	40			ns
Delay time, DS low to AS high	t_4	10		50µs	ns
DS low period	t_5	165			ns
DS high to R/W low setup time	t_6	15			ns
R/$\overline{W}$ hold time	t_7	10			ns
$\overline{CS}$ setup time	t_8	40			ns
$\overline{CS}$ hold time	t_9	0			ns
Address setup time	t_{10}	30			ns
Address hold time	t_{15}	10			ns
Write data setup time	t_{11}	50			ns
Write data hold time	t_{12}	0			ns
Output data response time	t_{13}		55	80	ns
Output data removal time	t_{14}		35	50	

The address is latched by the falling edge of the AS line. Data is written from the bus into the MA525 when R/$\overline{W}$ is low on the falling edge of DS (providing $\overline{CS}$ is low). Data can be read from the MA525 when R/$\overline{W}$ is high on the falling edge of DS. All bus timings are quoted with 30pF capacitance to V_{SS}.

Table 3: Motorola bus timings at V_{DD} = 5V, T_{amb} = +25°C

REGISTER ADDRESSING

AD_3 - AD_0	Register	Type	Function
0000	R0	Write only	Digit buffer
0001	R1	Write only	Dial conditions
0010	R2	Write only	Control
0011	R3	Write only	Output Configuration
0100	R4	Write only	Access pause time
0101	R5	Write only	DTMF dialling
0110	R6	Write only	HSW response time
0111	R7	Write only	TBR (Flash) time
1000	R8	Write only	IDP time
1001	R9	Write only	Single tone O/P
1010	R10	Read only	Status

Table 4: MA525 register addressing

Default register conditions are automatically set in all programmable registers on power-up and remain valid until a register is reprogrammed In addition the dial store is cleared

Read commands to a 'write only' register and write commands to a 'read only' register will be ignored

Note that register 11 is provided for in-house test purposes and should not be used during normal device operation. If a register number greater than 11 is addressed, the command will be ignored and the ERROR bit raised.

REGISTER FUNCTIONS

(A summary showing register functions and calculations is given on page 1-85)

It is recommended that parameters set in Registers 1, 3, 4, 5, 7 and 8 should not be changed while dialling is in progress. However, parameters can be changed during the same call provided that dialling is not active (i.e. if the BUSY bit in the status register is at 0') at the time -there is no need to go on-hook or to set the DISCON bit before changing parameters.

If parameters in registers 1, 3, 4, 5, 7 or 8 are changed during dialling, misdialling may occur but the device will operate normally when the dial sequence is complete. The ERROR flag will not be raised in this case.

REGISTER 0 - DIGIT BUFFER

Digits to be sent to the dial store should be loaded into Register 0. To load a TBR or a Pause into the dial store the appropriate bits should be set in register 2. Digits will be sent to the dial store in the order in which they are loaded into registers 0 and 2.

Digits may be loaded into the dial store in blocks of up to 22 digits. If more than 22 digits are loaded in total it is important not to perform a last number redial to ensure correct operation.

Digits can be loaded into Register 0 either before or after the DIAL Bit is set in Register 2. Digits loaded after the DIAL bit is set will be concatenated with any digits yet to be dialled. However, if digits are loaded whilst a Last Number Redial is being dialled the digits will be ignored.

Each digit can be loaded into the dial store using a handshaking routine. As each digit is loaded into register 0 (or bits 2 and 3 in register 2) the BUF bit is set in the status register (Register 10). When the digit has been accepted into the dial store from Register 0, the BUF bit is cleared. indicating that the next digit can be loaded into register 0. Alternatively digils can be loaded directly without monitoring the BUF bit providing that the timing requirements are met (see a.c. conditions). In either case the ERROR bit in the Status Register will be set if an attempt is made to load a digit while the BUF bit is set to 1 and the digit will not be accepted.

Up to 21 undialled digits can be held in the dial store at a time. Once the dial store is full the BUF bit will be set to 1 and no further digits can be loaded until it is reset to 0 either because space becomes available (due to digits having been dialled out) or until the device is sent onhook (in Phone mode) or DISCON is set to 1 (Modem mode).

Codes *,A,B,C,D and # are illegal in LD mode and will not be accepted into Register 0 while the device is set to LD mode. If an attempt is made to do this the ERROR bit will be set in the Status Register.

Bits 3210	Code	Digit	Comment
0000	0	0	0 = 10 pulses in LD mode
0001	1	1	
0010	2	2	
0011	3	3	
0100	4	4	
0101	5	5	
0110	6	6	
0111	7	7	
1000	8	8	
1001	9	9	
1010	10	*	Not allowed in LD mode
1011	11	A	Not allowed in LD mode
1100	12	B	Not allowed in LD mode
1101	13	C	Not allowed in LD mode
1110	14	D	Not allowed in LD mode
1111	15	#	Not allowed in LD mode

Table 5: Register 0 - digit buffer

REGISTER 1 - DIAL CONDITION REGISTER

Bit	Name	Default	Function
0	USE	0	Phone or Modem use 0 = Phone, 1 = Modem
1	B/M	0	Break/Make ratio 0 = 2:1, 1 = 3:2
2	DS	0	Dialling Speed (LD) 0 = Normal, 1 = Double
3	MODE	0	LD/DTMF dialling 0 = LD, 1 = DTMF

Table 6: Register 1

If the USE bit is cleared whilst the LINE output is at a '1' state, the LINE output will not be cleared. Normal Phone Mode operation will resume after the DISCON bit is next set.

Bit 2 of register 1 defines the dialling speed in LD only. If this bit is cleared the dialling speed will be set to 10 impulses per second and all other timings will be as per the relevant registers. If the DS bit is set however, the dialling speed will be 20 impulses per second and all other timings will also be halved.

REGISTER 2 - CONTROL REGISTER

Bit	Name	Default	Function
0	DIAL	0	Start dial sequence 1 = Start
1	DISCON	1	Disconnect 0 = Seize line, 1 = Disconnect line
2	ACCESS	0	Load access pause = 1
3	TBR	0	Load TBR (Flash) = 1

Table 7: Register 2

When the DIAL bit is set to 1, dialling will start, assuming DISCON is set to 0. If dialling is terminated either by the HSW being timed out (in Phone mode) or by sening the DISCON bit to 1 (in both modes), the dial bit is automatically reset to 0. Note that forcing the DIAL bit low using the microprocessor interface does *not* terminate dialling .

In Phone mode, setting the DISCON bit simply terminates dialling immediately. The device outputs then revert to their normal 'off-hook and idle' states. If, when programming Register 2 in Phone mode an attempt is made to set both the DIAL and DISCON bits to '0', the command will be ignored .

In Modem mode, setting the dial bit causes LINE to make a low to high transition after 6.6ms. After dialling is completed, the LINE output will remain high, thereby holding the line for subsequent speech/data interchange DISCON may be used at any time to relinquish the line thus ending the call. Further digits may be loaded and dialled at any time whilst LINE is high.

If, when programming register 2, an attempt is made to set both the DIAL and DISCON bits to '1', DIAL will be set to '0' and DISCON to '1', i.e. DISCON takes priority. The DIAL / DISCON protocol is shown in State Diagram form in Figs. 4 and 5. If PAUSE and TBR bits are set simultaneously, the write operation will be ignored and the ERROR flag raised.

If an LNR is required after setting DISCON, simply set the DIAL bit In order to prevent the device redialling the previous number, it is necessary to clear the DISCON bit f irst .

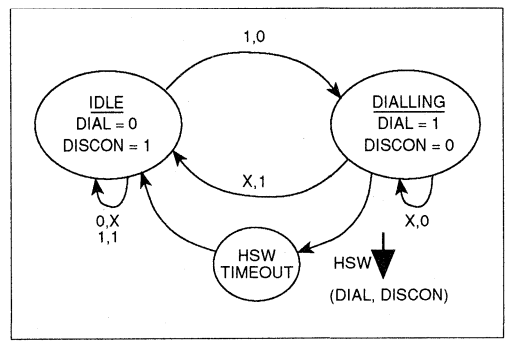


Figure 4: Finite state diagram - Phone mode

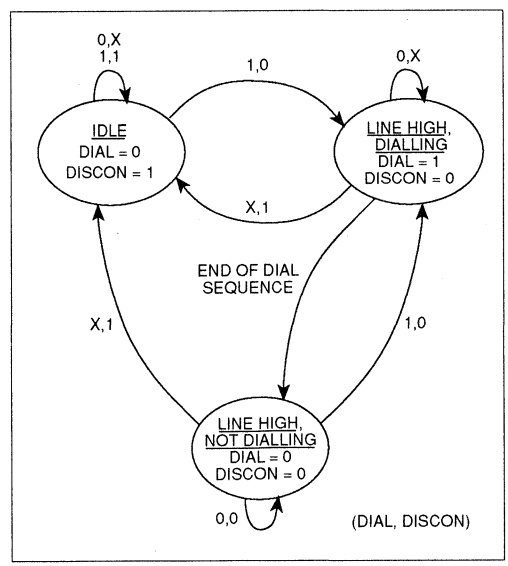


Figure 5: Finite state diagram - Modem mode

Note that since TBR and Pause are treated as normal digits, the device places a Pre-Digit Pause before, and an Inter-Digit Pause after the TBR/Pause whilst in LD mode. In DTMF mode, a tone pause period (as defined by register 5) is placed both before and after the TBR/Pause.

On power up, if the DIAL bit is set without first loading any digits in LD mode, the device defaults to dialling an access digit (9).

WARNING: No response will be obtained if Access Pause or TBR is entered as the first digit in a string with nondefault values in either Pause Duration register or TBR Duration register whilst in DTMF mode. If this condition is inadvertantly invoked it may be cleared by setting the DISCON bit (in both Phone and Modem modes), toggling the HSW input (in Phone mode only) or by powering down the MA525.

REGISTER 3 - OUTPUT CONFIGURATION REGISTER

Bit	Name	Default	Function
0	IE	0	Interrupt Enable 0 = Disable, 1 = Enable
1	LS	0	LINE output polarity 0 = Normal. 1 = Invert
2	MS	0	MUTE output polarity 0 = Normal, 1 = Invert
3	KS	0	MASK output polarity 0 = Normal, 1 = Invert

Table 8: Register 3

Disabling the Interrupt Enable simply disables both the IRQ output (i.e. high-impedance open-drain) and the IRQF bit in the Status Register.

REGISTER 4 - ACCESS PAUSE DURATION

Code	Default	Function
1 - 15	1 (ie. 500ms)	Set length of Access Pause. Duration = Code x 500ms.

Table 9: Register 4

If code 0 is loaded, the Access Pause duration will be set to the default value and the ERROR bit will be set in the status register.

If pauses longer than 7.5 seconds are required, Pauses may be programmed more than once in succession. This will give a longer 'seamless' pause with no transitions on any device outputs.

REGISTER 5 - DTMF DURATION

Bit	Name	Default	Function
0 - 3	Duration	15 (100ms)	Set tone on/off period. Period = (Code x 6.67) ms.

Table 10: Register 5

Register 5 sets both the active tone period and the pause time between tones. Note that if code 0 is loaded the DTMF duration is set to the default value and the ERROR bit will be raised in the Status Register.

REGISTER 6 - HOOKSWITCH RESPONSE TIME

Code	Default	Function
0 - 15	2 (ie. 200ms)	Set Hookswitch timeout period Duration = Code x 100ms.

Table 11: Register 6

The hookswitch timeout period is the time taken between the hookswitch going low and the on-hook condition being recognised by the MA525. It is used to differentiate between short line breaks due to electrical noise (or line polarity reversal) and the user placing the handset on-hook. If the HSW input returns high before the timeout period has elapsed then the on-hook condition is not recognised. The status of the HS bit in the status register reflects the immediate status of the HSW input rather than whether the device recognises the on-hook or off-hook condition. It should be noted that the actual hookswitch response time will vary between the nominal duration set and up to 100ms greater than this (eg. if 200ms is set the response time is 200-300ms).

Parameters set in Register 6 should not be changed when a hookswitch timeout is occuring, as this may give an unpredictable timeout period. If this occurs, however, the device will behave as normal after the timeout is complete.

REGISTER 7 - TIMED BREAK RECALL (FLASH) PERIOD

Code	Default	Function
0 - 15	1 (ie. 100ms)	Set TBR (Flash) Period. Duration = Code x 100ms.

Table 12: Register 7

If code 0 is loaded, the TBR (Flash) Period will be set to the default value and the ERROR bit will be set in the status register.

REGISTER 8 - INTER-DIGIT PAUSE DURATION

Code	Default	Function
0 - 15	8 (ie. 800ms)	Set IDP duration (LD dialling) Duration = Code x 100ms.

Table 13: Register 8

The IDP duration applies only to LD dialling. If code 0 is loaded, the IDP duration will be set to the default value and the ERROR bit will be set in the status register

REGISTER 9 - SINGLE TONE OUTPUT

Code	Default	Function
0 - 7	Disable	Disable single tone output
8		Enable 697 Hz output
9		Enable 770 Hz output
10		Enable 852 Hz output
11		Enable 941 Hz output
12		Enable 1209 Hz output
13		Enable 1339 Hz output
14		Enable 1477 output
15		Enable 1663 Hz output

Table 14: Register 9

When selected. the single tone output is generated from the DTMF output. The output level is therefore dependent upon whether the particular tone is in the high or low frequency group (see AC characteristics). Once selected, the single tone output is continuous until it is either disabled or until another single tone is selected. Single tones cannot be selected in LD mode.

Single tone outputs are active whether the device is on or off-hook.

During single tone outputs the BUSY bit is not set In addition, the device outputs (MUTE,MASK and LINE) will remain inactive.

If the DIAL bit is set whilst a single tone is active, the device will behave as it it is dialling (i.e. BUSY bit set, MUTE active et cetera) although the single tone will take priority on the TONE pin. It is therefore important to disable single tones before a DTMF dialling sequence.

REGISTER 10 - STATUS REGISTER (READ ONLY)

Bit	Name	Function
0	BUSY	Indicates dialling in progress: 1 = Busy
1	ERROR	Indicates programming error: 1 = Error
2	HS	Indicates hookswitch status: 0 = available 1 = in use
3	BUF	Indicates digit buffer status: 0 = available 1 = in use
7	IRQF	Interrupt request set flag: 0 = clear 1 = set

Table 15: Register 10

BIT 0: BUSY

The BUSY bit is active (i.e. set to '1') during dialling ot digits, TBR and Pauses in either LD or DTMF modes.

The BUSY bit is automatically reset to '0' when:

1. A dialling sequence is complete.
2. A dialling sequence is terminated by setting the DISCON bit (Reg 2) to 1.
3. A dialling sequence is terminated by an on-hook timeout.

BIT 1: ERROR

In general, the ERROR bit is raised when an illegal operation is performed. Some operations, such as changing certain registers whilst dialling, are not fundamentally illegal but are nevertheless not recommended Such errors do *not* raise the ERROR tlag.

The ERROR bit is always reset by reading the Status Register.

The ERROR bit is set to 1 under the following conditions:

1. When an attempt is made to load illegal digits into the digit buffer (Reg0) while the device is set to LD mode (i.e. A,B,C,D,*or #).
2. When an attempt is made to dial an illegal digit in LD mode (i.e. A,B,C,D,*or #) loaded whilst the device is in DTMF mode . If an attempt is made to load a digit into the dial store while the BUF bit is set to 1.
4. If an attempt is made to load code 0 into registers 4, 7 or 8.
5. When a register addressing error is made (i.e. if a register number greater than 11 is addressed).

BIT 2: HS

The HS bit is set to 1 immediately the HSW input goes high. HS remains high until the HSW input goes low, when it will be reset to 0. The status ot the HSW input has no relevance to device operation when in Modem mode, but the HS bit remains operational. If DISCON is invoked during a hookswitch timeout the device will assume the on-hook condition instantly, i.e. DISCON takes priority over the hookswitch timeout.

BIT 3: BUF

When the BUF bit is set to 0, this indicates that a digit (or a TBR or Pause) can be ioaded into the dial store via Register 0, the digit buffer (or via Register 2)

When the BUF bit is set to 1 this indicates that the temporary digit buffer is not available for use and that digits should therefore not be loaded If a digit is loaded while BUF = 1, it will not be accepted and the ERROR bit and IRaF will be set.

The BUF bit is set to 1 under the following conditions

1. While the MA525 is accepting a digit from the temporary digit buffer to the dial store. A handshaking procedure, as shown in Fig. 6, can be used to load digits from the digit buffer to the dial store. Such handshaking will ensure correct loading of the digits whether or not the MA525 oscillator is running at the time of first loading. Providing that the oscillator is running (see Oscillator Circuit section) handshaking need not be used so long as the buffer timing constraints are observed.
2. When the dial store is full and therefore unable to receive any further digits. As soon as a dial store location becomes available the BUF bit will be reset to 0 and the digit previously held in the buffer will be transferred to the dial store

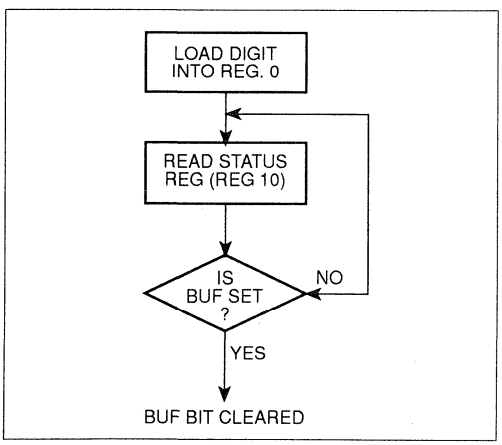


Figure 6: Digit loading handshaking procedure

BIT 7: IRQF

The IRQF bit simply reflects the status of the $\overline{IRQ}$ output. The IRQF bit is set to 1 ($\overline{IRQ}$ = 0) under the following conditions:

1. Whenever the ERROR bit is set to 1.
2. Whenever a dialling sequence is completed (but not if DISCON is asserted or the hookswitch is taken low before the sequence is complete).

The IRQF bit and $\overline{IRQ}$ are returned to their inactive states by reading the status register.

Note that if IRQF goes high and is subsequently cleared as a consequence of a good sequence, the Status Register will hold the data relating to the latter (correct) operation and not the former (incorrect) operation.

LAST NUMBER REDIAL FACILITY

The MA525 will dial the previous contents of the dial store if:

(i) No digits are loaded between HSW being timing out (or DISCON being set) and DIAL being set in Phone Mode.(See Fig. 7).

(ii) No digits are loaded between DISCON being set and DIAL being set in Modem Mode.(See Fig. 8).

Note:

(i) Digits cannot be appended to an LNR.

(ii) The presence of a Timed Break Recall (TBR) or Access Pause does not affect the LNR - they are simply treated as another digit.

OSCILLATOR CIRCUIT

The oscillator circuit requires an external 560kHz ceramic resonator between OSC and Vss. No other components should be used. Please see your resonator supplier who will recommend a suitable resonator type. The OSC pin may also be driven by an external logic signal if required .

Under normal MA525 operation, the oscillator will be started during dialling or digit loading sequences and shutdown afterwards in order to conserve power and reduce possible crosstalk to speech or other sensitive circuits.

Thus the oscillator will be started by:

1. The presence of a digit in the digit buffer. (whilst offhook or in Modem mode).
2. DIAL bit being set (whilst off-hook or in Modem mode).
3. Whilst performing a hookswitch timeout (whilst in Phone mode only).
4. Beginning a Single Tone output.

The oscillator will be shut-down following:

1. A hookswitch timeout (in Phone mode only).
2. DISCON bit being set.
3. Completion of a dialling sequence.
4. BUF being cleared. Note that if a 23rd digit is loaded, it will reside in the buffer until a space becomes available for it in the dial store. In the meantime, BUF will be set and the oscillator will run continuously. To ensure minimum crosstalk with any speech circuitry, it is advisable to avoid this situation.
5. Ending a Single Tone output.

Note that reading the Status Register will not restart the oscillator. Hence data held in this Register will not be updated after the oscillator has been shut-down.

Since the oscillator is stopped whilst the hookswitch is down in Phone mode it is not possible to load digits into the dial store. A single digit can be held in the buffer, however, until the device is next taken off-hook. Digits may, however, be loaded at any time whilst in Modem mode irrespective of hookswitch and DISCON status.

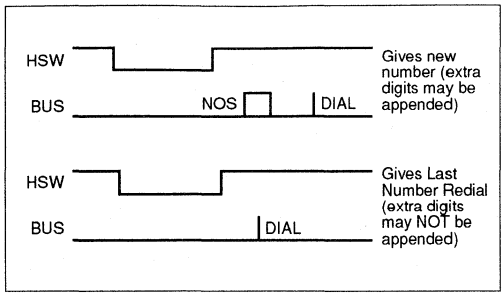


Figure 7: LNR protocol - Phone mode

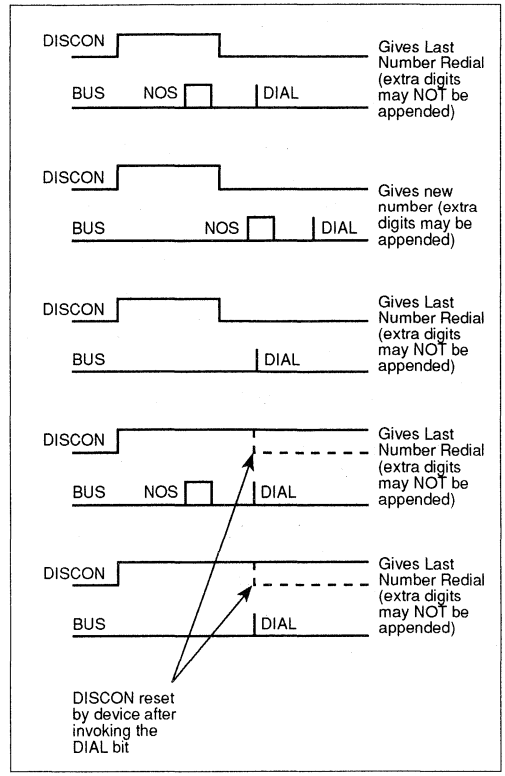


Figure 8: LNR protocol - Modem mode

Reg no.	Name	Bit 3 (MSB)	Bit 2	Bit 1	Bit 0 (LSB)
1	DIAL CONDITIONS	**MODE** 0 PULSE 1 DTMF	**DIAL SPEED** 0 NORM 1 DOUBLE	**B/M RATIO** 0 = 2:1 1 = 3:2	**USE** 0 PHONE 1 MODEM
2	CONTROL REGISTER	**TBR**	**ACCESS PAUSE**	**DISCON**	**DIAL**
3	OUTPUT CONFIGURATION	**MASK POLARITY** 0 NORM 1 INV	**MUTE POLARITY** 0 NORM 1 INV	**LINE POLARITY** 0 NORM 1 INV	**IE** 0 DISABLE 1 ENABLE
10	STATUS REGISTER	**BUF** 0 AVAIL 1 IN USE	**HS** 0 OFFHK 1 ONHK	**DIGIT ERROR**	**BUSY BIT**

Table 16: Summary of registers 1, 2, 3 and 10 functions

Reg. no.	Function	Coding
4	ACCESS PAUSE DURATION	CODE x 500ms
5	DTMF DURATION	CODE x 6.67ms
6	HOOKSWITCH RESPONSE TIME	CODE x 100ms
7	TBR (FLASH) DURATION	CODE x 100ms
8	INTER-DIGIT PAUSE DURATION	CODE x 100ms

Table 17: Summary of registers 4, 5, 6, 7 and 8 functions

Code	Register 9 - Single Tone Output
0-7	Disable single tone output
8	Enable 697 Hz output
9	Enable 770 Hz output
10	Enable 852 Hz output
11	Enable 941 Hz output
12	Enable 1209 Hz output
13	Enable 1336 Hz output
14	Enable 1477 Hz output
15	Enable 1663 Hz output

Table 18: Register 9 summary

PULSE DIALLING IN PHONE MODE

The MASK output is provided in order to disable the speech circuit during LD (Pulse) dialling. Consequently, the MASK output is normally at logic '0' in the off-hook condition, but changes to logic '1' during LD dialling. MASK also changes to logic '1' in order to signal a Timed Break Recall (Flash) to the line.

LD dialling is signalled on the LINE output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the LINE output sits at logic '0'.

Both MUTE and TONE outputs remain low during LD dialling. LINE, MUTE and MASK outputs may be inverted independently it desired.

If the HSW input goes low whilst dialling, the LINE and MASK outputs continue as normal until the hookswitch timeout occurs. If the hookswitch goes high again before the timeout, LINE and MASK will continue uninterrupted. The BUSY bit (Reg 10) will remain high until either the dialling sequence linishes internally or until a hookswitch timeout occurs (whichever comes first).

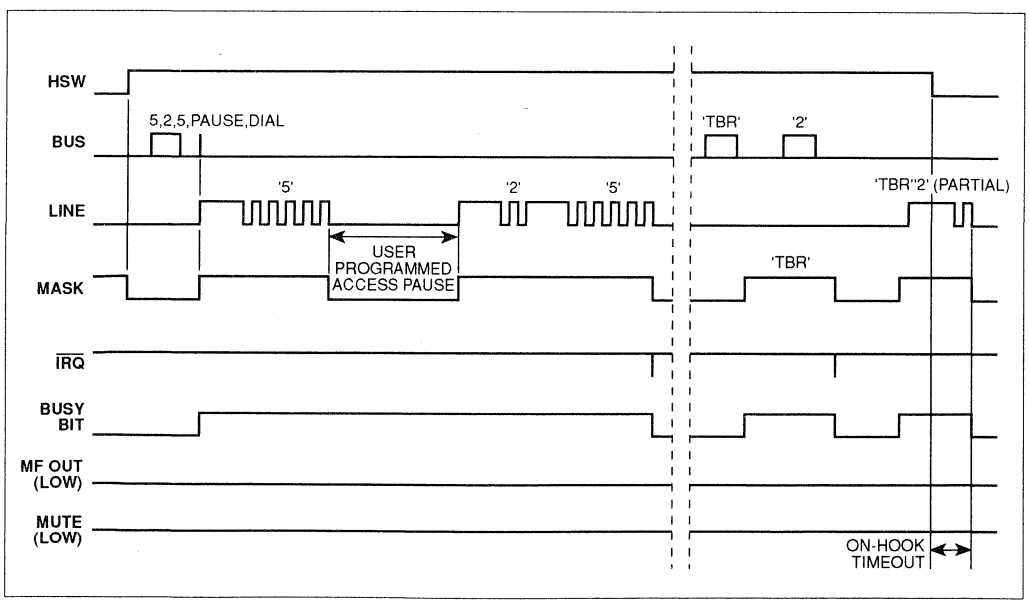
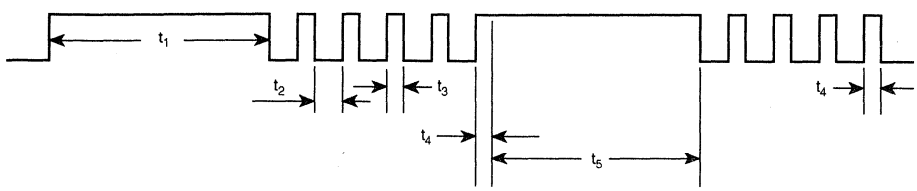


Figure 9: LD/phone mode timing diagram



Break:Make ratio	2:1	3:2	t_1 = Pre-digit pause (= t5): 100 to 1500ms (as set in Reg. 8)
t_2 = Break Period	67ms	60ms	t_4 = Post-digit make (= t3)
t_3 = Make Period	33ms	40ms	t_5 = Inter-digit pause

N.B. If dialling speed is set to Double Speed, all timings will be halved.

Figure 10. Timing data

PULSE DIALLING, IN MODEM MODE

The MASK output is provided in order to disable the speech circuit during LD dialling. Consequently, the MASK output is normally at logic '0' in the off-hook condition, but changes to logic 1' during LD dialling. MASK also changes to logic '1' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and TONE remain low during LD dialling. LINE, MUTE and MASK may be inverted independently if desired.

The status of the HSW input is irrelevant in Modern mode. However, HSW status can still be read from register 1 O.

The LINE output is used to control the on/off-hook status and for LD dialling. The line will be seized when dialling starts. A break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. After dialling finishes the LINE output will remain high until the line is disconnected by setting the DISCON bit to '1'.

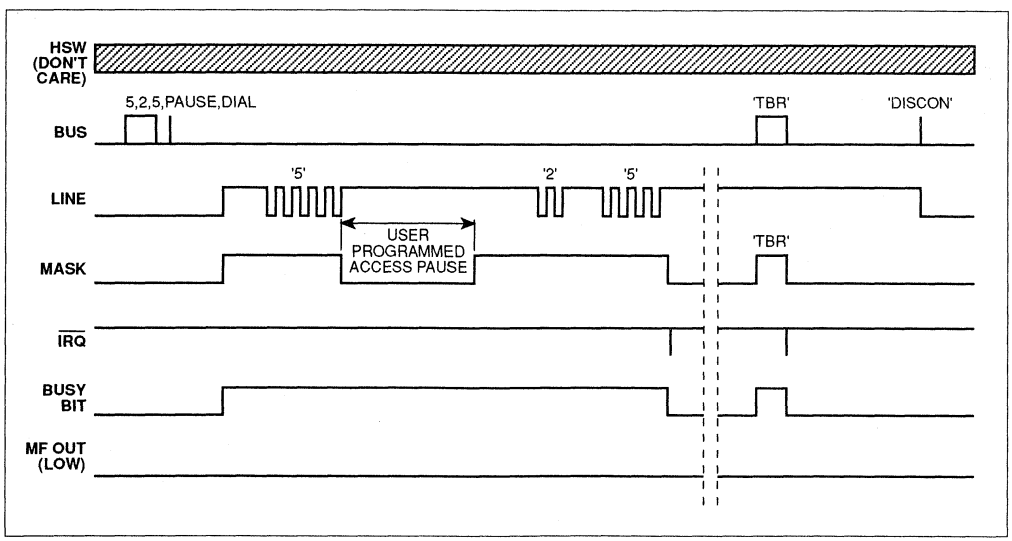


Figure 11: LD/modem mode timing diagram

DTMF DIALLING IN PHONE MODE

During DTMF dialling the MUTE output goes to logic '1' and remalns there for the duration of the tone transmission The LINE output remains low during tone transmission.

The MF OUT output rises to its DC level as soon as the MODE bit in register 1 is set and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

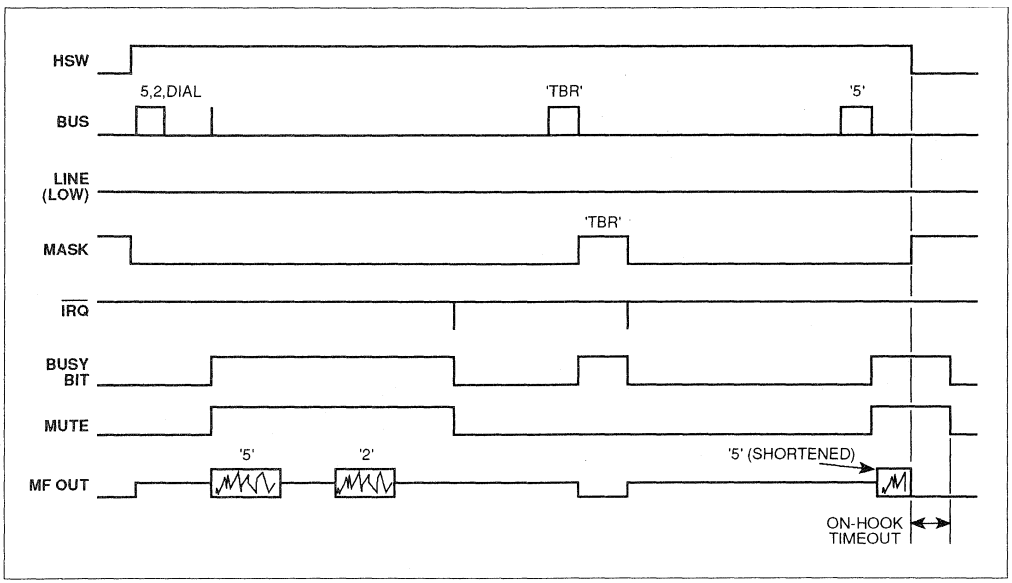


Figure 12: DTMF/phone mode timing diagram

	1209Hz	1336Hz	1447Hz	1633Hz
697Hz	1	2	3	A
770Hz	4	5	6	B
852Hz	7	8	9	C
941Hz	*	0	#	D

Table 19: Tone frequencies

Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	-0.07	-0.10	+0.19	-0.15	-0.17	-0.20	-0.22	-0.31

NOTE:
There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 20: Tone frequency accuracy

PULSE DIALLING IN MODEM MODE

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission. The LINE output is used to control the on/off hook status whilst MF OUT is used for tone transmission.

The MF OUT output rises to its DC level as soon as the MODE bit is set and remains there during tone bursts. This is to avoid transients at the beginning and end of tone bursts.

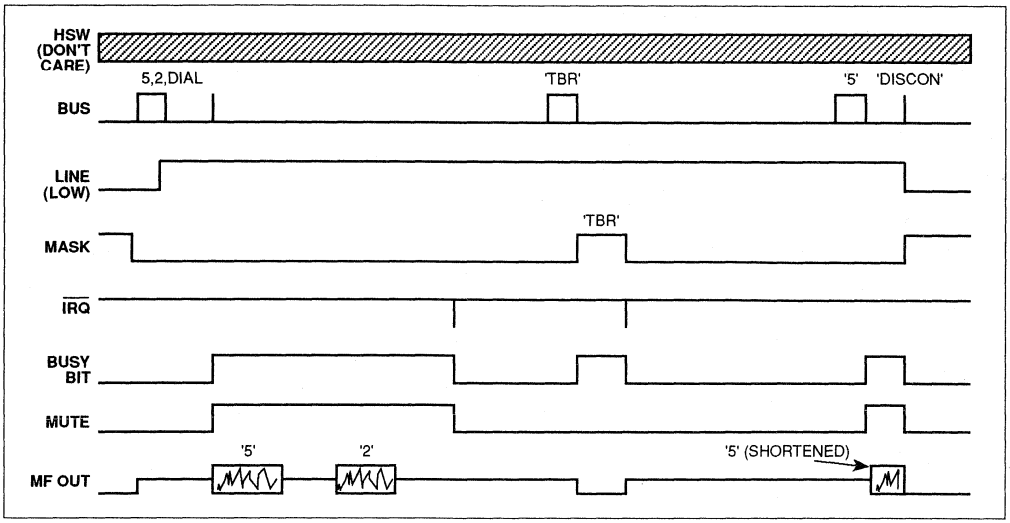


Figure 13: DTMF/Modem mode timing diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): T_{amb} = 25°C

DC CHARACTERISTICS AT V_{DD} = 2.5V

Characteristic		Min.	Typ.	Max.	Units	Condition
Supply Current:	On-hook		< 0.2	5.0	µA	V_{DD} = 2.0V. See note 1.
	Off-hook		1.5		µA	MF OUT low
	MF tone sending			1.0	mA	
	LD impulsing			200	µA	
Output high voltage (MASK, MUTE and LINE outputs)		2.2			V	I = -1 mA
Output low voltage (MASK, MUTE and LINE outputs)				0 3	V	I = + 1 mA
MF OUT DC level during tone sending			$0.5V_{DD}$			
MF OUT output resistance			15	20	kΩ	
Microprocessor interface: input high		-	2.0	V_{DD}	V	
Input low		-	0	0.5	V	
Output high		2.3	-	-	V	I = -50µA
Output low		-	-	0.2	V	I = + 50µA
$\overline{IRQ}$ Output	Output low			0.2	V	I = + 50µA
	Output high leakage	-	-	1	µA	

NOTE:

1. Specially tested versions with guaranteed lower on-hook supply current are available

DC CHARACTERISTICS AT V_{DD} = 5V

Characteristic		Min.	Typ.	Max.	Units	Condition
Supply Current:	On-hook		1.5		µA	MF OUT low
	MF tone sending		0.5	2.0	mA	
	LD impulsing			0.5	mA	
Output high voltage (MASK, MUTE and LINE outputs)		4.55	4.8		V	I = -10 mA
Output low voltage (MASK, MUTE and LINE outputs)			0.2	0.45	V	I = + 10 mA
Microprocessor interface: input high		-	2.0	V_{DD}	V	
	Input low	-	0	0.8	V	
	Output high	4.6	-	-	V	I = -1mA
	Output low	-	-	0.4	V	I = + 1mA
$\overline{IRQ}$ Output	Output low	-	-	0.4	V	I = + 1mA
	Output high leakage	-	-	1	µA	

NOTE:

2. All other characteristics are as specified at V_{DD} = 2.5V given on page 1-89.

AC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Tone output at VDD = 2 5V: LOW group	285	320		mV rms	No load
High group		405	455	mV rms	No load
Tone output at VDD - 5V: LOW group	570	640		mV rms	No load
High group		810	910	mV rms	No load
High-to-Low group amplitude ratio (pre-emphasis)	1.5	2	2.5	dB	All V_{DD}, see note 3
Total harmonic distortion: 0-4 kHz		1 5		%	All V_{DD}
0-10 kHz		25		%	All V_{DD}
0-50 kHz		50		%	All V_{DD}
0-200 kHz	_	65	10	%	All V_{DD}
Oscillator start-up time		< 0.1	1	ms	

NOTE:

3. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING TEMPERATURES

Condition		Min.	Typ.	Max.	Units	Notes
Supply Voltage:	On-hook	1.8		5.7	V	For memory retention
	Off-hook	2.4		5.7	V	
Hookswitch Input:	On-hook			$0.2V_{DD}$ V		
	Off-hook	$0.8V_{DD}$				
Oscillating frequency			560		kHz	
Digit load to dial store accept time (BUF high time)				36	µs	See note 4

NOTE:

4. Assumes oscillator is running. If oscillator is not running, add start-up time given in AC Characteristics above.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}-V_{SS}	-0.3 to 6.5V
Voltage on any pin (except HSW)	V_{SS} - 0.3V to V_{DD} + 0.3V
Voltage on HSW pin (See note 5)	V_{SS}- 0.3V min
Current at any pin (except HSW)	±1 mA
Storage temperature	-55°C to +125°C
Operating temperature range	-10°C to +55°C

NOTES

5. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300µA max no damage will occur.

6. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Section 2
PCM Circuits

GEC PLESSEY
SEMICONDUCTORS

MV1442

HDB3 ENCODER/DECODER/CLOCK REGENERATOR

(Supersedes June 1993 edition)

The MV1442, along with other devices in the GPS 2Mbit PCM signalling series comprise a group of circuits which will perform the common channel signalling and error detection functions for a 2.048Mbit PCM transmission link operating in accordance with the appropriate CCITT recommendations. The circuits are fabricated in CMOS and operate from a single +5V supply with all inputs and outputs being TTL compatible.

The MV1442 is an encoder/decoder for the HDB3 pseudo–ternary transmission code, described in Annex A of CCITT Recommendation G. 703. The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of the HDB3 coding, all ones detection and loss of input (all zeros detection). In addition a loop back function is provided for terminal testing. The MV1442 may be selected to function in either internal or external clock recovery modes. Internal clock recovery mode may be selected for either 1.544MHz or 2.048MHz operation and in this mode an external 16.384MHz crystal (12.352MHz for 1.544MHz Operation) is required. External clock recovery mode may be selected for 1.544MHz, 2.048MHz or 8.448MHz operation.

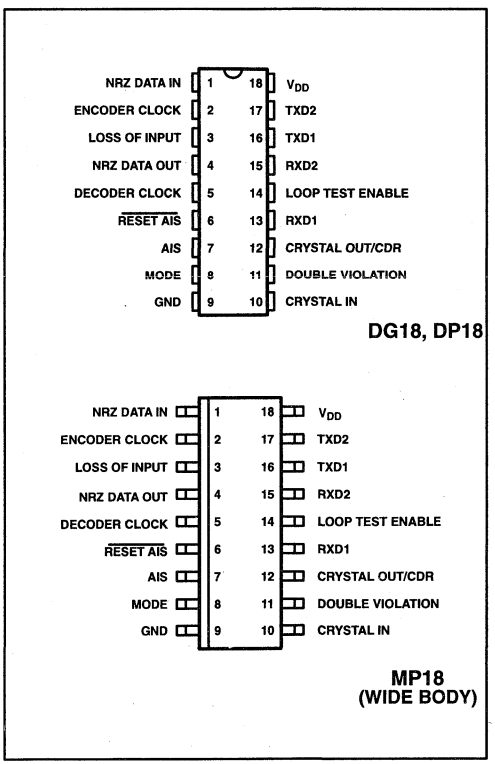


Fig. 1: Pin connections – top view

FEATURES

- On–chip Digital Clock Regenerator
- HDB3 Encoding and Decoding to CCITT Recommendation G.703
- Asynchronous operation
- Simultaneous Encoding and Decoding
- Clock Recovery signal allows Off–chip Clock Regeneration
- Loop Back Control
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm
- Low Power Operation
- 2.048MHz or 1.544MHz Operation in External or Internal Clock Recovery mode
- 8.448MHz Operation in External Clock Recovery mode

ORDERING INFORMATION

MV1442/IG/DPAS DIL plastic package
MV1442/IG/DGAS DIL cerdip package
MV1442/IG/MPES Minature plastic package

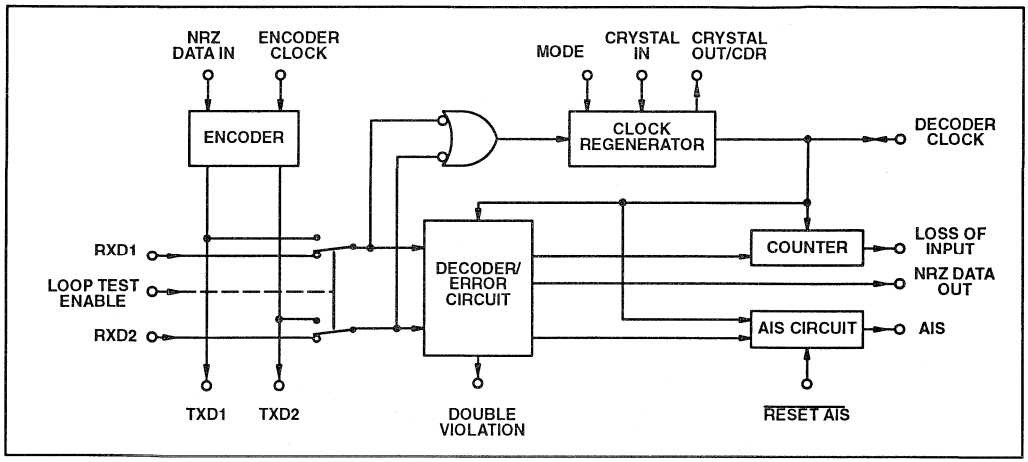


Fig. 2: Block diagram

FUNCTIONAL DESCRIPTION

High Density Bipolar 3 (HDB3) is a pseudo–ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to allow adequate clock recovery at the receiver. In any sequence of four consecutive binary zeros, the last zero is substituted by a mark of the same polarity as the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code, and ensures that successive violations alternate in polarity and as such introduce no DC component to the HDB3 signal.

The MV1442 consists of three main blocks, the HBD3 Encoder, the HDB3 Decoder and the Clock Regenerator. The function of each block is now described separately.

HDB3 ENCODER

The HDB3 Encoder is responsible for converting the incoming NRZ data into pseudo–ternary form for transmission over a PCM link. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703. The data to be encoded is input on the NRZ DATA IN pin and the encoding process is synchronised to the clock signal being input on the ENCODER CLOCK pin. The two TXD outputs, TXD1 and TXD2, represent the HDB3 data in pseudo–ternary form. If a mark is to be transmitted the output goes high after the rising edge of the clock. The length of the pulse is set by the positive clock pulse width. The timing diagram of the HDB3 Encoder is shown in Fig.3.

HDB3 DECODER

The HDB3 Decoder is responsible for decoding the HDB3 pseudo–ternary data on its inputs RXD1 and RXD2, into NRZ form to be output on the NRZ DATA OUT pin. In addition to this the decoder circuit provides three alarm outputs. The first of these alarms is DOUBLE VIOLATION. As its name suggests, a logic high on this output denotes that two successive violations have been received with the same polarity, thus violating the HDB3 coding laws. The second alarm, LOSS OF INPUT, is used to denote that 11 consecutive zeros have been received on the RXD inputs. The final alarm output is AIS (All ones). This alarm goes high if less than 3 decoded zeros have been detected in the preceding RESET AIS = 1 period (i.e. between RESET AIS = 0 pulses) and as such this alarm can be used as an all ones' detector. The decoding process and all the alarm circuitry is synchronised to the clock signal being input to this block on the DECODER CLOCK pin. This clock signal may be asynchronous with the ENCODER CLOCK signal. The timing diagrams of the HDB3 Decoder and alarm circuitry are shown in Figs. 4 to 7.

In addition to the normal mode of operation, a loop test mode is available for terminal testing. This mode is selected by taking the LOOP TEST ENABLE input high. In this mode, the HDB3 encoded pseudo–ternary data outputs of the Encoder block are fed back as the inputs to the Decoder block, which in turn decodes this data and outputs it in NRZ form.

CLOCK REGENERATOR

The Clock Regenerator block has two possible modes of operation. With the MODE pin high, internal crystal controlled clock regeneration is selected whilst with the MODE pin low, external clock regeneration is selected, using, for example, a tuned circuit.

In external clock regeneration mode, a logically 'OR'ed version of the HDB3 data, from the RXD inputs, is output to the external clock regeneration circuitry on the CRYSTAL OUT/CDR pin. The regenerated clock is then fed back into the MV1442 on the DECODER CLOCK pin. External clock regeneration may be used for operation with data rates of 1.544Mbits, 2.048Mbits or 8.448Mbits.

In internal clock regeneration mode, the logically 'OR'ed data is input to a digital regenerator, which constantly resynchronises a divide–by–8 counter to the incoming data stream. The clock thus regenerated is output to the decoder circuitry and to any external circuitry on the DECODER CLOCK pin. A crystal of frequency 8 times the required data rate must be connected between the CRYSTAL IN and CRYSTAL OUT/CDR pins. Thus the crystal frequency needs to be 16.384MHz or 12.352MHz for data rates of 2.048Mbits or 1.544Mbits respectively. Internal clock regeneration may not be used for operation at a data rate of 8.448Mbits.

The MV1442 is capable of withstanding up to 0.25UI of peak to peak input jitter at a jitter frequency of 2.048MHz without introducing errors into the decoded data. At lower jitter frequencies, the MV1442 is capable of withstanding much larger values of peak to peak input jitter. In the absence of input jitter, the MV1442 will produce an output jitter waveform in the form of a sawtooth ramping between 0UI and 0.125UI. The period of this waveform will be dependent upon the difference

in frequencies between the remote transmitters clock and the crystal controlled clock of the MV1442.

The MV1442 was originally designed as a pin compatible replacement for the MV1441 with a much improved internal clock recovery circuit and allowing operation at 8.448MHz with external clock recovery selected. However, there are certain minor differences between the two circuits which are described in a separate Applications Brief (AB33).

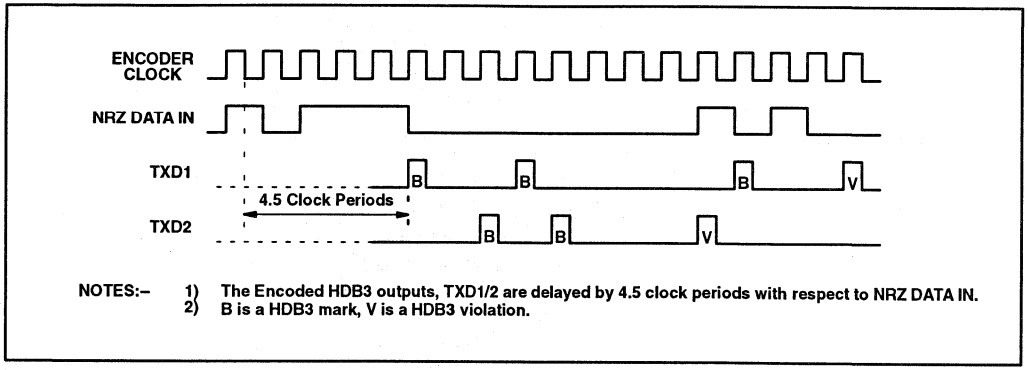


Fig. 3: Encoder waveforms

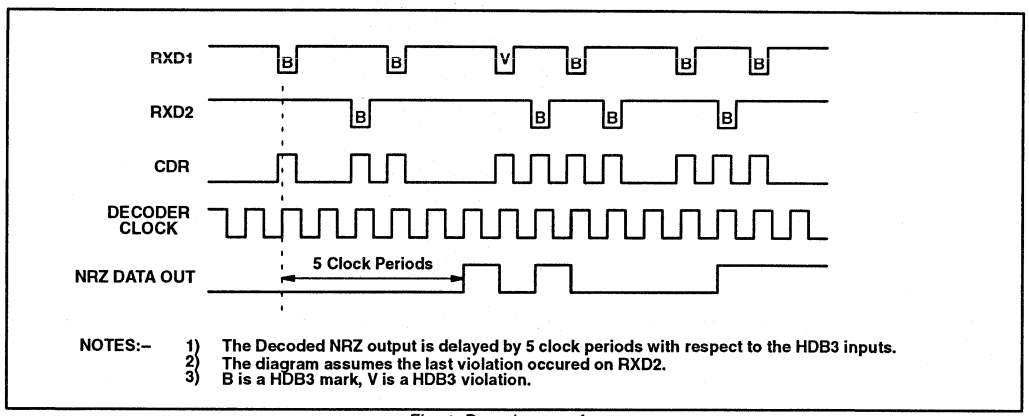


Fig. 4: Decoder waveforms

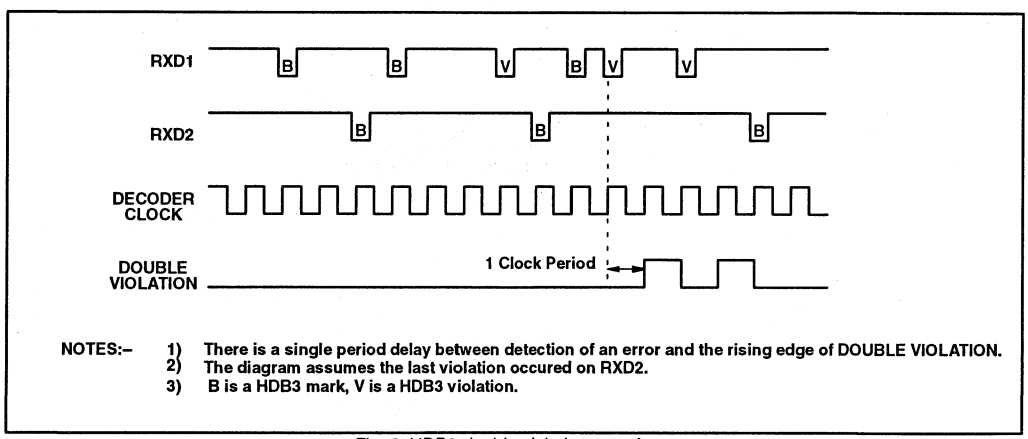


Fig. 5: HDB3 double violation waveforms

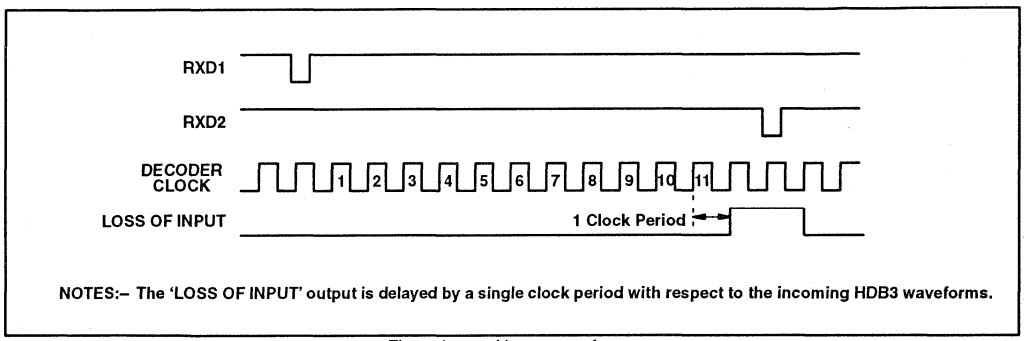


Fig. 6: Loss of input waveforms

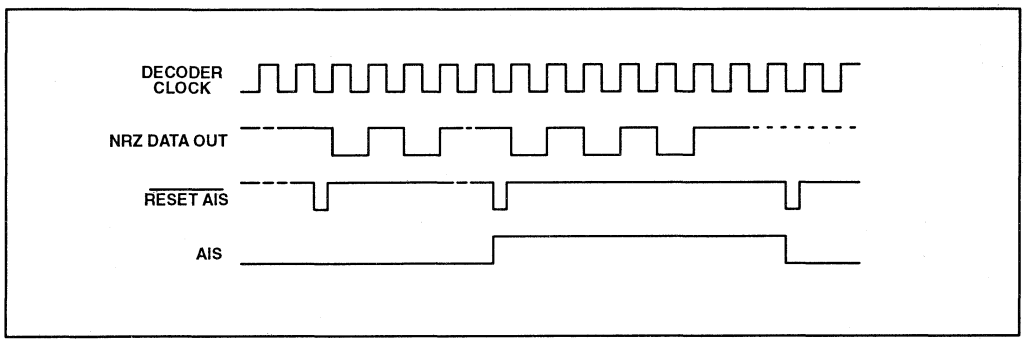


Fig. 7: AIS and RESET AIS waveforms

PIN DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	NRZ DATA IN	Input pin for data to be encoded into pseudo–ternary HDB3 form. This data is clocked into the Encoder block by the falling edge of ENCODER CLOCK.
2	ENCODER CLOCK	Clock input for the encoding of data on pin 1.
3	LOSS OF INPUT	Output from the loss of input circuit. This output goes high one clock period after the detection of eleven consecutive zeros on the decoder inputs. Any logic '1' at the input (RXD1 or RXD2 = 0) resets this count after a single clock period delay.
4	NRZ DATA OUT	NRZ data output obtained from the decoding of the pseudo–ternary inputs to the Decoder block.
5	DECODER CLOCK	Clock input to the Decoder block, for decoding data on RXD1 and RXD2, or TXD1 and TXD2 in loop test mode. In internal clock regeneration mode, this pin is used to output the regenerated clock to external circuitry. In external clock regeneration mode, this pin is used to input the externally regenerated clock signal direct to the Decoder block.
6	$\overline{\text{RESET AIS}}$	Reset input to the decoded zero counter. A logic '0' on this input resets a decoded zero counter. It will also reset the AIS output to '0' provided 3 or more zeros have been decoded in the preceding $\overline{\text{RESET AIS}}$ = 1 period, or set AIS to '1' if less than 3 zeros have been decoded in the preceding $\overline{\text{RESET AIS}}$ = 1 period. This may be used to indicate loss of timeslot zero. A logic '1' on this pin enables the decoded zero counter.
7	AIS	Output from AIS circuit (see description for pin 6).

8	MODE	Input pin for selection of clock regeneration mode. A logic high on this input selects internal crystal controlled clock regeneration whilst a logic low selects external clock regeneration.
9	GND	Digital ground. 0 Volts.
10	CRYSTAL IN	Input to crystal oscillator amplifier when in internal clock regeneration mode, with the crystal connected between pins 10 and 12. Alternatively, this pin may be used as the 16.384/12.352MHz input to the internal clock regeneration circuitry if one oscillator is shared between several decoders. This pin has no function when external clock regeneration is selected and should be tied to GND.
11	DOUBLE VIOLATION	Output from the error detector circuit. This output goes high for one period of Decoder clock, one period after the detection of a HDB3 violation of the same polarity as the previous HDB3 violation.
12	CRYSTAL OUT/CDR	In external clock regeneration mode, this pin is used to output the OR function of the two HDB3 inputs, RXD1 and RXD2 (or TXD1 and TXD2 if loop test mode is selected), to an external clock regeneration circuit. In internal clock regeneration mode, this is the output which forms the crystal oscillator with pin 10.
13	RXD1	HDB3 input 1 to Decoder block. This input asynchronously latches the incoming HDB3 encoded data and is falling edge sensitive.
14	LOOP TEST ENABLE	Input pin for selection of normal or loop back operation. A logic low on this pin selects normal operation, with encoder and decoder being independant and asynchronous. A logic high on this pin internally connects TXD1 to RXD1 and TXD2 to RXD2. Note that in loop back mode, a decoder clock must be supplied (or regenerated from pin 12) along with the encoder clock.
15	RXD2	HDB3 input 2 to Decoder block. See pin 13 description.
16	TXD1	HDB3 Encoded output 1 from Encoder block. This output goes high after the rising edge of clock if a mark is to be transmitted. The length of the pulse is set by the positive clock pulse width.
17	TXD2	HDB3 Encoded output 2. See pin 16 description.
18	VDD	Digital supply voltage. 5Volt ±10%.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{DD} = 5V ± 0.5V Ambient Temperature T_{amb} = −40°C to +85°C

STATIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low Level Input Voltage	V_{IL}	0		0.8	Volts	
High Level Input Voltage	V_{IH}	2.0		V_{DD}	Volts	
Low Level Output Voltage	V_{OL}			0.4	Volts	I_{SINK} = 2mA
High Level Output Voltage	V_{OHT} V_{OHC}	2.4 V_{DD} −1.0			Volts Volts	I_{SOURCE} = 2mA I_{SOURCE} =1mA
Input Leakage Current	I_{IN}	−10		+200	µAmp	V_{IN} = V_{DD} or GND
Supply Current	I_S			15	mAmps	1.544/2.048MHz Operation with Internal clock regeneration, Note 1.
				5	mAmps	1.544/2.048MHz Operation with External clock regeneration, Note 1.
				15	mAmps	8.448MHz Operation, Note 1.
Input Capacitance	C_{IN}		5		pF	All Inputs
Output Capacitance	C_{OUT}		5		pF	All Outputs

Notes:– 1. All supply currents specified with outputs unloaded. These currents are not tested but are guaranteed by characterisation and a static current test.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{DD} = 5V ± 0.5V Ambient Temperature T_{amb} = –0°C to +70°C

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Clock Period	T_{CP}	100			nS	Refer Fig. 8
Clock Rise/Fall Time	T_{CR}/T_{CF}			20	nS	Refer Fig. 8
Clock High/Low time	T_{CH}/T_{CL}	30			nS	Refer Fig. 8
Encoder Data Setup Time	T_{EDS}	10			nS	Refer Fig. 9
Encoder Data Hold Time	T_{EDH}	10			nS	Refer Fig. 9
TXD1/TXD2 Output Propagation Delay	T_{EPDR}/T_{EPDF}			45	nS	Note 1, refer Fig. 9
CDR Propagation Delay	T_{CPDR}/T_{CPDF}			40	nS	Note 1, refer Fig. 10
RXD1/2 Data Setup Time	T_{RS}	15			nS	Refer Fig. 10
RXD1/2 Pulse Width	T_{RW}	20			nS	Refer Fig. 10
Decoder Output Propagation Delay	T_{OPD}			45	nS	Notes 1 and 2, refer Fig. 10
$\overline{\text{RESET AIS}}$ Hold Off Time	T_{RAHO}	10			nS	Refer Fig. 10
$\overline{\text{RESET AIS}}$ Pulse Width	T_{RAW}	15			nS	Refer Fig.10
$\overline{\text{RESET AIS}}$ Setup Time	T_{RAS}	10			nS	Refer Fig. 10
AIS Output Propagation Delay	T_{APD}			45	nS	Note 1, refer Fig. 10

Notes:– 1. All propagation delays are measured with the relevant output loaded with a 50pF capacitor.
2. T_{OPD} applies to outputs NRZ DATA OUT, LOSS OF INPUT and DOUBLE VIOLATION, but does not apply to AIS.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{DD} = 5V ± 0.5V Ambient Temperature T_{amb} = –40°C to +85°C

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Clock Period	T_{CP}	100			nS	Refer Fig. 8
Clock Rise/Fall Time	T_{CR}/T_{CF}			20	nS	Refer Fig. 8
Clock High/Low time	T_{CH}/T_{CL}	35			nS	Refer Fig. 8
Encoder Data Setup Time	T_{EDS}	20			nS	Refer Fig. 9
Encoder Data Hold Time	T_{EDH}	20			nS	Refer Fig. 9
TXD1/TXD2 Output Propagation Delay	T_{EPDR}/T_{EPDF}			50	nS	Note 1, refer Fig. 9
CDR Propagation Delay	T_{CPDR}/T_{CPDF}			45	nS	Note 1, refer Fig. 10
RXD1/2 Data Setup Time	T_{RS}	20			nS	Refer Fig. 10
RXD1/2 Pulse Width	T_{RW}	25			nS	Refer Fig. 10

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Decoder Output Propagation Delay	T_{OPD}			50	nS	Notes 1 and 2, refer Fig. 10
$\overline{\text{RESET AIS}}$ Hold Off Time	T_{RAHO}	15			nS	Refer Fig. 10
$\overline{\text{RESET AIS}}$ Pulse Width	T_{RAW}	20			nS	Refer Fig.10
$\overline{\text{RESET AIS}}$ Setup Time	T_{RAS}	15			nS	Refer Fig. 10
AIS Output Propagation Delay	T_{APD}			55	nS	Note 1, refer Fig. 10

Notes:– 1. All propagation delays are measured with the relevant output loaded with a 50pF capacitor.
2. T_{OPD} applies to outputs NRZ DATA OUT, LOSS OF INPUT and DOUBLE VIOLATION, but does not apply to AIS.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

$+V_{DD}$	–0.5 to +7V
Inputs	V_{DD} + 0.5V to GND –0.5V
Outputs	V_{DD} +0.5V to GND –0.5V
Storage temperature	Plastic –55 to +125°C
	Ceramic –65 to +150°C

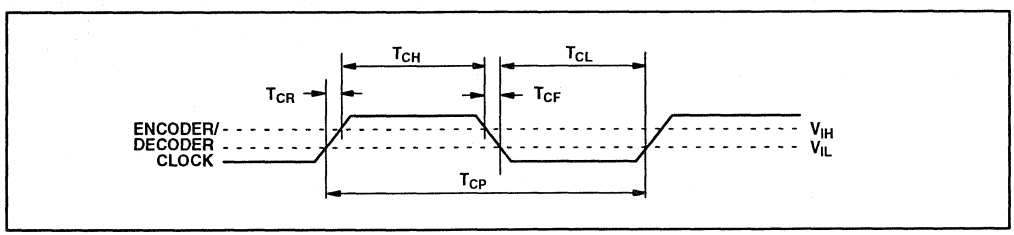


Fig. 8: Clock timing parameters

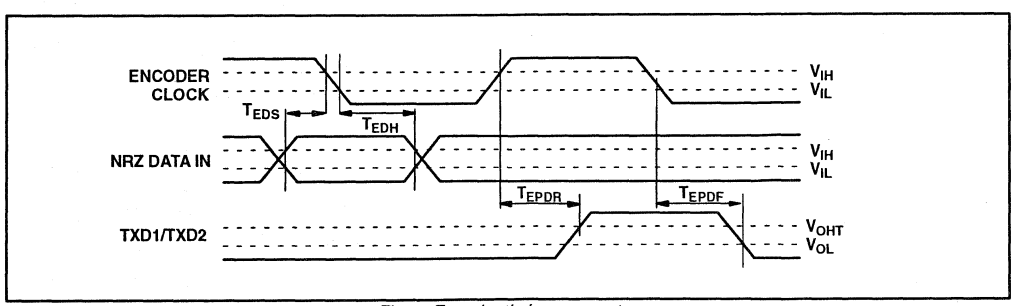


Fig. 9: Encoder timing parameters

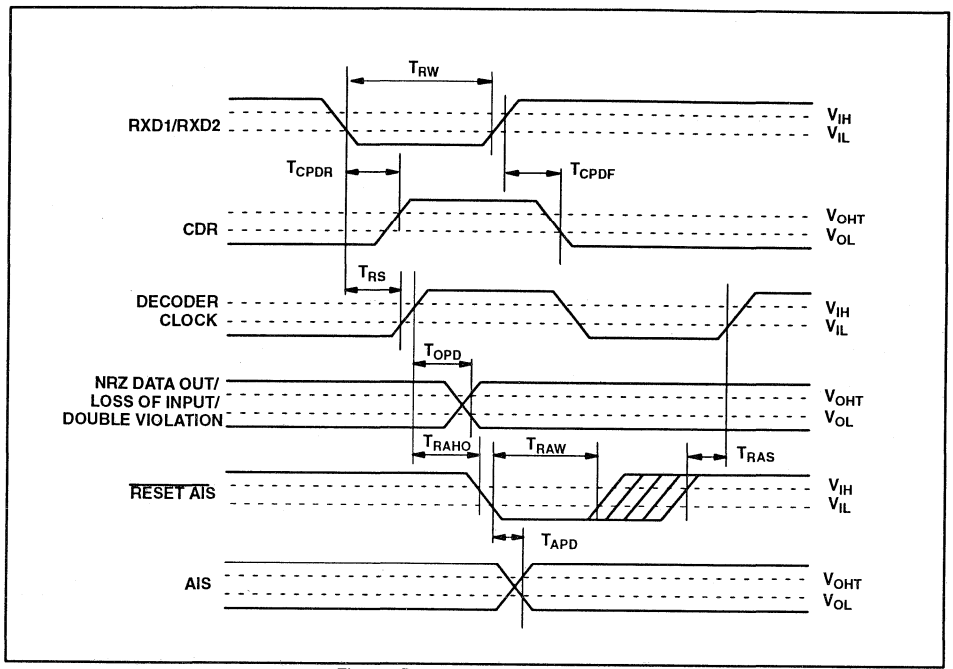


Fig. 10: Decoder timing parameters

MV1443

PCM TIMESLOT ZERO TRANSMITTER AND RECEIVER

The MV1443 combines the Timeslot Zero Transmitter and Receiver functions required by a 2.048Mbit 30 channel PCM transmission link operating in accordance with the appropriate CCITT Recommendations and forms part of the GPS 2Mbit PCM signalling series of devices. The circuit is fabricated in CMOS and operates from a single +5V supply with all inputs and outputs being TTL compatible.

The Timeslot Zero Transmitter half of the circuit is responsible for generating the timeslot zero synchronising word of a 2Mbit PCM link in accordance with CCITT Recommendation G.704. This function is performed by alternately generating sync frames, containing the CCITT Frame Alignment Signal, and non-sync frames containing user data bits.

The Timeslot Zero Receiver function searches for the CCITT Frame Alignment signal in the incoming data stream and when this is present the receiver synchronises itself to this pattern in accordance with the Frame Alignment strategy detailed in CCITT Recommendation G.732. Once frame alignment has been achieved the Timeslot Zero Receiver produces various timing outputs for the use of external circuitry and extracts the user data bits of timeslot zero.

FEATURES

- Single +5V supply.
- All Inputs and Outputs TTL compatible.
- Transmitter generates Frame Alignment Signal in accordance with CCITT Recommendation G.704.
- Enables access to User Data Bits of Timeslot Zero.
- Receiver Frame Synchronisation carried out in accordance with CCITT Recommendation G.732.
- Provides Alarm Outputs for Reception of Corrupted Alignment word and Loss of Frame Alignment.
- Extracts the International Spare Bits from Alternate Frames or from Frames 13 and 15 of the CCITT CRC multiframe.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

ELECTRICAL RATINGS

Supply Voltage	-0.5V to +7V
Input Voltage	-0.5V to VDD +0.5V
Output Voltage	-0.5V to VDD +0.5V

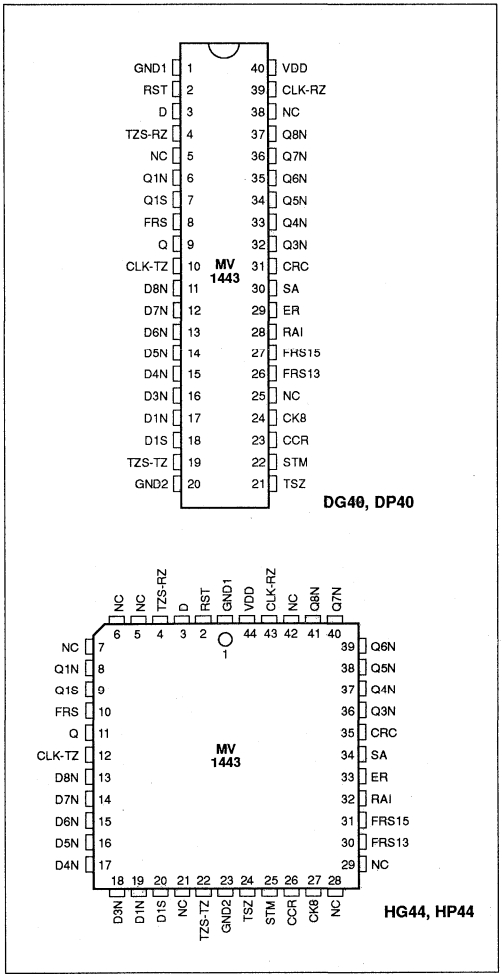


Fig. 1 Pin connections - top view

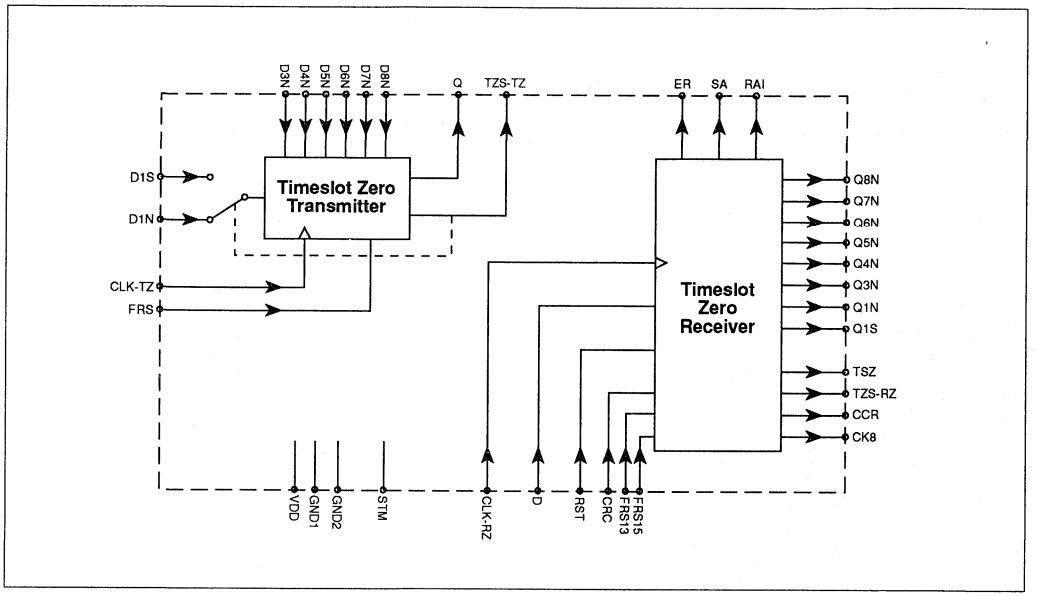


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The MV1443 combines the Timeslot Zero Transmitter and Receiver functions required by a 2.048Mbit 30 channel PCM transmission link operating in accordance with the appropriate CCITT Recommendations. The block diagram of the MV1443 is shown in Fig.2 and the function of each block is now described separately.

Timeslot Zero Transmitter

The Timeslot Zero Transmitter circuit generates the timeslot zero synchronising word required by a 2.048Mbit PCM link in accordance with CCITT Recommendation G.704. During alternate frames, denoted sync frames, the CCITT Frame Alignment Signal (FAS - 0011011) is combined with the International / CRC data bit input, D1S, for bit 1 and injected on to the PCM highway via the Q output. During the other interleaved frames, denoted non-sync frames, bit 2 of timeslot zero is set to '1' to avoid imitation of the FAS and this is combined with the second International / CRC data bit, D1N, for bit 1 and the user data bits, D3N-D8N, for bits 3 to 8, and again injected on to the PCM highway.

In order to perform this function the Timeslot Zero Transmitter requires 2 timing inputs in addition to the parallel data bit inputs, pins CLK-TZ and FRS. The CLK-TZ input is a 2.048MHz clock input whilst FRS is a high going pulse, 8 clock periods long, which is required to mask timeslot zero of each frame. In addition to the PCM data stream output the Timeslot Zero Transmitter produces a timing output, TZS-TZ, which changes state one clock period after the end of Timeslot Zero and is high during the transmission of timeslot zero of sync frames.

The timing diagram of the Timeslot Zero Transmitter circuit is shown in Fig.3.

Timeslot Zero Receiver

The Timeslot Zero Receiver circuit is responsible for searching for and locking on to the CCITT Frame Alignment Signal present in timeslot zero of the PCM data stream being clocked in to its D input. This process is carried out in accordance with the loss and recovery of frame alignment strategy described in CCITT Recommendation G.732. Once frame alignment has been achieved the Timeslot Zero Receiver circuit outputs various timing reference signals for the synchronisation of external circuitry. These timing outputs will all free run if frame synchronisation is subsequently lost. In addition, a control input, RST, may be used to reset this synchronisation process, forcing the receiver out of frame alignment.

The Timeslot Zero Receiver circuit produces 4 timing outputs for use by external circuitry if required. The first of these timing outputs is TSZ which is an 8 clock period long, high going pulse masking the position of timeslot zero, similar to the FRS input of the Timeslot Zero Transmitter, and facilitates the frame alignment of external circuitry. The second timing output, TZS-RZ, is a 4KHz signal which changes state once per frame, one clock period after the end of timeslot zero, and is high during sync frames to allow sync and non-sync frames to be distinguished. The third timing output, CCR, is a low going pulse, one clock period wide, occurring during 1 bit, timeslot 1 of sync frames. The final timing output, CK8, is an 8KHz signal going low at the end of bit 7 of each timeslot zero and high at the end of bit 7 in each timeslot 16.

In addition to these timing outputs, two alarm outputs are provided to indicate errors in the incoming data stream. The first of these alarms, ER, goes high for one frame following a sync frame in which a corrupted FAS was detected when the receiver is in sync. Three consecutive alarms of this type will put the receiver out of sync. The second alarm, SA, goes high to indicate that the Timeslot Zero Receiver is out of frame alignment.

In addition to the frame synchronisation process, the Timeslot Zero Receiver is also responsible for extracting the user data bits of non-sync words and the two International / CRC bits of timeslot zero. The user data bits present in bits 3 to 8 of timeslot zero of non-sync frames are extracted and output on the Q3N-Q8N parallel data outputs. The third bit of non-sync words, Q3N, is used as the remote alarm bit in 2Mbit PCM systems and a third alarm output, RAI, is derived from this bit. This alarm is a persistence checked version of Q3N which goes high when two consecutive Q3N bits have been received high whilst the receiver is in sync. The Timeslot Zero Receiver also extracts the data present in bit 1 of timeslot zero under control of the CRC input. This input selects between CCITT CRC-4 and non-CRC-4 modes of operation. In non-CRC-4 mode, the international spare bits are extracted from bit 1 of all sync and non-sync frames and output on pins Q1S and Q1N respectively. In CRC-4 mode, these data outputs are extracted from bit 1 of frames 13 and 15 of the CCITT CRC-4 multiframe structure respectively. In order to accomplish this, two timing inputs, FRS13 and FRS15, are required in CRC-4 mode. These inputs are required to be high during bit 8 of the appropriate frame, low during bit 8 of any other non-sync frame and any state elsewhere. The timing diagrams for the Timeslot Zero Receiver are shown in Fig.4

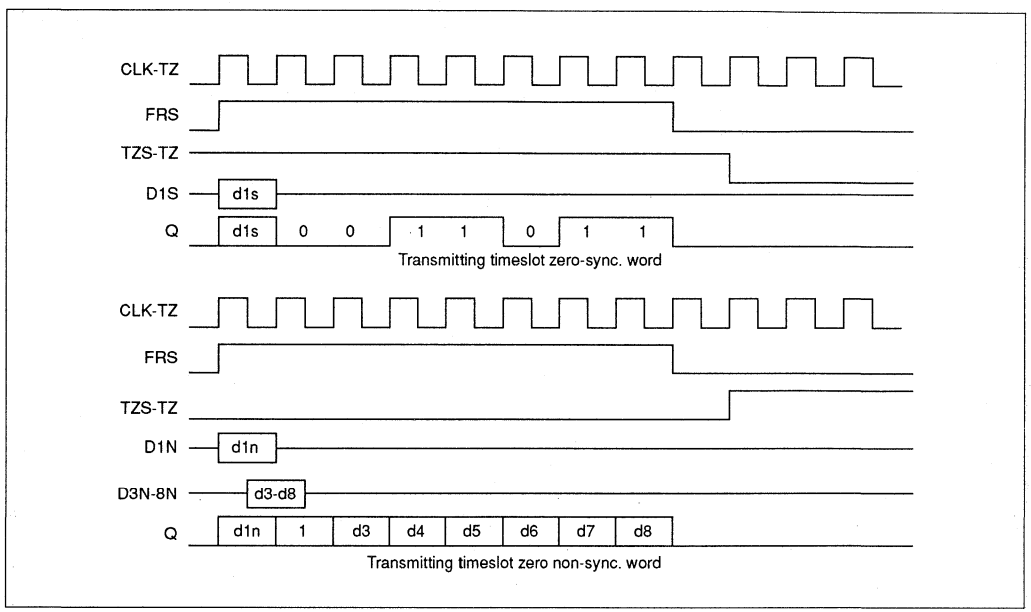


Fig. 3 Timeslot zero transmitter timing

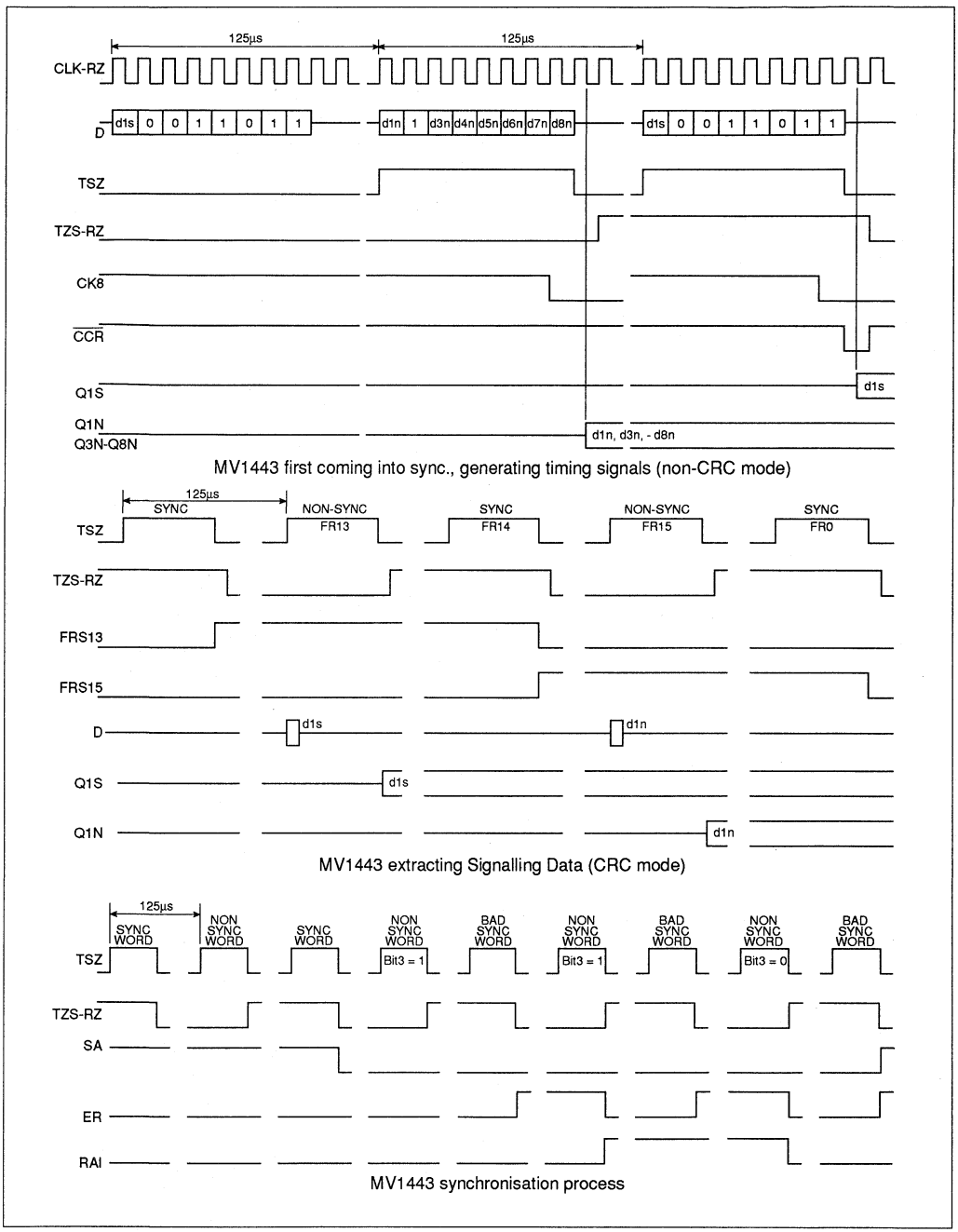


Fig. 4 Timeslot zero receiver timing

PIN DESCRIPTIONS

Pin name	Pin Number		Pin Description
	DG40	HG44	
GND1	1	1	Digital Ground. 0V (Note 1)
RST	2	2	Reset Input to Timeslot Zero Receiver. A logic high on this pin straddling a falling edge of CLK-RZ will reset the state machine of the Timeslot Zero Receiver, forcing it out of frame alignment.
D	3	3	PCM Data Stream Input to Timeslot Zero Receiver. This pin is used to input the 2.048Mbit PCM data stream to the Timeslot Zero Receiver and it is this data stream which is searched for the Frame Alignment Signal. This input is latched by the falling edge of CLK-RZ.
TZS-RZ	4	4	Timeslot Zero Sync Frame Output from Timeslot Zero Receiver. This 4KHz output changes state at the end of bit 1, timeslot 1 (Note 2) of every frame and is high during timeslot zero of sync frames.
Q1N	6	8	International / CRC Data Bit Output of Timeslot Zero Receiver for Non-sync Frames. With CRC=0, this output latches data from bit 1, timeslot zero of non-sync frames. With CRC=1, this output latches data from bit 1, timeslot zero of frame 15 of the CRC-4 multiframe, under control of the FRS15 input. In either case this output changes state on the falling edge of CLK-RZ, half a clock period after the end of timeslot zero.
Q1S	7	9	International / CRC Data Bit Output of Timeslot Zero Receiver for Sync Frames. With CRC=0, this output latches data from bit 1, timeslot zero of sync frames. With CRC=1, this output latches data from bit 1, timeslot zero of frame 13 of the CRC-4 multiframe, under control of the FRS13 input. In either case this output changes state on the falling edge of CLK-RZ, half a clock period after the end of timeslot zero.
FRS	8	10	Timeslot Zero Frame Sync Input of Timeslot Zero Transmitter. This input is required to be an 8 bit long, high going pulse masking timeslot zero. This input is latched by the falling edge of CLK-TZ although the first bit of timeslot zero is output asynchronously after the rising edge of FRS is detected.
Q	9	11	Timeslot Zero Data Stream Output of Timeslot Zero Transmitter. The sync and signalling data words produced by the Timeslot Zero Transmitter are output on this pin in 8 bit bursts during timeslot zero. During any other timeslot this output is held low. Bit 1 appears immediately after the rising edges of CLK-TZ and FRS.
CLK-TZ	10	12	2.048MHz Clock Input to Timeslot Zero Transmitter.
D8N D7N D6N D5N D4N D3N	11 12 13 14 15 16	13 14 15 16 17 18	User Data Bit Inputs to Timeslot Zero Transmitter. These 6 parallel data inputs are inserted by the Timeslot Zero Transmitter into bits 8-3 of timeslot zero during non-sync words. These inputs must be set up prior to the rising edge of CLK-TZ at the end of bit 1, timeslot zero of non-sync frames.

PIN DESCRIPTIONS (continued)

Pin name	Pin Number		Pin Description
	DG40	HG44	
D1N	17	19	International / CRC Data Bit Input to Timeslot Zero Transmitter for Non-Sync Frames. The data on this pin is output on the Q pin during bit 1, timeslot zero of non-sync frames and must be set up prior to the rising edge of FRS during non-sync frames.
D1S	18	20	International / CRC Data Bit Input to Timeslot Zero Transmitter for Sync Frames. The data on this pin is output on the Q pin during bit 1, timeslot zero of sync frames and must be set up prior to the rising edge of FRS during sync frames.
TZS-TZ	19	22	Timeslot Zero Sync Frame Output from Timeslot Zero Transmitter. This 4KHz output changes state at the end of bit 1, timeslot 1 of every frame and is high during timeslot zero of sync frames.
GND2	20	23	Digital Ground. 0V (Note 1)
TSZ	21	24	Timeslot Zero Marker Output from Timeslot Zero Receiver. This timing output goes high for the 8 clock periods of timeslot zero and is low at all other times.
STM	22	25	Scan Path Test Global Mode Pin. A logic high on this pin configures the MV1443 in scan test mode. For normal operation this pin should be tied low.
CCR	23	26	Channel Reset Timing Output from Timeslot Zero Receiver. This output pulses low for a single period during bit 1, timeslot 1 of sync frames.
CK8	24	27	8KHz Clock Output from Timeslot Zero Receiver. This output goes low at the beginning of bit 8, timeslot 0 and high at the beginning of bit 8, timeslot 16.
FRS13	26	30	Frame 13 Marker Input to Timeslot Zero Receiver. This input is used by the Timeslot Zero Receiver operating in CRC-4 mode to reference the position of Frame 13. This input is required to be high during bit 8, Frame 13 of the CRC multiframe and low during bit 8 of all other non-sync frames.
FRS15	27	31	Frame 15 Marker Input to Timeslot Zero Receiver. This input is used by the Timeslot Zero Receiver operating in CRC-4 mode to reference the position of Frame 15. This input is required to be high during bit 8, Frame 15 of the CRC multiframe and low during bit 8 of all other non-sync frames.
RAI	28	32	Remote Alarm Indication Output of Timeslot Zero Receiver. This alarm output is a persistence checked version of the Q3N output. When the receiver is in sync this output will go high if 2 consecutive Q3N bits are received high. This output changes state at the beginning of bit 1, timeslot 1 of non sync frames. When the receiver is out of sync this output is forced low in the non-sync frame following the last bad sync frame, and is held low until the receiver comes back in to sync.

PIN DESCRIPTIONS (continued)

Pin name	Pin Number		Pin Description
	DG40	HG44	
ER	29	33	Sync Word Error Output of Timeslot Zero Receiver. This alarm output goes high for one frame immediately after detection of a bad timeslot zero frame alignment signal, whilst the receiver is in sync. Three consecutive errors of this type will put the receiver out of sync and the last ER pulse of this sequence will be longer than 256 periods if a valid sync word is detected during the pulse.
SA	30	34	Synchronisation Alarm Output from Timeslot Zero Receiver. This output is high whenever the receiver is out of sync and only changes state at the beginning of bit 1, timeslot 1 of sync frames.
CRC	31	35	CRC-4 Mode Select Input to Timeslot Zero Receiver. This input is used to control the extraction of the Q1N and Q1S data outputs from the incoming PCM data stream. A logic high on this input selects CRC-4 mode of operation.
Q3N Q4N Q5N Q6N Q7N Q8N	32 33 34 35 36 37	36 37 38 39 40 41	User Data Bit Outputs of Timeslot Zero Receiver. These 6 parallel data outputs are extracted from bits 3-8 of timeslot zero during non-sync frames. These outputs change state on the falling edge of CLK-RZ half a clock period after the end of timeslot zero.
CLK-RZ	39	43	2.048MHz Clock Input to Timeslot Zero Receiver.
VDD	40	44	Digital Supply Voltage. 5V

NOTES

1. In order to facilitate adequate supply decoupling, both digital ground pins should be connected to 0V.
2. The bits of a timeslot are numbered from 1 to 8 whereas the timeslots of a frame are numbered from 0 to 31 and the frames of a CCITT multiframe are numbered from 0 to 15.
3. All inputs except STM have 100K on-chip pull down resistors. The STM pin has neither pull-up nor pull-down resistor and should be tied to digital ground during normal operation.

ELECTRICAL CHARACTERISTICS

Test Conditions:

Supply Voltage VDD = 5V ± 0.5V Ambient Temperature Tamb = -40°C to +85°C

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low Level Input Voltage	V_{IL}	0.0		0.8	V	
High Level Input Voltage	V_{IH}	2.0		V_{DD}	V	
Low Level Output Voltage	V_{OL}			0.4	V	Isink=2mA
High Level Output Voltage	V_{OHT}	2.4			V	Isource=2mA
	V_{OHC}	V—- 1.0			V	Isource=1mA
Input Leakage Current	I_{IL}	-10		200	uA	$V_{IN}=V_{DD}$ or V_{SS}
Input Capacitance	C_{IN}		5		pF	All Inputs
Output Capacitance	C_{OUT}		5		pF	All Outputs

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
CLOCK						
Clock Period	t_{CP}	400			ns	See Fig. 5
Clock Rise/Fall Time	t_{CR}/t_{CF}			20	ns	See Fig. 5
Clock High/LowTime	t_{CH}/t_{CL}	150			ns	See Fig. 5
TRANSMITTER						
FRS Rising Hold Time	t_{FRH}	50			ns	See Fig. 6
FRS Rising Setup Time	t_{FRS}	100			ns	See Fig. 6
FRS Falling Hold Time	t_{FFH}	100			ns	See Fig. 6
FRS Falling Setup Time	t_{FFS}	50			ns	See Fig. 6
International Data Bit Setup Time	t_{IDS}	50			ns	See Fig. 6
International Data Bit Hold Time	t_{IDH}	50			ns	See Fig. 6
User Data Setup Time	t_{UDS}	50			ns	See Fig. 6
User Data Hold Time	t_{UDH}	50			ns	See Fig. 6
Q Propagation Delay from FRS (bit 1, TS0)	t_{QPDF}			60	ns	See Fig. 6, Note 1.
Q Propagation Delay from CLK-RZ (bits 2-8	t_{QPDC}			60	ns	See Fig. 6, Note 1.
TZS-TZ Propagation Delay	t_{TTPD}			60	ns	See Fig. 6, Note 1.
RECEIVER						
Data / Control Setup Time	t_{DS}	50			ns	See Fig. 7, Note 2.
Data / Control Hold Time	t_{DH}	50			ns	See Fig. 7, Note 2.
Timing / Alarm Propagation Delay	t_{TAPD}			60	ns	See Fig. 7, Notes 1 and 3.
Data Outputs Propagation Delay	t_{DPD}			75	ns	See Fig. 7, Notes 1 and 4.

NOTES

1. All output propagation delays are measured with a 50pF load.

2. The Timeslot Zero Receiver Data / Control setup and hold time parameters, t_{DS} and t_{DH}, apply to the following inputs: D, RST, FRS13 and FRS15.

3. The Timeslot Zero Receiver Timing / Alarm Output propagation delay parameter applies to the following outputs: TSZ, TZS, CCR, CK8, ER, SA and RAI.

4. The Timeslot Zero Receiver Data Output propagation delay parameter applies to the following outputs: Q1S, Q1N, Q3N, Q4N, Q5N, Q6N, Q7N and Q8N.

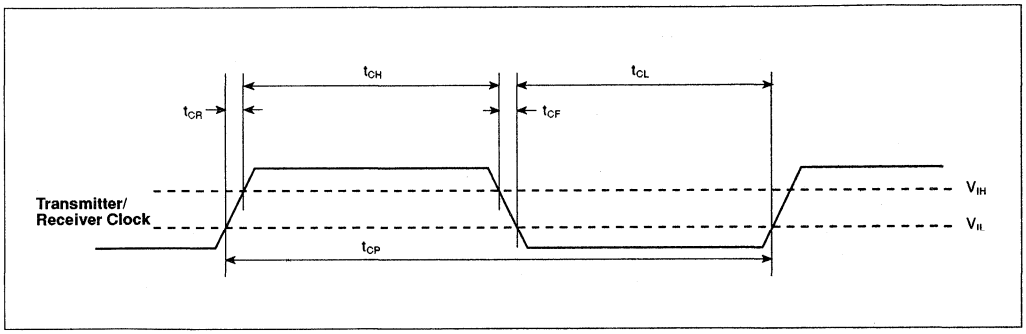


Fig. 5 Clock Timing Parameters

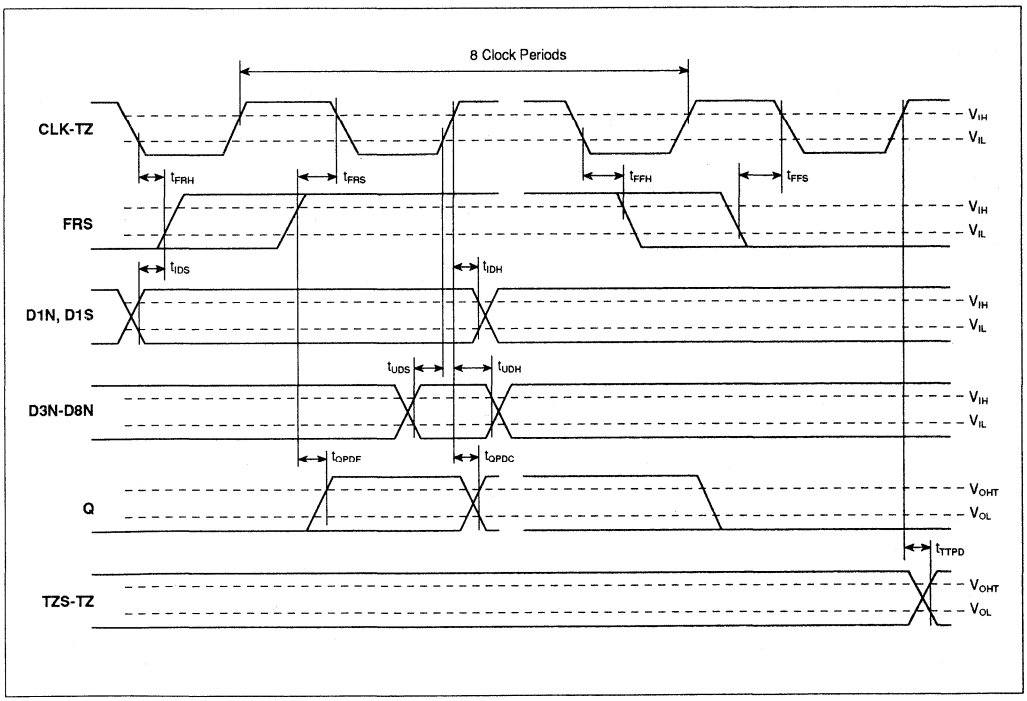


Fig. 6 Timeslot Zero Transmitter Timing

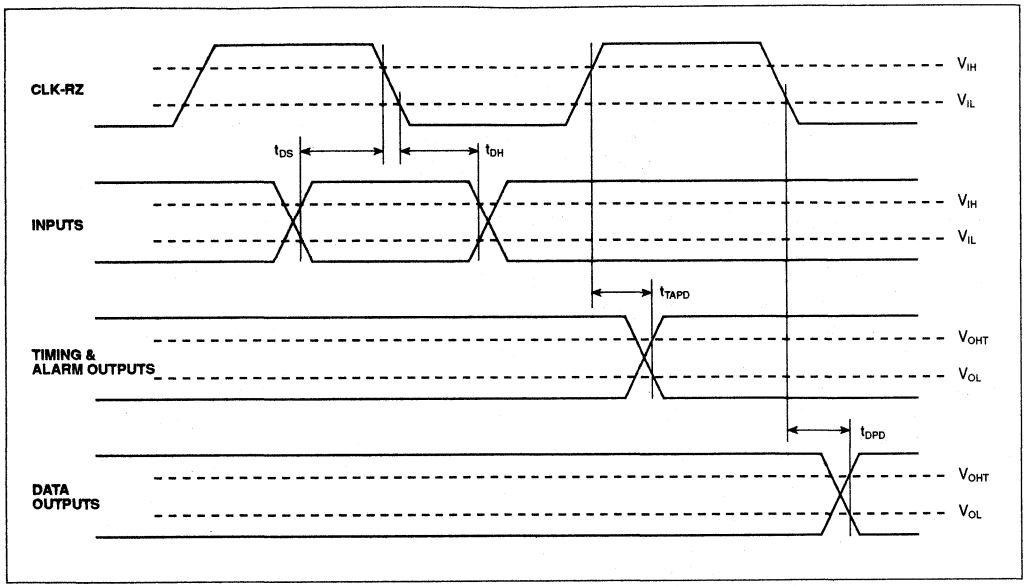


Fig. 7 Timeslot Zero Receiver Timing

ORDERING INFORMATION

MV1443/IG/DGAS
MV1443/IG/DPAS
MV1443/IG/HGAS
MV1443/IG/HPAS

MV1444

COMBINED PCM TIMESLOT ZERO TRANSMITTER AND HDB3 ENCODER

The MV1444 combines the Timeslot Zero Transmitter and HDB3 Encoder functions required by a 2.048Mbit 30 channel PCM transmission link operating in accordance with the appropriate CCITT Recommendations and forms part of the GPS 2Mbit PCM signalling series of devices. The circuit is fabricated in CMOS and operates from a single +5V supply with all inputs and outputs being TTL compatible.

The Timeslot Zero Transmitter half of the circuit is responsible for generating the timeslot zero synchronising word of a 2Mbit PCM link in accordance with CCITT Recommendation G.704. This function is performed by alternately generating sync frames, containing the CCITT Frame Alignment Signal, and non-sync frames containing user data bits.

The data being output from the Timeslot Zero Transmitter is multiplexed together with data for the remaining 31 timeslots by the transmission multiplexer and the PCM data stream thus created is fed in to the HDB3 Encoder.

The HDB3 Encoder half of the circuit is responsible for converting the incoming PCM data stream from the transmission multiplexer from NRZ form in to pseudo-ternary HDB3 transmission code for transmission over a 2Mbit PCM link. This process is carried out in accordance with Annex A to CCITT Recommendation G. 703 and ensures adequate clock recovery at the PCM receiver.

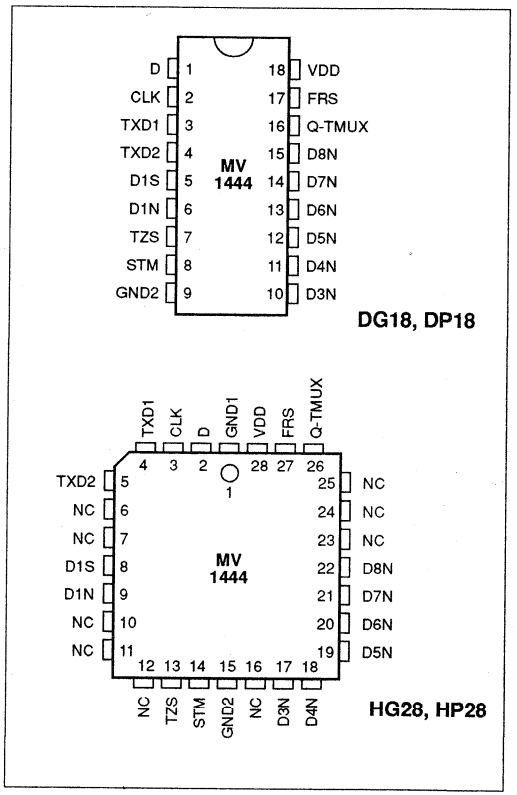


Fig. 1 Pin connections - top view

FEATURES

- Single +5V supply.
- All Inputs and Outputs TTL compatible.
- Timeslot Zero Transmitter generates Frame Alignment Signal in accordance with CCITT Recommendation G.704.
- Enables access to 6 User data bits and 2 International data bits of Timeslot Zero.
- On-chip Transmission Multiplexer allows combination of Timeslot Zero data with remaining 31 Timeslots of data.
- HDB3 Encoding carried out in Accordance with Annex A to CCITT Recommendation G.703.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

ELECTRICAL RATINGS

Supply Voltage	-0.5V to +7V
Input Voltage	-0.5V to VDD +0.5V
Output Voltage	-0.5V to VDD +0.5V

ORDERING INFORMATION

MV1444/IG/DGAS
MV1444/IG/DPAS
MV1444/IG/HGAS
MV1444/IG/HPAS

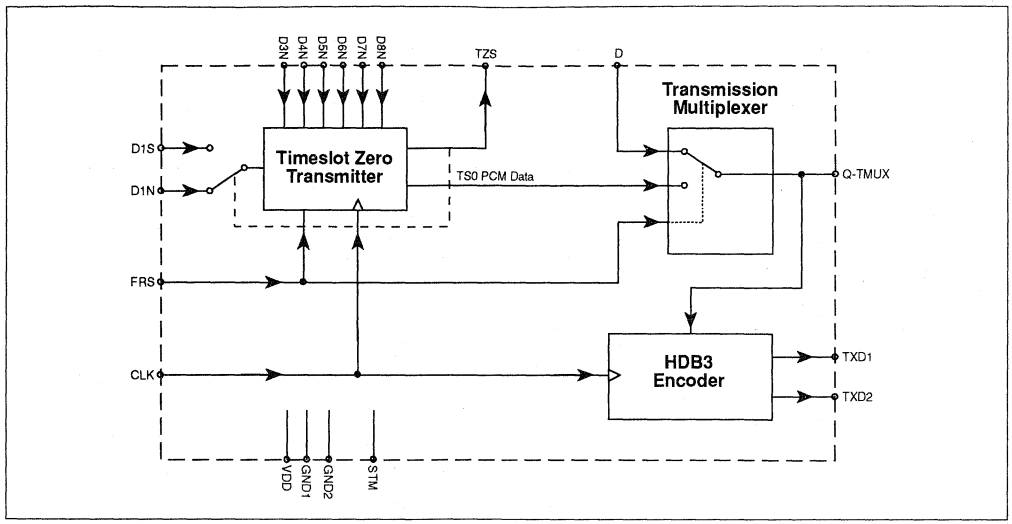


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The MV1444 combines the Timeslot Zero Transmitter, Transmission Multiplexer and HDB3 Encoder functions required by a 2.048Mbit 30 channel PCM transmission link operating in accordance with the appropriate CCITT Recommendations. The block diagram of the MV1444 is shown in Fig. 2, and the function of each block is now described separately.

Timeslot Zero Transmitter

The Timeslot Zero Transmitter circuit generates the timeslot zero synchronising word required by a 2.048Mbit PCM link in accordance with CCITT Recommendation G.704. During alternate frames, denoted sync frames, the CCITT Frame Alignment Signal (FAS - 0011011) is combined with the International / CRC data bit input, D1S, for bit 1 and injected in to the transmission multiplexer for HDB3 Encoding. During the other interleaved frames, denoted non-sync frames, bit 2 of timeslot zero is set to '1' to avoid imitation of the FAS and this is combined with the second International / CRC data bit, D1N, for bit 1 and the user data bits, D3N-D8N, for bits 3 to 8, and again output to the transmission multiplexer.

In order to perform this function the Timeslot Zero Transmitter requires 2 timing inputs in addition to the parallel data bit inputs, pins CLK and FRS. The CLK input is a 2.048MHz clock input whilst FRS is a high going pulse, 8 clock periods long, which is required to mask timeslot zero of each frame. In addition to the PCM data stream output the Timeslot Zero Transmitter produces a timing output, TZS, which changes state one clock period after the end of Timeslot Zero and is high during the transmission of timeslot zero of sync frames. The timing diagram of the entire MV1444 is shown in Fig.3.

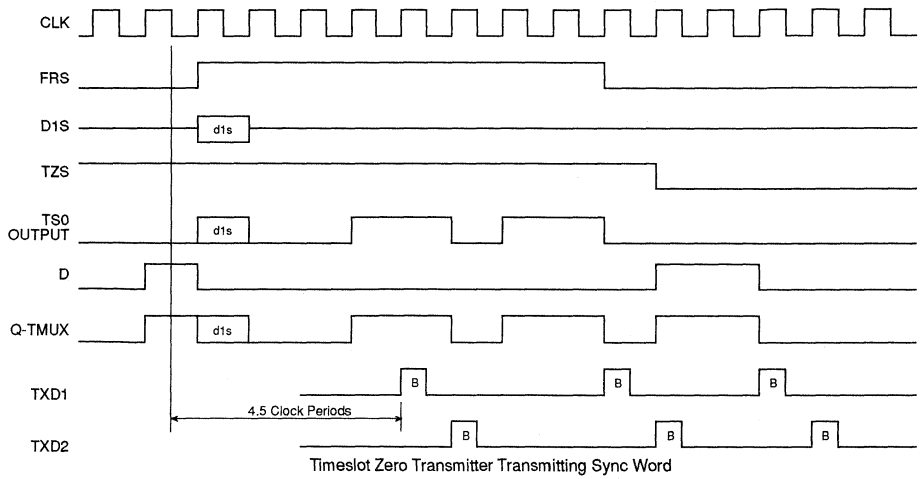
Transmission Multiplexer

The Transmission Multiplexer circuit mutiplexes together the output from the Timeslot Zero Transmitter with the PCM data stream for the remaining 31 timeslots being input on the D pin. This multiplexing is carried out under control of the FRS input such that the output from the Timeslot Zero Transmitter is selected whenever FRS is high. The output from the transmission multiplexer is input to the HDB3 Encoder and is also available as a device output on the Q-TMUX pin.

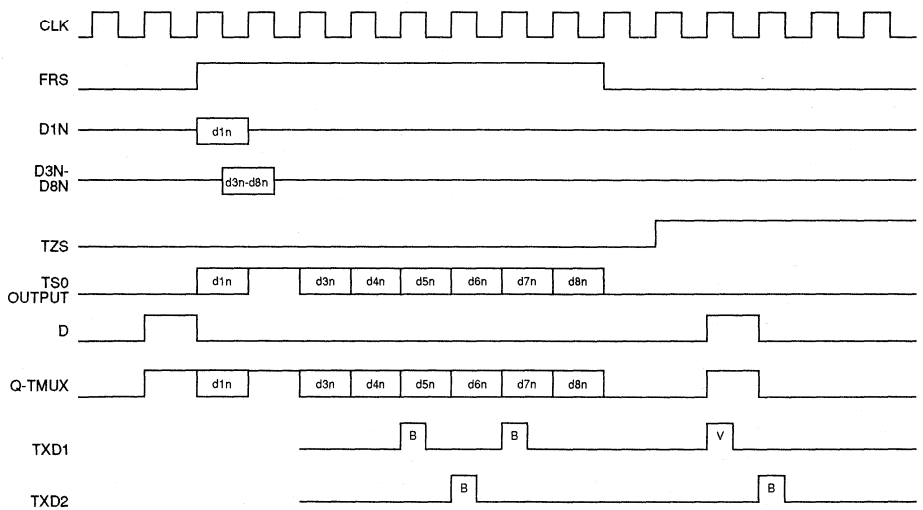
HDB3 Encoder

The HDB3 Encoder is responsible for converting the NRZ data being output by the transmission multiplexer into pseudo-ternary form for transmission over a 2.048Mbit PCM link. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703, Annex A.

High Density Bipolar 3 (HDB3) is a ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to ensure adequate clock recovery at the receiver. In any sequence of four consecutive binary zeroes, the last zero is substituted by a mark of the same polarity of the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code and ensures that successive violations alternate in polarity and as such introduce no DC component to the HDB3 signal. The data to be encoded is the PCM data stream being output by the transmission multiplexer and this is latched into the HDB3 Encoder by the falling edge of CLK. The HDB3 Encoder has two outputs, TXD1 and TXD2, which represent the HDB3 encoded PCM data stream in pseudo-ternary form. If a mark or violation is to be transmitted the output pulses high after the rising edge of clock, with the length of the pulse set by the clock high pulse width.



Timeslot Zero Transmitter Transmitting Sync Word



Timeslot Zero Transmitter Transmitting Non-sync Word

NOTES

1) The encoded HDB3 outputs, TXD1/2 are delayed by 4.5 clock periods with respect to Q-TMUX.
2) B is a mark, V is a HDB3 violation.
3) The TXD outputs are produced under the assumption that d1s=d1n=1, d3n-d8n=0.
4) Both diagrams assume the last mark and last violation occured on TXD2.

Fig. 3 MV1444 Timing diagrams

PIN DESCRIPTIONS

Pin name	Pin no.		Pin description
	DG18	HG28	
GND1	-	1	Digital Ground. OV (Note 1)
D	1	2	2.048Mbit PCM Voice Channel Input to Transmission Multiplexer. Data on this pin is input to the transmission multiplexer during timeslots 1-31 of a CCITT PCM frame for HDB3 encoding. After multiplexing this data is latched in to the HDB3 Encoder by the falling edge of CLK.
CLK	2	3	2.048MHz System Clock Input to Timeslot Zero Transmitter and HDB3 Encoder.
TXD1	3	4	HDB3 Encoded Pseudo-Ternary Output 1 from HDB3 Encoder. The PCM data stream produced by the transmission multiplexer is HDB3 encoded and output on this pin and pin TXD2. This output is always low during the low half cycle of clock and is only high during the high half cycle of clock if a mark is to be output. There is a 4.5 clock period delay from the falling edge of CLK to TXD1.
TXD2	4	5	HDB3 Encoded Pseudo-Ternary Output 2 from HDB3 Encoder. See Pin TXD1 description.
D1S	5	8	International / CRC Data Bit Input to Timeslot ZeroTransmitter for Sync Frames. The data on this pin is output to the transmission multiplexer during bit 1, timeslot zero of sync frames and must be set up prior to the rising edge of FRS during sync frames.
D1N	6	9	International / CRC Data Bit Input to Timeslot Zero Transmitter for Non-Sync Frames. The data on this pin is output to the transmission multiplexer during bit 1, timeslot zero of non-sync frames and must be set up prior to the rising edge of FRS during non-sync frames.
TZS	7	13	Timeslot Zero Sync Frame Output from Timeslot Zero Transmitter. This 4KHz output changes state at the end of bit 1, timeslot 1 (Note 2) of every frame and is high during timeslot zero of sync frames.
STM	8	14	Scan Path Test Global Mode Pin. A logic high on this pin configures the MV1444 in scan test mode. For normal operation this pin should be tied low.
GND2	9	15	Digital Ground. OV (Note 1)

PIN DESCRIPTIONS (continued)

Pin name	Pin no.		Pin description
	DG18	HG28	
D3N D4N D5N D6N D7N D8N	10 11 12 13 14 15	17 18 19 20 21 22	User Data Bit Inputs to Timeslot Zero Transmitter. These 6 parallel data inputs are inserted by the Timeslot Zero Transmitter into bits 8-3 of timeslot zero during non-sync words. These inputs must be set up prior to the rising edge of CLK at the end of bit 1, timeslot zero of non-sync frames.
Q-TMUX	16	26	PCM Data Stream Output from Transmission Multiplexer. During Timeslot Zero this output represents the data stream being produced by the Timeslot Zero Transmitter. During any other timeslot it represents the data being input on the D pin.
FRS	17	27	Timeslot Zero Frame Sync Input of Timeslot ZeroTransmitter and Transmission Multiplexer. This input is required to be an 8 bit long, high going pulse masking timeslot zero. This input is latched by the falling edge of CLK although the first bit of timeslot zero is output asynchronously immediately after the rising edge of FRS. This input is also used as the select input to the transmission multiplexer,which selects the output of the Timeslot zero transmitter as long as FRS is high, the D input whenever FRS is low.
V_{DD}	18	28	Digital Supply Voltage. 5 Volt ±10%

NOTES

1. In order to aid adequate supply decoupling, both digital ground pins of the HG28 and HP28 variants should be connected to 0V.
2. The bits of a timeslot are numbered from 1 to 8 whereas the timeslots of a frame are numbered from 0 to 31 and the frames of a CCITT multiframe are numbered from 0 to 15.
3. All inputs have 100K on-chip pull down resistors.

ELECTRICAL CHARACTERISTICS TEST CONDITIONS:

Supply Voltage VDD = 5V ± 0.5V Ambient Temperature T_{amb} = -40°C to +85°C

STATIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low Level Input Voltage	V_{IL}	0.0		0.8	V	
High Level Input Voltage	V_{IH}	2.0		V_{DD}	V	
Low Level Output Voltage	V_{OL}			0.4	V	Isink=2mA
High Level Output Voltage	V_{OHT}	2.4			V	Isource=2mA
	V_{OHC}	V_{DD}-1.0			V	Isource=lmA
Input Leakage Current	I_{IL}	-10		200	uA	Vin=V_{DD} or V_{SS}
Input Capacitance	C_{IN}		5		pF	All Inputs
Output Capacitance	C_{OUT}		5		pF	All Outputs

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Clock Period	t_{CP}	400			ns	See Fig. 4
Clock Rise/Fall Time	t_{CR}/t_{CF}			20	ns	See Fig. 4
Clock High/Low Time	t_{CH}/t_{CL}	150			ns	See Fig. 4
FRS Rising Hold Time	t_{FRH}	100			ns	See Fig. 5
FRS Rising Setup Time	t_{FRS}	100			ns	See Fig. 5
FRS Falling Hold Time	t_{FFH}	100			ns	See Fig. 5
FRS Falling Setup Time	t_{FFS}	100			ns	See Fig. 5
International Data Bit Setup Time	t_{IDS}	50			ns	See Fig. 5
International Data Bit Hold Time	t_{IDH}	70			ns	See Fig. 5
User Data Setup Time	t_{UDS}	50			ns	See Fig. 5
User Data Hold Time	t_{UDH}	50			ns	See Fig. 5
TZS Propagation Delay	t_{SFPD}			60	ns	See Fig. 5, Note 1.
PCM Data Setup Time	t_{PDS}	50			ns	See Fig. 5
PCM Data Hold Time	t_{PDH}	50			ns	See Fig. 5
Q-TMUX Propagation Delay from FRS (for bit 1, TS0)	t_{QPDF}			70	ns	See Fig. 5, Note 1.
Q-TMUX Propagation Delay from CLK (for bits 2-8, TS0)	t_{QPDC}			75	ns	See Fig. 5, Note 1.
Q-TMUX Propagation Delay from D (for Timeslots 1-31)	t_{QPDD}			60	ns	See Fig. 5, Note 1.
TXD1/2 Output Propagation Delay	t_{TPDR}/ t_{TPDF}			60	ns	See Fig. 5, Note 1.

NOTES

1. All output propagation delays are measured with a 50pF load.

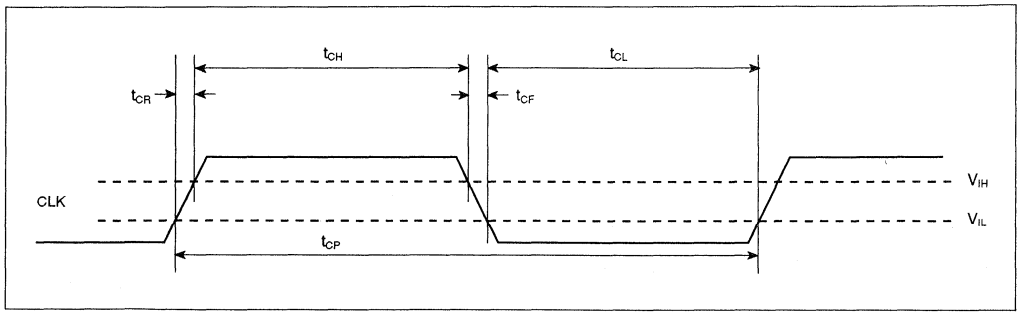


Fig. 4 Clock timing parameters

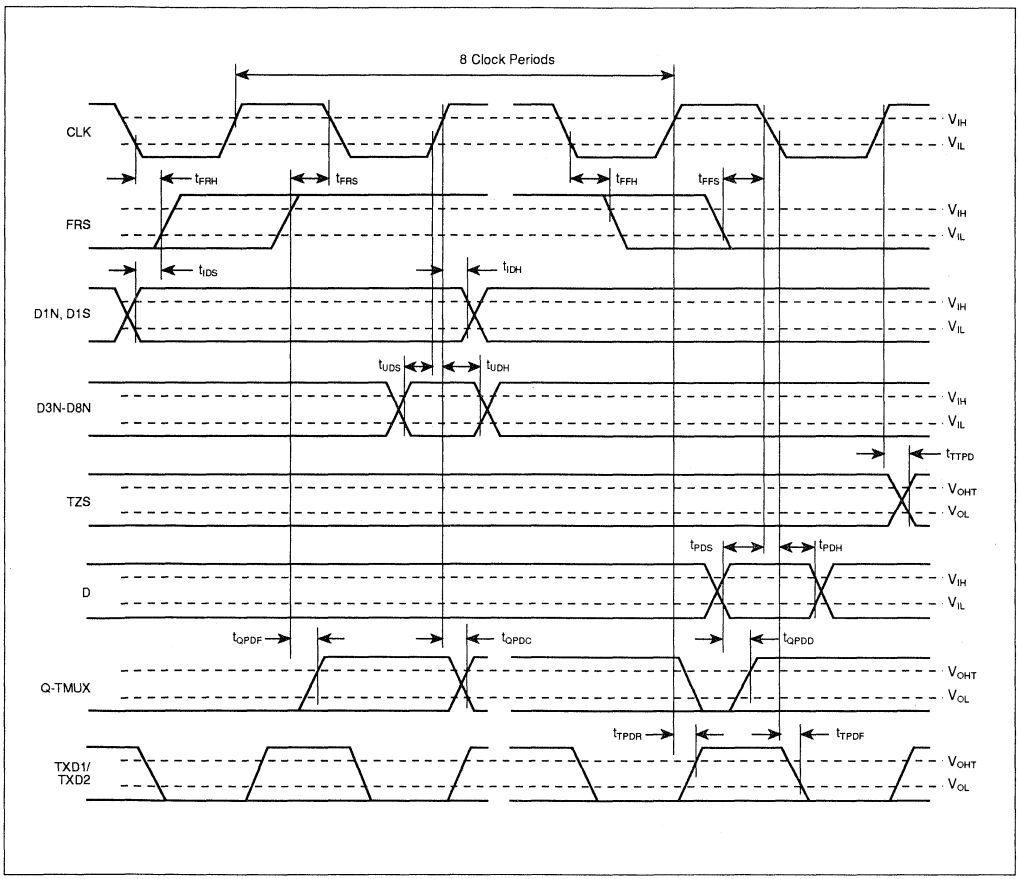


Fig. 5 MV1444 Timing parameters

MV1445

COMBINED PCM HDB3 DECODER, DIGITAL CLOCK REGENERATOR AND TIMESLOT ZERO RECEIVER

The MV1445 combines the HDB3 Decoder, Digital Clock Regnerator and Timeslot Zero Receiver functions required by a 2.048Mbit 30 channel PCM transmission link operating in accordance with the appropriate CCITT Recommendations and forms part of the GPS 2Mbit PCM signalling series of devices. The circuit is fabricated in CMOS and operates from a single +5V supply.

The HDB3 Decoder section of the MV1445 is responsible for decoding the incoming 2.048Mbit HDB3 encoded pseudo-ternary PCM data stream back into NRZ binary form. This decoding is carried out in accordance with Annex A to CCITT Recommendation G.703.

In order to perform this process, the HDB3 Decoder requires a 2.048MHz clock signal to be recovered from the incoming HDB3 data stream. This clock regeneration may be carried out externally using a tuned circuit or internally using the on-chip Digital Clock Regenerator. This digital clock regenerator circuit continuously re-synchronises a divide-by-8 counter being clocked at 16.384MHz to the incoming HDB3 data stream and performs in accordance with the tolerance to input jitter specification of CCITT Recommendation G.823.

The Timeslot Zero Receiver function searches for the CCITT Frame Alignment signal in the NRZ data stream being output by the HDB3 Decoder and when this pattern is detected the receiver synchronises itself to it in accordance with the Frame Alignment strategy detailed in CCITT Recommendation G.732. Once frame alignment has been achieved the Timeslot Zero Receiver produces various timing outputs for the use of external circuitry and extracts the user data bits of timeslot zero.

FEATURES

- Single +5V supply.
- All Inputs and Outputs TTL compatible.
- HDB3 Decoding carried out in accordance with CCITT Recommendation G.703.
- Provides HDB3 Error Monitor, Loss of Input Alarm and AIS Monitor.
- On-chip digital clock regenerator operates in accordance with tolerance to input jitter specification of CCITT Recommendation G.823.
- Receiver Frame Synchronisation carried out in accordance with CCITT Recommendation G.732.
- Provides Alarm Outputs for Reception of Corrupted Alignment word and Loss of Frame Alignment.
- Extracts the International Spare Bits from Alternate Frames or from Frames 13 and 15 of the CCITT CRC-4 multiframe.

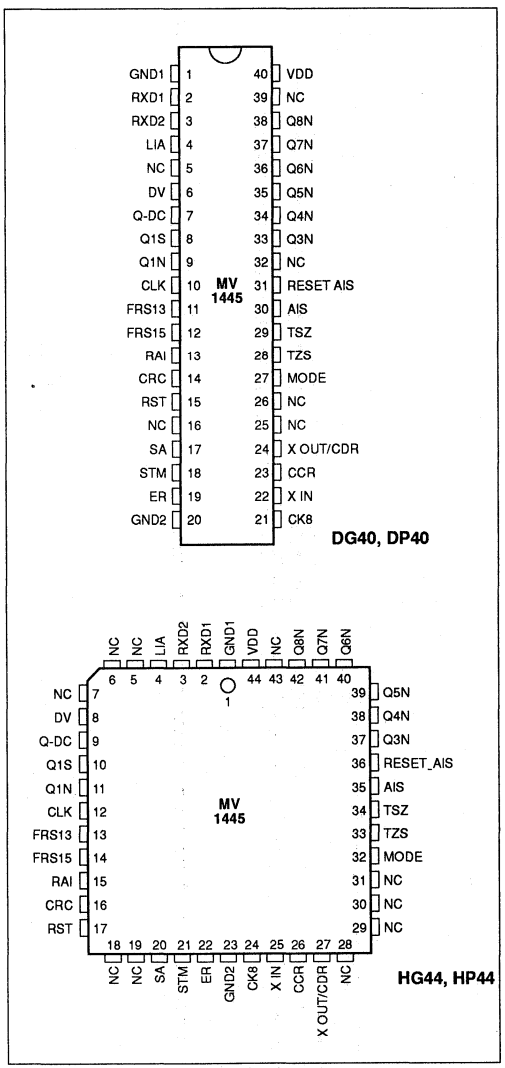


Fig. 1 Pin connections - top view

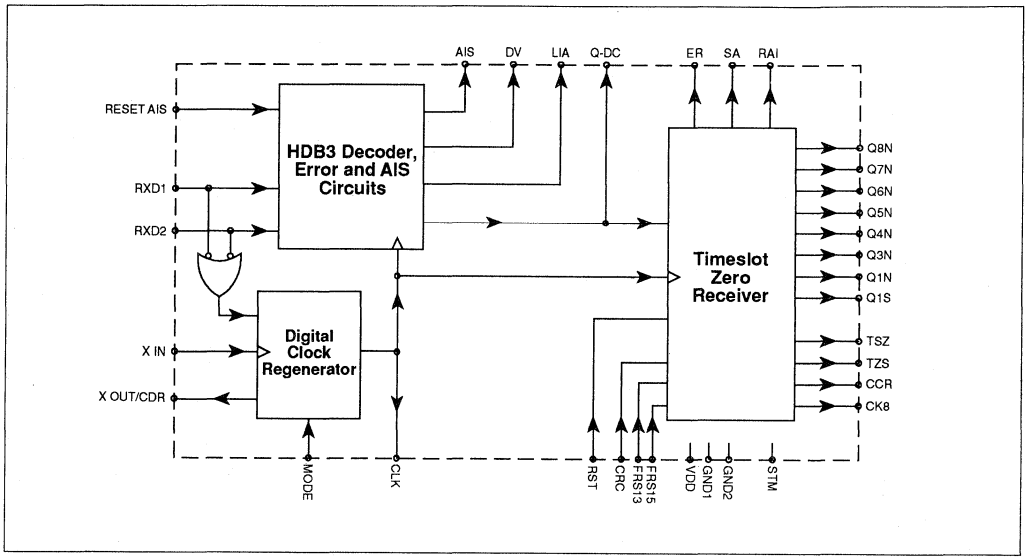


Fig. 2 Block diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

ELECTRICAL RATINGS

Supply Voltage	-0.5V to +7V
Input Voltage	-0.5V to VDD +0.5V
Output Voltage	-0.5V to VDD +0.5V

FUNCTIONAL DESCRIPTION

The MV1445 combines the HDB3 Decoder, Digital Clock Regenerator and Timeslot Zero Receiver functions required by a 2.048Mbit 30 channel PCM transmission link operating in accordance with the appropriate CCITT Recommendations. The block diagram of the MV1445 is shown in Fig.2 and the function of each block is now described separately.

HDB3 Decoder

The HDB3 decoder circuit is responsible for converting the 2.048Mbit HDB3 encoded pseudo-ternary PCM data stream on its inputs, RXD1 and RXD2, back in to NRZ binary form to be output to external circuitry and the Timeslot Zero Receiver. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703, Annex A.

High Density Bipolar 3 (HDB3) is a ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to ensure adequate clock recovery at the receiver. In any sequence of four consecutive binary zeroes, the last zero is substituted by a mark of the same polarity of the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code and ensures that successive violations alternate in polarity and as such introduce no DC component to the HDB3 signal.

The HDB3 Decoder synchronously decodes the data on its RXD input pins into NRZ form under control of a 2.048MHz system clock. There is a 5 clock period delay between the HDB3 data being clocked in from the RXD inputs and the NRZ data appearing on the Q-DC output. In addition to the basic HDB3 decoding the circuit also provides three alarm outputs. The first of these alarms is DV (Double Violation) and a logic high on this output denotes that two successive violations have been received with the same polarity, thus violating the HDB3 decoding laws. The second alarm, LIA (Loss of Input Alarm), is used to denote that 11 consecutive zeroes have been received on the RXD inputs. The third alarm output is AIS (Alarm Indication Signal). This output will go high if less than 3 decoded zeros have been detected in the preceding RESET AIS=1 period (i.e. between RESET AIS=0 pulses) and as such this alarm can be used to detect the CCITT Alarm Indication Signal. The timing diagrams of the HDB3 Decoder circuit are shown in Fig. 3.

Digital Clock Regenerator

In order to decode the incoming HDB3 data stream the HDB3 decoder requires a 2.048MHz clock to be recovered from the incoming data stream. This may either be produced externally using a tuned circuit or internally using the on-chip digital clock regenerator.

Selection between these 2 recovery modes is carried out by the MODE control pin, and with MODE high, internal clock recovery is selected.

When external clock recovery is selected, a logical 'OR' function of the inverted HDB3 inputs is output on the X OUT/CDR pin for the use of the external clock recovery circuit. The 2.048MHz clock signal thus regenerated is then input back to the MV1445 on the CLK I/O pin.

In internal clock recovery mode, the digital clock regenerator requires either a 16.384MHz clock signal to be input to the X IN pin or a 16.384MHz crystal to be connected between pins X IN and X OUT/CDR. The 16.384MHz clock signal thus produced is used to clock a divide-by-8 counter to produce the recovered 2.048MHz system clock. This counter is continuously re-synchronised to the incoming data stream and attempts to choose the 16.384MHz clock edge furthest from the falling edge of either of the RXD inputs to use as the rising edge of the 2MHz recovered clock, giving the highest tolerance to incoming jitter. This circuit performs in full compliance with the tolerance to input jitter specification of CCITT Recommendation G.823. The regenerated clock thus produced is input to the HDB3 Decoder and Timeslot Zero Receiver circuits and is also output to external circuitry on the CLK I/O pin.

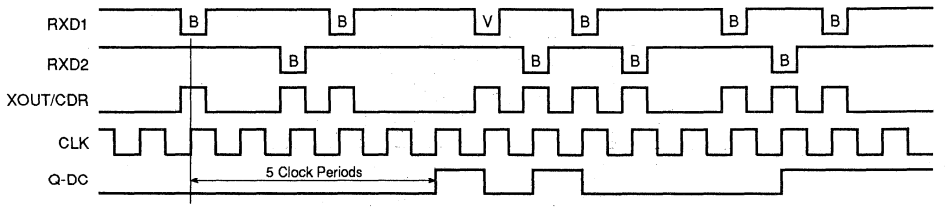
Timeslot Zero Receiver

The Timeslot Zero Receiver circuit is responsible for searching for and locking on to the CCITT Frame Alignment Signal present in timeslot zero of the NRZ PCM data stream being decoded by the HDB3 Decoder. This process is carried out in accordance with the loss and recovery of frame alignment strategy described in CCITT Recommendation G.732. Once frame alignment has been achieved the Timeslot Zero Receiver circuit outputs various timing reference signals for the synchronisation of external circuitry. These timing outputs will all free run if frame synchronisation is subsequently lost. In addition, a control input, RST, may be used to reset this synchronisation process, forcing the receiver out of frame alignment.

The Timeslot Zero Receiver circuit produces 4 timing outputs for use by external circuitry if required. The first of these timing outputs is TSZ which is an 8 clock period long, high going pulse masking the position of timeslot zero and facilitates the frame alignment of external circuitry. The second timing output, TZS, is a 4KHz signal which changes state once per frame, one clock period after the end of timeslot zero, and is high during sync frames to allow sync and non-sync frames to be distinguished. The third timing output, CCR, is a low going pulse, one clock period wide, occurring during bit 1, timeslot 1 of sync frames. The final timing output, CK8, is an 8KHz signal going low at the end of bit 7 of each timeslot zero and high at the end of bit 7 in each timeslot 16.

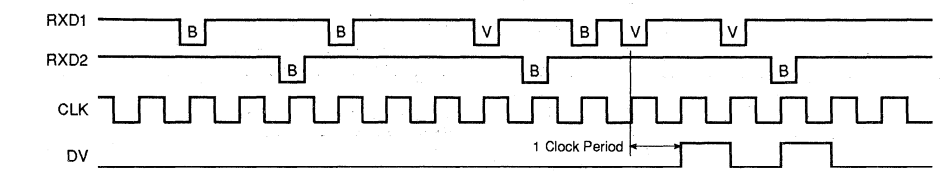
In addition to these timing outputs, two alarm outputs are provided to indicate errors in the incoming data stream. The first of these alarms, ER, goes high for one frame following a sync frame in which a corrupted FAS was detected when the receiver is in sync. Three consecutive alarms of this type will put the receiver out of sync. The second alarm, SA, goes high to indicate that the Timeslot Zero Receiver is out of frame alignment.

In addition to the frame synchronisation process, the Timeslot Zero Receiver is also responsible for extracting the user data bits of non-sync words and the two International / CRC bits of timeslot zero. The user data bits present in bits 3 to 8 of timeslot zero of non-sync frames are extracted and output on the Q3N-Q8N parallel data outputs. The third bit of non-sync words, Q3N, is used as the remote alarm bit in 2Mbit PCM systems and a third alarm output, RAI, is derived from this bit. This alarm is a persistence checked version of Q3N which goes high when two consecutive Q3N bits have been received high whilst the receiver is in sync. The Timeslot Zero Receiver also extracts the data present in bit 1 of timeslot zero under control of the CRC input. This input selects between CCITT CRC-4 and non-CRC-4 modes of operation. In non-CRC-4 mode, the international spare bits are extracted from bit 1 of all sync and non-sync frames and output on pins Q1S and Q1N respectively. In CRC-4 mode, these data outputs are extracted from bit 1 of frames 13 and 15 of the CCITT CRC-4 multiframe structure respectively. In order to accomplish this, two timing inputs, FRS13 and FRS15, are required in CRC-4 mode. These inputs are required to be high during bit 8 of the appropriate frame, low during bit 8 of any other non-sync frame and any state elsewhere. The timing diagrams for the Timeslot Zero Receiver are shown in Fig.4.



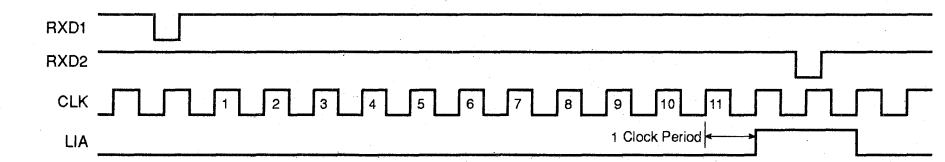
Notes:- 1) The Decoded NRZ output is delayed by 5 clock periods with respect to the HDB3 inputs.
2) The diagram assumes the last violation occured on RXD2.
3) B is HDB3 mark, V is a HDB3 violation.

Decoder waveforms



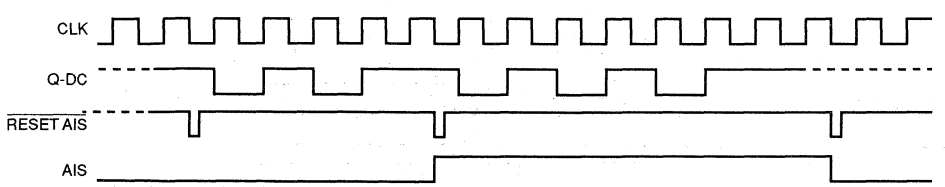
Notes:- 1)There is a single period delay between detection of an error and the rising edge of DOUBLE VIOLATION
2) The diagram assumes the last violation occured on RXD2.
3) B is HDB3 mark, V is a HDB3 violation.

HDB3 Double violation waveforms



Note:- 1)The 'LOSS OF INPUT' is delayed by a single clock period with respect to the incoming HDB3 waveforms.

Loss of input violations



AIS and $\overline{\text{RESET AIS}}$ waveforms

Fig. 3 HDB3 Decoder timing

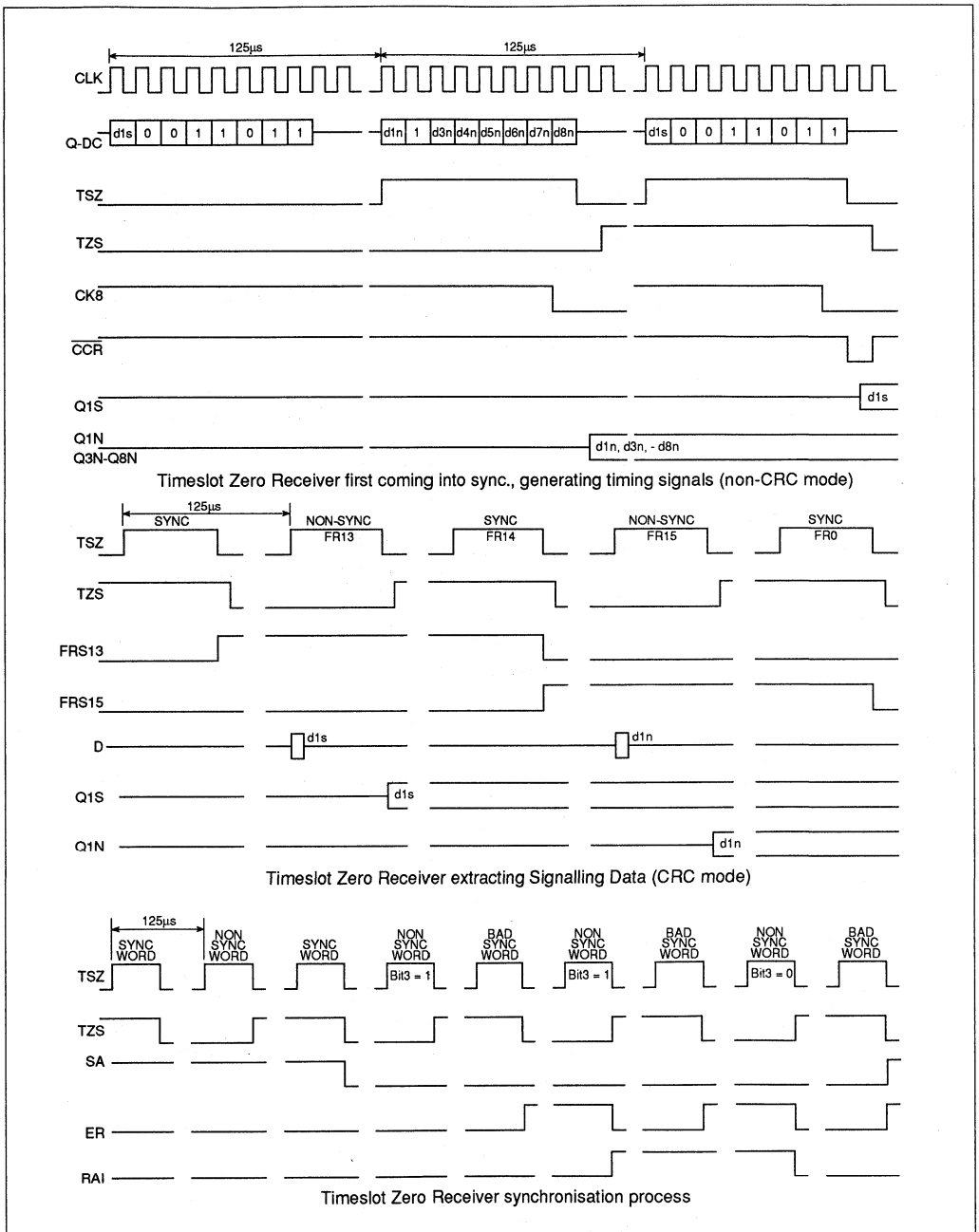


Fig. 4 Timeslot zero receiver timing

PIN DESCRIPTIONS

Pin name	Pin no.		Pin description
	DG40	HG44	
GND1	1	1	Digital Ground. OV (Note 1)
RXD1	2	2	HDB3 Encoded Input 1 to HDB3 Decoder. This is one of the pair of 2.048Mbit pseudo-ternary HDB3 encoded PCM data stream inputs to the HDB3 Decoder. This input asynchronously latches the incoming HDB3 data and is falling edge sensitive. Since the input is asynchronously latched it is not necessary for the RXD pulse to straddle a rising clock edge.
RXD2	3	3	HDB3 Encoded Input 2 to HDB3 Decoder. See description for pin RXD1.
LIA	4	4	Loss of Input Alarm Output from HDB3 Decoder. This output goes high one period after the detection of 11 consecutive zeroes on the RXD inputs. Any HDB3 mark on the inputs (RXD1 or RXD2=0) resets this output low after a single clock period delay.
DV	6	8	Double Violation Alarm Output from HDB3 Decoder. This output goes high for one period of CLK, one period after the detection of a HDB3 violation of the same polarity as the previous HDB3 violation.
Q-DC	7	9	NRZ Data Output from HDB3 Decoder. This output represents the HDB3 input data decoded back in to NRZ binary form, with a 5 clock period delay from the HDB3 inputs to the NRZ output. The 2.048Mbit PCM data stream on this pin is also input to the Timeslot Zero Receiver.
Q1S	8	10	International / CRC Data Bit Output of Timeslot Zero Receiver for Sync Frames. With CRC=0, this output latches data from bit 1, timeslot zero of sync frames. With CRC=1, this output latches data from bit 1, timeslot zero of frame 13 of the CRC-4 multiframe, under control of the FRS13 input. In either case this output changes state on the falling edge of CLK, half a clock period after the end of timeslot zero.
Q1N	9	11	International / CRC Data Bit Output of Timeslot Zero Receiver for Non-sync Frames. With CRC=0, this output latches data from bit 1, timeslot zero of non-sync frames. With CRC=1, this output latches data from bit1, timeslot zero of frame 15 of the CRC-4 multiframe, under control of the FRS15 input. In either case this output changes state on the faliing edge of CLK, half a clock period after the end of timeslot zero.
CLK	10	12	2.048MHz System Clock I/O pin. In Internal Clock Regeneration mode (MODE=1), this pin is used to output the internally recovered 2.048MHz clock signal to external circuitry. In external clock regeneration mode (MODE=0), this pin is used to input the externally regenerated clock signal to the HDB3 Decoder and Timeslot Zero Receiver blocks.

PIN DESCRIPTIONS (continued)

Pin name	Pin no.		Pin description
	DG40	HG44	
FRS13	11	13	Frame 13 Marker Input to Timeslot Zero Receiver. This input is used by the Timeslot Zero Receiver operating in CRC-4 mode to reference the position of Frame 13. This input is required to be high during bit 8, Frame 13 of the CRC multiframe and low during bit 8 of all other non-sync frames.
FRS15	12	14	Frame 15 Marker Input to Timeslot Zero Receiver. This input is used by the Timeslot Zero Receiver operating in CRC-4 mode to reference the position of Frame 15. This input is required to be high during bit 8, Frame 15 of the CRC multiframe and low during bit 8 of all other non-sync frames.
RAI	13	15	Remote Alarm Indication Output of Timeslot Zero Receiver. This alarm output is a persistence checked version of the Q3N output. When the receiver is in sync this output will go high if 2 consecutive Q3N bits are received high. This output changes state at the beginning of bit 1, timeslot 1 of non sync frames. When the receiver is out of sync this output is forced low in the non-sync frame following the last bad sync frame, and is held low until the receiver comes back in to sync.
CRC	14	16	CRC-4 Mode Select Input to Timeslot Zero Receiver. This input is used to control the extraction of the Q1N and Q1S data outputs from the incoming PCM data stream. A logic high on this input selects CRC-4 mode of operation.
RST	15	17	Reset Input to Timeslot Zero Receiver. A logic high on this pin straddling a falling edge of CLK will reset the state machine of the Timeslot Zero Receiver, forcing it out of frame alignment.
SA	17	20	Synchronisation Alarm Output from Timeslot Zero Receiver. This output is high whenever the receiver is out of sync and only changes state at the beginning of bit 1, timeslot 1 of sync frames.
STM	18	21	Scan Path Test Global Mode Pin. A logic high on this pin configures the MV1445 in scan test mode. For normal operation this pin should be tied low.
ER	19	22	Sync Word Error Output of Timeslot Zero Receiver. This alarm output goes high for one frame immediately after detection of a bad timeslot zero frame alignment signal, whilst the receiver is in sync. Three consecutive errors of this type will put the receiver out of sync and the last ER pulse of this sequence will be longer than 256 periods if a valid sync word is detected during the pulse.
GND2	20	23	Digital Ground. OV (Note 1)
CK8	21	24	8KHz Clock Output from Timeslot Zero Receiver. This output goes low at the beginning of bit 8, timeslot 0 and high at the beginning of bit 8, timeslot 16.

PIN DESCRIPTIONS (continued)

Pin name	Pin no.		Pin description
	DG40	HG44	
X IN	22	25	Crystal Amplifier Input of Digital Clock Regenerator Circuit. In Internal clock recovery mode this pin forms the input to the crystal oscillator circuit, used in conjunction with the X OUT/CDR pin. Alternatively, this pin may be used as a 16.384Mhz clock input to the internal clock regenerator if one oscillator is shared between several devices. This pin has no function when external clock recovery is selected and should be tied to GND.
CCR	23	26	Channel Reset Timing Output from Timeslot Zero Receiver. This output pulses low for a single period during bit 1, timeslot 1 of sync frames.
X OUT/ CDR	24	27	Crystal Amplifier/Clock Regenerate output from Digital Clock Regenerator. In internal clock recovery mode, this pin is used as the 16.384MHz output of the crystal oscillator circuit and is not used if an externally generated 16.384Mhz clock is used. In external clock recovery mode, this pin is used to output the logical 'OR' function of the inverted HDB3 inputs for the use of the external clock recovery circuit.
MODE	27	32	Clock Recovery Mode Select Input. This input is used to select between internal and external clock recovery modes. A logic high on this input selects internal clock regeneration.
TZS	28	33	Timeslot Zero Sync Frame Output from Timeslot Zero Receiver. This 4KHz output changes state at the end of bit 1, timeslot 1 (Note 2) of every frame and is high during timeslot zero of sync frames.
TSZ	29	34	Timeslot Zero Marker Output from Timeslot Zero Receiver. This timing output goes high for the 8 clock periods of timeslot zero and is low at all other times
AIS	30	35	Alarm Indication Signal Output from HDB3 Decoder. See description for RESET AIS pin.
RESET AIS	31	36	Reset AIS Input to HDB3 Decoder. A logic '0' on this input resets a decoded zeros counter in the HDB3 Decoder. It will also reset the AIS output to '0' provided 3 or more zeros have been decoded in the preceding RESET AIS=1 period, or set AIS to '1' if less than 3 zeros have been decoded in the preceding RESET AIS=1 period. This may be used to detect the CCITT Alarm Indication Signal. A logic '1' on this pin enables the decoded zeros counter.
Q3N Q4N Q5N Q6N Q7N Q8N	33 34 35 36 37 38	37 38 39 40 41 42	User Data Bit Outputs of Timeslot Zero Receiver. These 6 parallel data outputs are extracted from bits 3-8 of timeslot zero during non-sync frames. These outputs change state on the falling edge of CLK half a clock period after the end of timeslot zero.
VDD	40	44	Digital Supply Voltage. 5V

NOTES

1. In order to facilitate adequate supply decoupling, both digital ground pins should be connected to 0V.

2. The bits of a timeslot are numbered from 1 to 8 whereas the timeslots of a frame are numbered from 0 to 31 and the frames of a CCITT multiframe are numbered from 0 to 15.

3. All inputs except X IN have 100K on-chip pull down resistors. The X IN pin has neither pull-up nor pull-down resistor to allow operation as a crystal oscillator and should be tied to digital ground if external clock regeneration is selected.

ELECTRICAL CHARACTERISTICS

Test Conditions:

Supply Voltage VDD = 5V ± 0.5V Ambient Temperature T_{amb} = -40°C to +85°C

STATIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low Level Input Voltage	V_{IL}	0.0		0.8	V	
High Level Input Voltage	V_{IH}	2.0		V_{DD}	V	
LOW Level Output Voltage	V_{OL}			0.4	V	Isink=2mA
High Level Output Voltage	V_{OHT}	2.4			V	Isource=2mA
	V_{OHC}	V_{DD}-1.0			V	Isource=lmA
Input Leakage Current	I_{IL}	-10		200	uA	$V_{IN} = V_{DD}$ or V_{SS}
Input Capacitance	C_{IN}		5		pF	All Inputs
Output Capacitance	C_{OUT}		5		pF	All Outputs

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
CLOCK						
Clock Period	t_{CP}	400			ns	See Fig. 5
Clock Rise/Fall Time	t_{CR}/t_{CF}			20	ns	See Fig. 5
Clock High/Low Time	t_{CH}/t_{CL}	150			ns	See Fig. 5
DECODER						
RXD1/2 Data Setup Time	t_{RS}	50			ns	See Fig. 6
RXD1/2 Pulse Width	t_{RW}	50			ns	See Fig. 6
CDR Propagation Delay	t_{CPDR}/t_{CPDF}	50			ns	See Fig. 6, Notes 1 and 2.
Decoder Output Propagation Delay.	t_{OPD}	60			ns	See Fig. 6, Notes 1 and 3.
RESET AIS Hold-Off Time	t_{RAHO}	20			ns	See Fig. 6
RESET AIS Pulse Width	t_{RAW}	30			ns	See Fig. 6
Reset AIS Setup Time	t_{RAS}	20			ns	See Fig. 6
AIS Propagation Delay	t_{APD}			65	ns	See Fig. 6, Note 1.
RECEIVER						
Data / Control Setup Time	t_{DS}	50			ns	See Fig. 7, Note 4.
Data / Control Hold Time	t_{DH}	50			ns	See Fig. 7, Note 4.
Timing / Alarm Propagation Delay	t_{TAPD}			70	ns	See Fig. 7, Notes 1 and 5.
Data Outputs Propagation Delay	t_{DPD}			80	ns	See Fig. 7, Notes 1 and 6.

NOTES

1. All output propagation delays are measured with a 50pF load.
2. This parameter assumes external clock recovery is selected.
3. The t_{OPD} parameter applies to outputs Q-DC, LIA and DV, but does not apply to AIS.
4. The Timeslot Zero Receiver Data / Control setup and hold time parameters, t_{DS} and t_{DH}, apply to the following inputs: D, RST, FRS13 and FRS15.
5. The Timeslot Zero Receiver Timing / Alarm Output propagation delay parameter applies to the following outputs: TSZ, TZS, CCR, CK8, ER, SA and RAI.
6. The Timeslot Zero Receiver Data Output propagation delay parameter applies to the following outputs: QIS, QIN, Q3N, Q4N, Q5N, Q6N, Q7N and Q8N.

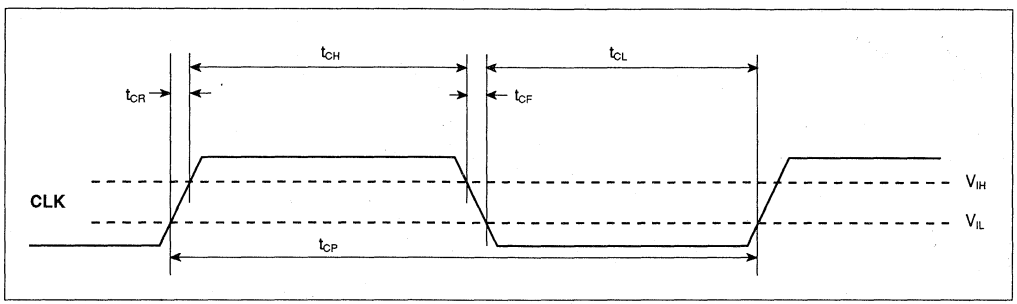


Fig. 5 Clock timing parameters

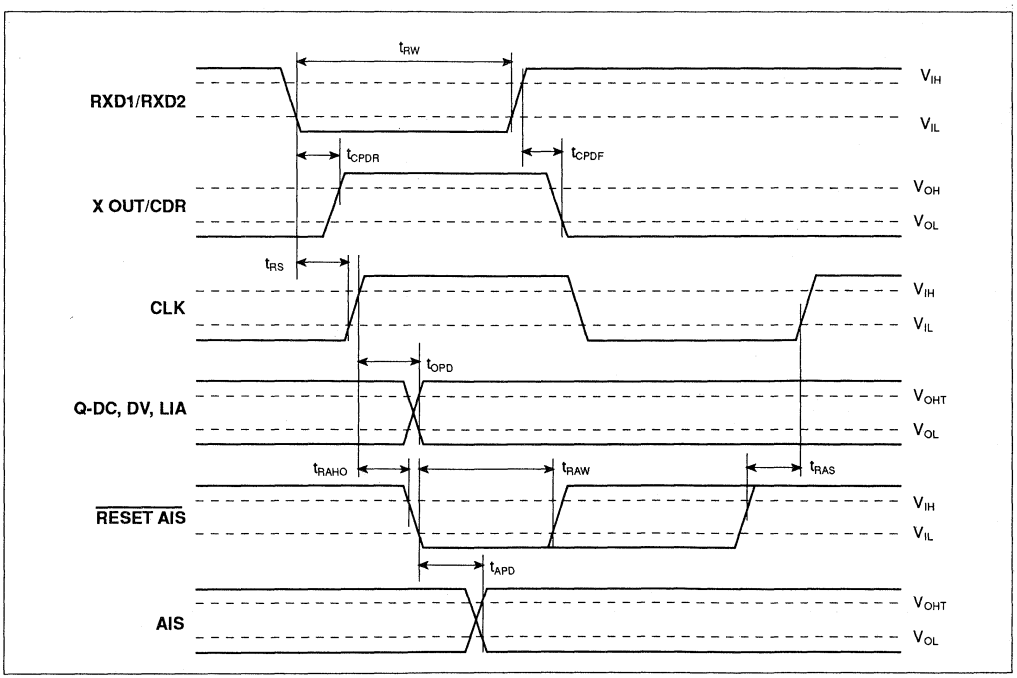


Fig. 6 HDB3 Decoder timing parameters

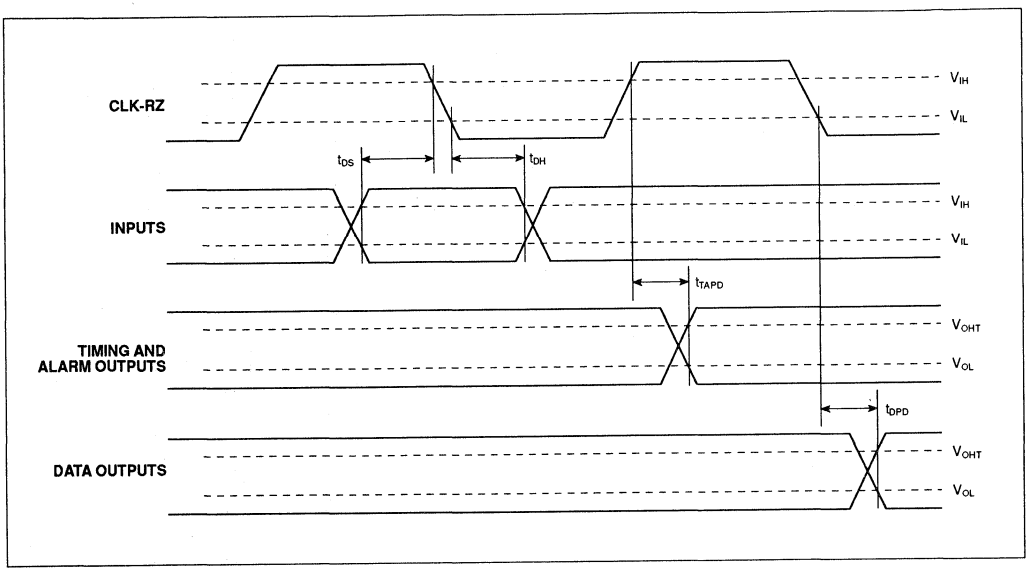


Fig. 7 Timeslot zero receiver timing

ORDERING INFORMATION

MV1445/IG/DGAS
MV1445/IG/DPAS
MV1445/IG/HGAS
MV1445/IG/HPAS

MV1449

PCM HDB3 ENCODER/DECODER

The MV1449, along with other devices in the GPS 2Mbit PCM signalling series comprise a group of circuits which will perform the common channel signalling and error detection functions for a 2.048Mbit PCM transmission link operating in accordance with the appropriate CCITT Recommendations. The MV1449 is also capable of operation at the next CCITT hierarchical bit rate of 8.448Mbit. The MV1449 circuit is fabricated in CMOS and operates from a single +5V supply with all inputs and outputs being TTL compatible.

The MV1449 is an encoder/decoder for the HDB3 pseudo-ternary transmission code, described in Annex A of CCITT Recommendation G.703. The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of the HDB3 coding, all ones detection and loss of input (all zero's detection). In addition a loop back function is provided for terminal testing.

FEATURES

- Single +5V supply.
- All Inputs and Outputs TTL compatible.
- HDB3 Encoding and Decoding to CCITT Recommendation G.703.
- Simultaneous Encoding and Decoding.
- Clock Recovery Signal allows Clock Regeneration from Incoming HDB3 Data.
- Loop Back Control.
- HDB3 Error Monitor.
- Alarm Indication Signal Monitor.
- Loss of Input Alarm.
- Low Power Operation.
- 2.048MHz or 8.448MHz Operation.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

ELECTRICAL RATINGS

Supply Voltage	-0.5V to +7V
Input Voltage	-0.5V to VDD +0.5V
Output Voltage	-0.5V to VDD +0.5V

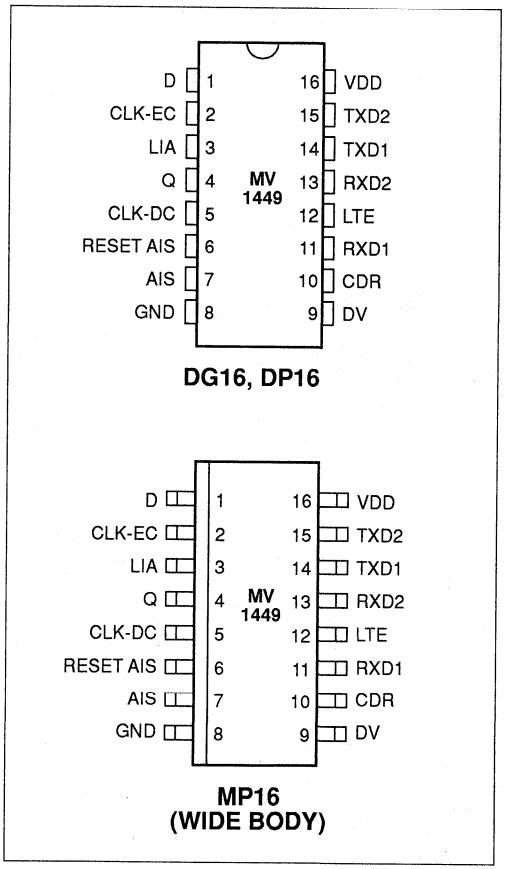


Fig. 1 Pin connections - top view

ORDERING INFORMATION

MV1449/IG/DGAS
MV1449/IG/DPAS
MV1449/IG/MPES

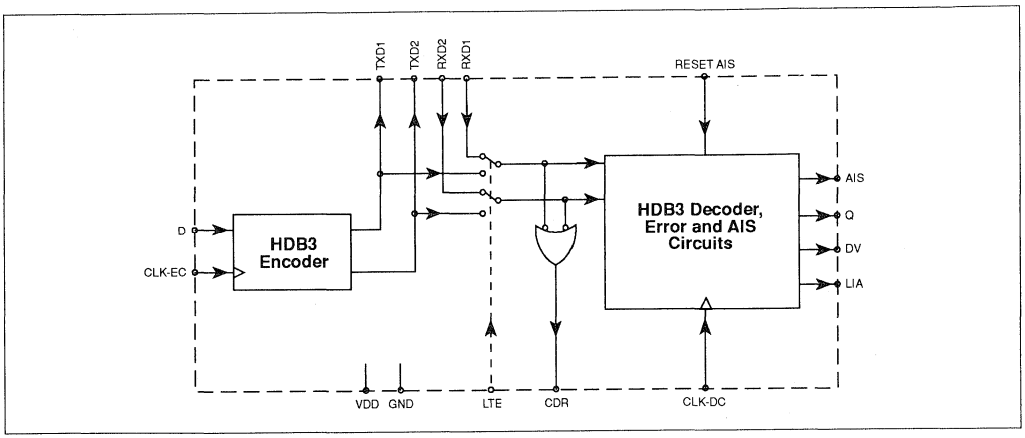


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

High Density Bipolar 3 (HDB3) is a ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to ensure adequate clock recovery at the receiver. In any sequence of four consecutive binary zero's, the last zero is substituted by a mark of the same polarity of the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code and ensures that successive violations alternate in polarity and as such introduce no DC component to the HDB3 signal.

The MV1449 consists of two main blocks, the HDB3 Encoder and the HDB3 Decoder, with the Block Diagram being shown in Fig. 2. The function of each block is now described separately.

HDB3 Encoder

The HDB3 Encoder is responsible for converting the incoming NRZ data into HDB3 Encoded pseudo-ternary form for transmission over a 2.048Mbit/8.448Mbit PCM link. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703, Annex A.

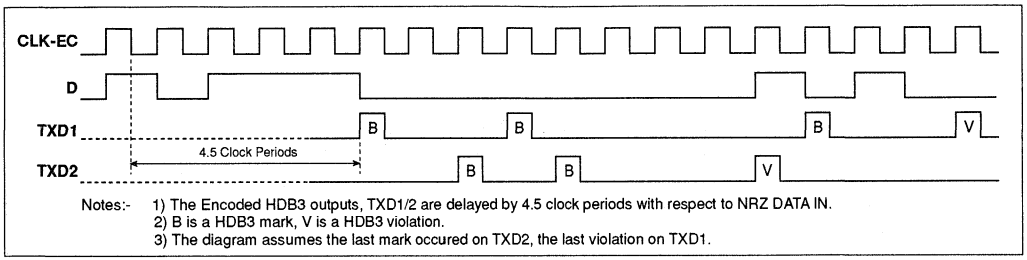
The data to be encoded is input on the D input pin and the encoding process is synchronised to the 2.048MHz/8.448MHz clock signal being input on the CLK-EC pin. The HDB3 Encoder has two outputs, TXD1 and TXD2, which represent the HDB3 encoded PCM data stream in pseudo-ternary form. If a mark or violation is to be transmitted the output pulses high after the rising edge of clock, with the length of the pulse set by the clock high pulse width. The timing diagram of the HDB3 Encoder is shown in Fig. 3.

HDB3 Decoder

The HDB3 Decoder circuit is responsible for converting the 2.048Mbit/8.448Mbit HDB3 encoded pseudo-ternary PCM data stream on its inputs, RXD1 and RXD2, into NRZ binary form to be output on the Q output pin. This conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G.703, Annex A. The HDB3 Decoder synchronously decodes the data on its RXD input pins into NRZ form under control of the 2.048MHz/8.448MHz clock being input on its CLK-DC pin. There is a 5 clock period delay between the HDB3 data being clocked in from the RXD inputs and the NRZ data appearing on the Q output. The Decoder clock must be externally regenerated from the incoming HDB3 data stream and in order to aid this clock recovery a logical 'OR' function of the inverted HDB3 inputs is output on the CDR pin.

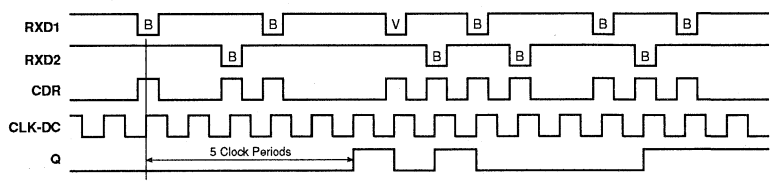
In addition to the basic HDB3 decoding the circuit also provides three alarm outputs. The first of these alarms is DV (Double Violation) and a logic high on this output denotes that two successive violations have been received with the same polarity, thus violating the HDB3 decoding laws. The second alarm, LIA (Loss of Input Alarm), is used to denote that 11 consecutive zero's have been received on the RXD inputs. The third alarm output is AIS (Alarm Indication Signal). This output will go high if less than 3 decoded zero's have been detected in the preceding RESET AIS=1 period (i.e. between RESET AIS=0 pulses) and as such this alarm can be used to detect the CCITT Alarm Indication Signal. All the alarm circuitry as well as the decoding process is synchronised to the clock signal being input on the CLK-DC pin. The clock signal may be asynchronous with the CLK-EC signal. The timing diagrams of the HDB3 Decoder circuit are shown in Fig. 4.

In addition to the normal mode of operation, a loop test mode is available for terminal testing. This mode is selected by taking the LTE (Loop Test Enable) input high. In this mode, the HDB3 encoded pseudo-ternary data outputs of the encoder block are inverted and fed back as the inputs to the decoder block, which in turn decodes this data and outputs it in NRZ form.



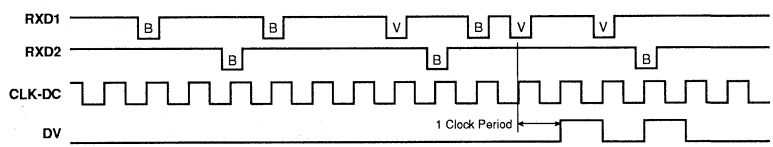
Notes:- 1) The Encoded HDB3 outputs, TXD1/2 are delayed by 4.5 clock periods with respect to NRZ DATA IN.
2) B is a HDB3 mark, V is a HDB3 violation.
3) The diagram assumes the last mark occured on TXD2, the last violation on TXD1.

Fig. 3 HDB3 Encoder waveforms



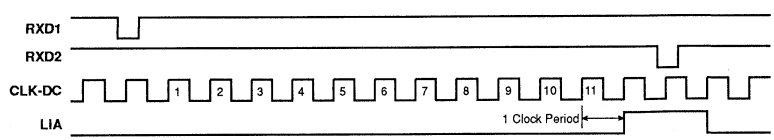
Notes:- 1) The Decoded NRZ output is delayed by 5 clock periods with respect to the HDB3 inputs.
2) The diagram assumes the last violation occured on RXD2.
3) B is HDB3 mark, V is a HDB3 violation.

Decoder waveforms



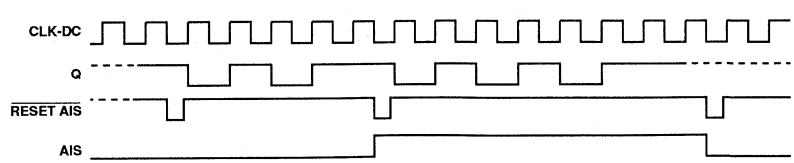
Notes:- 1)There is a single period delay between detection of an error and the rising edge of DOUBLE VIOLATION
2) The diagram assumes the last violation occured on RXD2.
3) B is HDB3 mark, V is a HDB3 violation.

HDB3 Double violation waveforms



Note:- 1)The 'LOSS OF INPUT' is delayed by a single clock period with respect to the incoming HDB3 waveforms.

Loss of input violations



AIS and $\overline{\text{RESET AIS}}$ waveforms

Fig. 4 HDB3 Decoder waveforms

PIN DESCRIPTIONS

Pin Name	Pin no.	Pin description
D	1	NRZ Data Input pin to HDB3 Encoder. The NRZ binary data on this pin is input to the HDB3 Encoder for conversion to HDB3 pseudo-ternary form under control of the CLK-EC signal. The D input is latched into the Encoder block by the falling edge of CLK-EC.
CLK-EC	2	2.048MHz/8.448MHz Clock Input to HDB3 Encoder. The clock signal on this input pin is used for the encoding of data on pin 1.
LIA	3	Loss of Input Alarm Output from HDB3 Decoder. This output goes high one period after the detection of 11 consecutive zeroes on the RXD inputs. Any HDB3 mark on the inputs (RXD1 or RXD2=0) resets this output low after a single clock period delay.
Q	4	NRZ Data Output from HDB3 Decoder. This output represents the HDB3 input data decoded back into NRZ binary form, with a 5 clock period delay from the HDB3 inputs to the NRZ output. This decoding process is carried out under control of the CLK-DC signal.
CLK-DC	5	2.048MHz/8.448MHz clock Input to HDB3 Decoder. The clock signal on this pin is used for the decoding of data on the RXD input pins, or the TXD pins in Loop Test Mode. This pin is used to input the externally regenerated clock signal recovered from the incoming HDB3 waveforms back to the Decoder block.
RESET AIS	6	Reset AIS Input to HDB3 Decoder. A logic '0' on this input resets a decoded zeros counter in the HDB3 Decoder. It will also reset the AIS output to '0' provided 3 or more zeros have been decoded in the preceding RESET AIS=1 period, or set AIS to '1' if less than 3 zeros have been decoded in the preceding RESET AIS=1 period. This may be used to detect the CCITT Alarm Indication Signal. A logic '1' on this pin enables the decoded zeros counter.
AIS	7	Alarm Indication Signal Output from HDB3 Decoder. See description for RESET AIS pin.
GND	8	Digital Ground. 0V
DV	9	Double Violation Alarm Output from HDB3 Decoder. This output goes high for one period of CLK-DC, one period after the detection of a HDB3 violation of the same polarity as the previous HDB3 violation.
CDR	10	Clock Recovery Output from HDB3 Decoder. This pin is used to output the logical 'OR' function of the inverted HDB3 inputs for the use of the external clock recovery circuit.

PIN DESCRIPTIONS (continued)

Pin Name	Pin no.	Pin description
RXD1	11	HDB3 Encoded Input 1 to HDB3 Decoder. This is one of the pair of 2.048Mbit pseudo-ternary HDB3 encoded PCM data stream inputs to the HDB3 Decoder. This input asynchronously latches the incoming HDB3 data and is falling edge sensitive. Since the input is asynchronously latched it is not necessary for the RXD pulse to straddle a rising clock edge.
LTE	12	Loop Test Enable Control Input. A logic low on this pin selects normal operation, with encoding and decoding being independent and asynchronous. A logic high on this pin internally connects TXD1 to RXD1 and TXD2 to RXD2. Note that in loop back mode, a decoder clock must be supplied (or regenerated from CDR) along with the encoder clock.
RXD2	13	HDB3 Encoded Input 2 to HDB3 Decoder. See description for pin RXD1.
TXD1	14	HDB3 Encoded Pseudo-Ternary Output 1 from HDB3 Encoder. The NRZ PCM data stream being input on the D pin is HDB3 encoded and output on this pin and pin TXD2. This output is always low during the low half cycle of clock and is only high during the high half cycle of clock if a mark is to be output. There is a 4.5 clock period delay from the falling edge of CLK-EC to TXD1.
TXD2	15	HDB3 Encoded Pseudo-Ternary Output 2 from HDB3 Encoder. See Pin TXD1 description.
VDD	16	Digital Supply Voltage. 5V

NOTES

1. All inputs have 100K on-chip pull down resistors.

ELECTRICAL CHARACTERISTICS

Test Conditions:
Supply Voltage VDD = 5V ± 0.5V Ambient Temperature T_{amb} = -40°C to +85°C

STATIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low Level Input Voltage	V_{IL}	0.0		0.8	V	
High Level Input Voltage	V_{IH}	2.0		V_{DD}	V	
Low Level Output Voltage	V_{OL}			0.4	V	Isink=2mA
High Level Output Voltage	V_{OHT}	2.4			V	Isource=2mA
	V_{OHC}	V_{DD}-1.0			V	Isource=lmA
Input Leakage Current	I_{IL}	-10		200	uA	V_{IN}=V_{DD} or V_{SS}
Supply Current	I_S			5	mA	2.048MHz Operation, Note 1.
				15	mA	8.448MHz Operation, Note 1.
Input Capacitance	C_{IN}		5		pF	All Inputs
Output Capacitance	C_{OUT}		5		pF	All Outputs

NOTES

1. All supply currents measured with outputs unloaded.

DYNAMIC CHARACTERISTICS

Note: Two sets of dynamic characterisitics are supplied, for use over the Commercial and Industrial Temperature ranges. The parameter set for the Commercial temperature range is aimed at customers wishing to switch from either the MJ1440 or MV1448 devices to the MV1449 since both the older devices were specified over the Commercial temperature range.

Test Conditions:
Supply Voltage VDD = 5V ± 0.5V Ambient Temperature T_{amb} = 0°C to +70°C

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
CLOCK						
Clock Period	t_{CP}	100			ns	See Fig. 5
Clock Rise/Fall Time	t_{CR}/t_{CF}			20	ns	See Fig. 5
Clock High/Low Time	t_{CH}/t_{CL}	30			ns	See Fig. 5
ENCODER						
Encoder Data Setup Time	t_{EDS}	15			ns	See Fig. 6
Encoder Data Hold Time	t_{EDH}	15			ns	See Fig. 6
TXD1/TXD2 Output Propagation Delay	t_{EPDR}/ t_{EPDF}			45	ns	See Fig. 6, Note 1.
DECODER						
RXD1/2 Data Setup Time	t_{RS}	15			ns	See Fig. 7
RXD1/2 Pulse Width	t_{RW}	20			ns	See Fig. 7
CDR Propagation Delay	t_{CPDR}/ t_{CPDF}			40	ns	See Fig. 7, Note 1.
Decoder Output Propagation Delay.	t_{OPD}			45	ns	See Fig. 7, Notes 1 and 2.
RESET AIS Hold-Off Time	t_{RAHO}	15			ns	See Fig. 7
RESET AIS Pulse Width	t_{RAW}	15			ns	See Fig. 7
Reset AIS Setup Time	t_{RAS}	10			ns	See Fig. 7
AIS Propagation Delay	t_{APD}			45	ns	See Fig. 7, Note 1.

Test Conditions:
Supply Voltage VDD = 5V ± 0.5V Ambient Temperature T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
CLOCK						
Clock Period	t_{CP}	100			ns	See Fig. 5
Clock Rise/Fall Time	t_{CR}/t_{CF}			20	ns	See Fig. 5
Clock High/Low Time	t_{CH}/t_{CL}	35			ns	See Fig. 5
ENCODER						
Encoder Data Setup Time	t_{EDS}	20			ns	See Fig. 6
Encoder Data Hold Time	t_{EDH}	20			ns	See Fig. 6
TXDI/TXD2 Output Propagation Delay	t_{EPDR}/ t_{EPDF}			50	ns	See Fig. 6, Note 1.
DECODER						
RXD1/2 Data Setup Time	t_{RS}	20			ns	See Fig. 7
RXD1/2 Pulse Width	t_{RW}	25			ns	See Fig. 7
CDR Propagation Delay	t_{CPDR}/ t_{CPDF}			45	ns	See Fig. 7, Note 1.
Decoder Output Propagation Delay.	t_{OPD}			50	ns	See Fig. 7, Notes 1 and 2.
RESET AIS Hold-Off Time	t_{RAHO}	15			ns	See Fig. 7
RESET AIS Pulse Width	t_{RAW}	20			ns	See Fig. 7
Reset AIS Setup Time	t_{RAS}	15			ns	See Fig. 7
AIS Propagation Delay	t_{APD}			55	ns	See Fig. 7, Note 1.

NOTES

1. All output propagation delays are measured with a 50pF load.
2. The t_{OPD} parameter applies to outputs Q, LIA and DV, but does not apply to AIS.

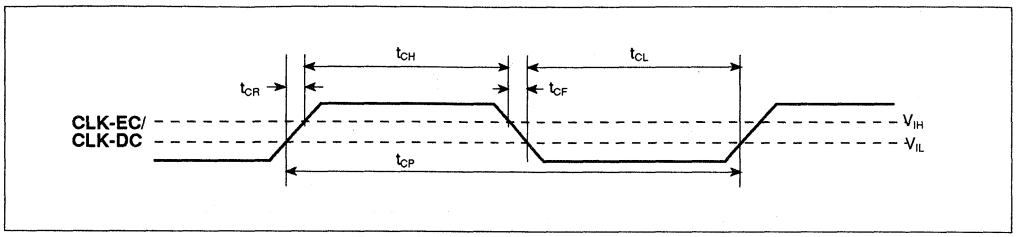


Fig. 5 Clock timing parameters

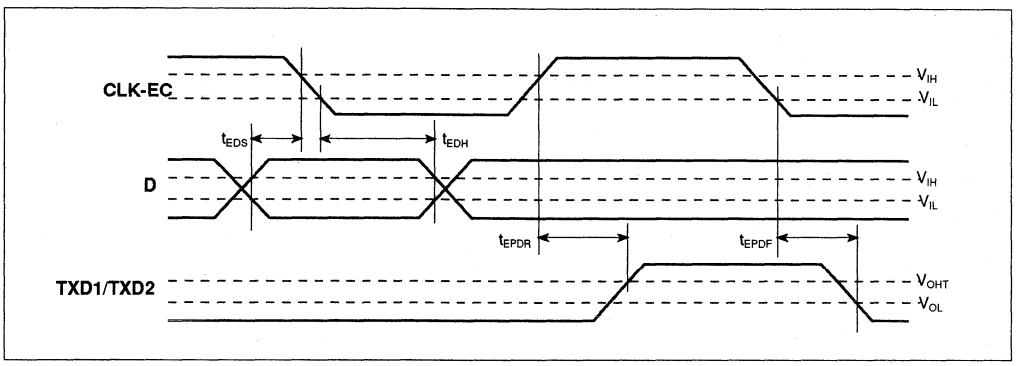


Fig. 6 Encoder timing parameters

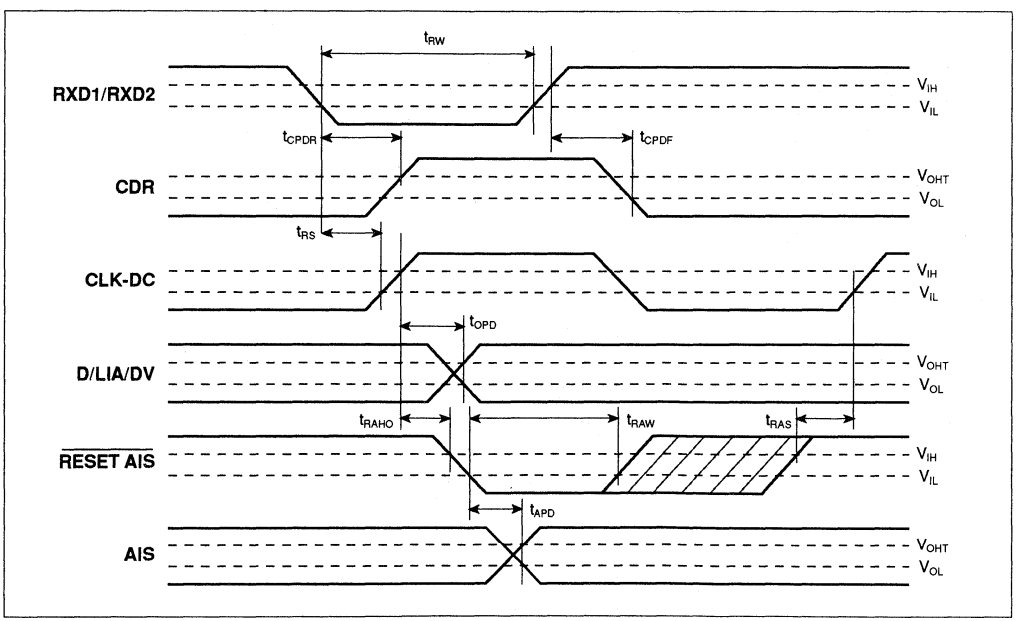


Fig. 7 Decoder timing parameters

MV1471

HDB3/AMI ENCODER/DECODER

The MV1471, along with other devices in the GPS 2Mbit PCM signalling series comprise a group of circuits which will perform the common channel signalling and error detection functions for a 2.048Mbit PCM transmission link operating in accordance with the appropriate CCITT Recommendations. The MV1471 is also capable of operating at clock rates up to 10MHz. The MV1471 circuit is fabricated in CMOS and operates from a single +5V supply with all inputs and outputs being TTL compatible.

The MV1471 is an encoder/decoder for pseudo–ternary transmission codes. The code can be selected as either true Alternate Mark Inversion (AMI) code or AMI modified according to the HDB3 coding laws specified in Annex A of CCITT Recommendation G. 703. The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of the HDB3 coding and all ones detection. In addition a loop back function is provided for terminal testing.

FEATURES

- Single +5V supply
- All Inputs and Outputs TTL compatible
- Selectable HDB3 or AMI coding
- HDB3 Encoding and Decoding to CCITT Recommendation G. 703
- Simultaneous Encoding and Decoding
- Clock Recovery Signal allows Clock Regeneration from Incoming PCM data
- Loop Back Control
- HDB3 error monitor
- Alarm Indication Signal Monitor
- Low Power Operation
- 2.048MHz or 8.448MHz Operation

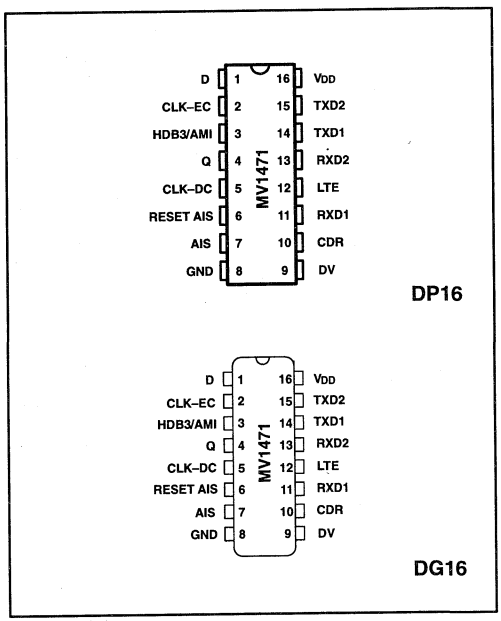


Fig. 1 Pin connections top view

ORDERING INFORMATION

MV1471/CG/DPAS
MV1471/CG/DGAS

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Supply Voltage	–0.5V to +7V
Input Voltage	–0.5V to V_{DD} +0.5V
Output Voltage	–0.5V to V_{DD} +0.5V
Storage temperature (DP)	–55 to +150°C
Storage temperature (DG)	–65 to +150°C

Functional Description

High density bipolar 3 (HDB3) is a ternary transmission code in which the number of consecutive zeros which may occur is restricted to three, to ensure adequate clock recovery at the receiver. In any sequence of four consecutive binary zero's, the last zero is substituted by a mark of the same polarity as the previous mark, thus breaking the Alternate Mark Inversion (AMI) code. This mark is termed a violation. In addition, the first zero may also be substituted by a mark if the last mark and last violation are of the same polarity. This mark does not violate the AMI code and ensures that successive violations alternate in polarity and as such introduce no DC components to the HDB3 signal.

The MV1471 consists of two main blocks, the HDB3/AMI Encoder and the HDB3/AMI Decoder, with the block diagram being shown in Fig. 2. The function of each block is now described separately.

HDB3/AMI Encoder

The HDB3/AMI Encoder is responsible for converting the incoming NRZ data into pseudo–ternary form for transmission over a 2.048Mbit/8.448Mbit PCM link according to either the true AMI rules or AMI modified according to the HDB3 encoding rules. In HDB3 mode, this conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G. 703, Annex A. Selection between the two encoding schemes is controlled by the HDB3/AMI control input. A logic high on this pin will configure the device in HDB3 mode.

The data to be encoded is input on the D input pin and the encoding process is synchronised to the 2.048/8.448MHz clock signal being input on the CLK–EC pin. The HDB3/AMI Encoder has two outputs, TXD1 and TXD2, which represent the encoded PCM data stream in pseudo–ternary form. If a mark or HDB3 violation is to be transmitted the output pulses high after the rising edge of the clock, with the length of the pulse set by the clock high pulse width. The timing diagram of the HDB3/AMI Encoder is shown in Fig. 3.

HDB3/AMI Decoder

The HDB3/AMI Decoder circuit is responsible for converting the 2.048Mbit/8.448Mbit HDB3/AMI encoded pseudo–ternary PCM data stream on its inputs, RXD1 and RXD2, into NRZ binary form to be output on the Q output pin. In HDB3 mode this conversion is carried out in accordance with the HDB3 coding laws specified in CCITT Recommendation G. 703, Annex A. The HDB3/AMI decoder synchronously decodes the data on its RXD input pins into NRZ form under control of the 2.048MHz/8.448MHz clock being input on its CLK–DC pin. There is a 5 clock period delay between the encoded data being clocked in from the RXD inputs and the NRZ data appearing on the Q output. The Decoder clock must be externally regenerated from the incoming PCM data streams and in order to aid this clock recovery a logical 'OR' function of the decoder inputs is output on the CDR pin.

In addition to the HDB3/AMI decoding the circuit also provides two alarm outputs. The first of these alarms is DV (Double Violation) and a logic high on this output denotes that two successive violations have been received with the same polarity, thus violating the HDB3 decoding laws. The second alarm output is AIS (Alarm Indication Signal). This output will go high if less than 3 decoded zero's have been detected in the preceding two RESET AIS=1 periods (i.e. between two RESET AIS=0 pulses) and as such this alarm can be used to detect the CCITT Alarm Indication Signal. All the alarm circuit as well as the decoding process is synchronised to the clock signal being input on the CLK–DC pin. The clock signal may by asynchronous with the CLK–EC signal. The timing diagrams of the HDB3/AMI Decoder circuit are shown in Fig.4. In addition to the normal mode of operation, a loop test mode is available for terminal testing. This mode is selected by taking the LTE (Loop Test Enable) input high. In this mode, the HDB3/AMI encoded pseudo–ternary data outputs of the encoder block are fed back as the inputs to the decoder block, which in turn decodes this data and outputs it in NRZ form.

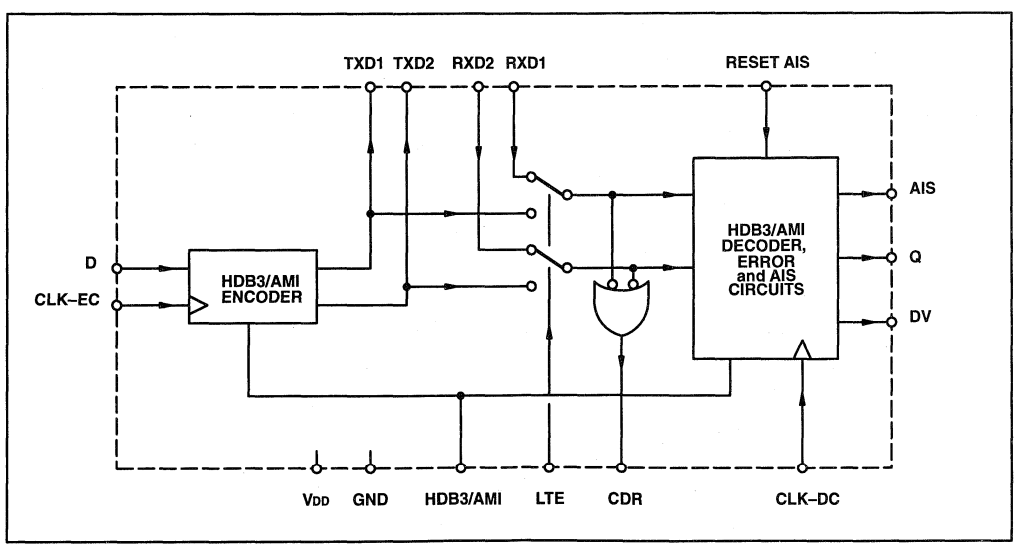
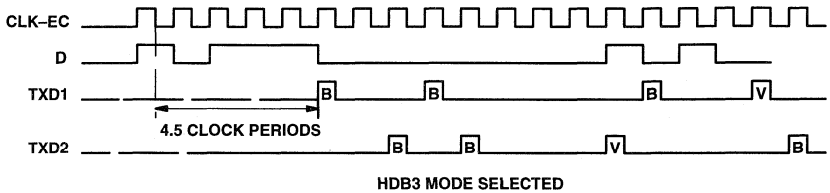
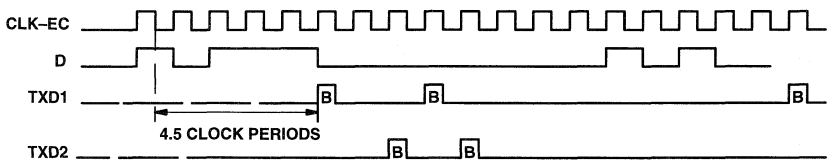


Fig. 2 Block diagram



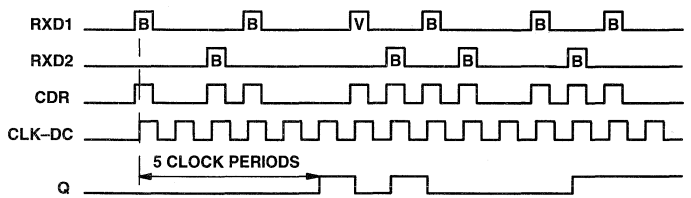
HDB3 MODE SELECTED



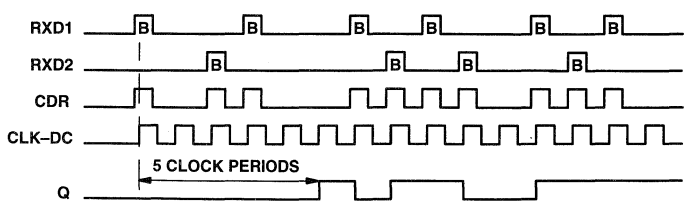
AMI MODE SELECTED

NOTES
1) The Encoder outputs, TXD1/2 are delayed by 4.5 clock periods with respect to D.
2) B is a HDB3 mark, V is a HDB3 violation.
3) Both diagrams assume the last mark occured on TXD2 and the last violation on TXD1.

Fig. 3 HDB3/AMI Encoder waveforms



DECODER WAVEFORMS – HDB3 MODE SELECTED



DECODER WAVEFORMS – AMI MODE SELECTED

NOTES
1) The decoder NRZ output is delayed by 5 clock periods with respect to the PCM inputs.
2) B is a HDB3 mark, V is a HDB3 violation.
3) The diagrams assume that the last mark and last violation both occured on RXD2.

Fig. 4 HDB3/AMI Decoder waveforms

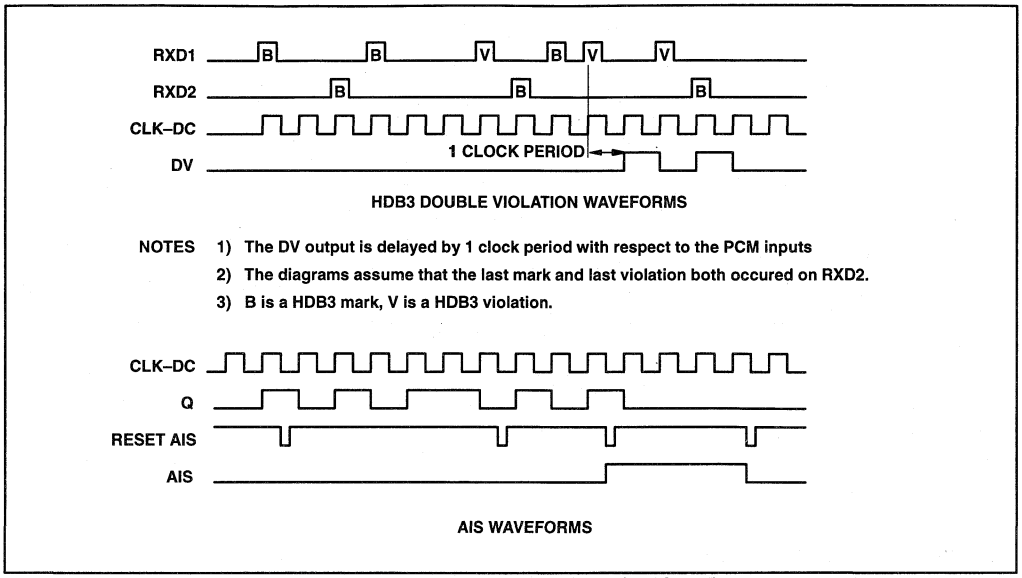


Fig. 4 HDB3/AMI Decoder waveforms ***(continued)***

PIN DESCRIPTION

Pin Name	Pin No	Description
D	1	NRZ Data Input pin to HDB3/AMI Encoder. The NRZ binary data on this pin is input to the HDB3/AMI Encoder for conversion to HDB3/AMI pseudo–ternary form under control of the CLK–EC signal. The D input is latched into the encoder block by the falling edge of CLK–EC.
CLK–EC	2	2.048MHz Clock Input to HDB3 Encoder. The clock signal on this input is used for the encoding of data on pin 1.
HDB3/AMI	3	HDB3/AMI Mode Select Input. A logic high on this pin selects HDB3 operation. A logic low selects AMI mode.
Q	4	NRZ Data Output from HDB3/AMI Decoder. This output represents the HDB3/AMI input data decoded back into NRZ binary form, with a 5 clock period delay from the PCM inputs to the NRZ output. This decoding process is carried out under control of the CLK–DC signal.
CLK–DC	5	2.048MHz Clock Input to HDB3/AMI Decoder. The clock signal on this pin is used for decoding of data on the RXD input pins, or the TXD pins in Loop Test Mode. This pin is used to input the externally regenerated clock signal recovered from the incoming HDB3/AMI waveforms back to the decoder block.
RESET AIS	6	Reset AIS Input to HDB3/AMI Decoder. A logic '0' on this input resets a decoded zeros counter in the HDB3/AMI decoder. It will also reset the AIS output to '0' provided 3 or more zeros have been decoded in the preceding RESET AIS=1 period, or set AIS to '1' if less than 3 zeros have been decoded in the preceding two RESET AIS=1 periods. This may be used to detect the CCITT Alarm Indication Signal. A logic '1' on this pin enables the decoded zeros counter.
AIS	7	Alarm Indicator Signal Output from HDB3/AMI Decoder. See description for RESET AIS pin.
GND	8	Digital Ground. 0V.
DV	9	Double Violation Alarm Output from HDB3/AMI Decoder. This output goes high for one period of CLK–DC, one period after the detection of a HDB3 violation of the same polarity as the previous HDB3 violation.
CDR	10	Clock Recovery Output from HDB3/AMI Decoder. This pin is used to output the logical 'OR' function of the PCM inputs for the use of the external clock recovery circuit.

RXD1	11	HDB3/AMI Encoded Input 1 to HDB3/AMI Decoder. This is one of the pair of 2.048Mbit/8.448Mbit pseudo–ternary PCM data stream inputs to the HDB3/AMI Decoder. This input asynchronously latches the incoming HDB3/AMI data and is rising edge sensitive. Since the input is asynchronously latched it is not necessary for the RXD pulse to straddle a rising clock edge.
LTE	12	Loop Test Enable Control Input. A logic low on this pin selects normal operation, with encoding and decoding being independent and asynchronous. A logic high on this pin internally connects TXD1 to RXD1 and TXD2 to RXD2. Note that in loop back mode, a decoder clock must be supplied.
RXD2	13	HDB3/AMI Encoded Input 2 to HDB3/AMI Decoder. See description for pin RXD1.
TXD1	14	HDB3/AMI Encoded Pseudo–Ternary Output 1 from HDB3/AMI Encoder. The NRZ PCM data stream being input on the D pin is HDB3/AMI encoded and output on this pin and pin TXD2. This output is always low during the low half cycle of clock and is only high during the high half cycle of clock if a mark is to be output. There is a 4.5 clock period delay from the falling edge of CLK–EC to TXD1.
TXD2	15	HDB3/AMI Encoded Pseudo–Ternary Output 1 from HDB3/AMI Encoder. See Pin TXD1 description.
VDD	16	Digital Supply Voltage. 5V.

NOTES

1. All inputs except HDB3/AMI have 100K on–chip pull down resistors. HDB3/AMI has a 100K on–chip pull–up resistor.

ELECTRICAL CHARACTERISTICS

Test Conditions

Supply Voltage V_{DD} = 5V ±0.5V Ambient Temperature T_{amb} = 0°C to + 70°C

STATIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Low level input voltage	V_{IL}	0.0		0.8	V	
High level input voltage	V_{IH}	2.0		V_{DD}	V	
Low level output voltage	V_{OL}			0.4	V	I_{sink} = 2mA
High level output voltage	V_{OHT}	2.4			V	I_{source} = 2mA
	V_{OHC}	V_{DD}–1.0			V	I_{source} = 1mA
Input leakage current	I_{IL}	–10		200	µA	V_{in} = V_{DD} or GND
Supply current	I_S			5	mA	2.048MHz operation Note 1.
				15	mA	8.448MHz operation Note 1.
Input capacitance	C_{IN}		5		pF	All inputs
Output capacitance	C_{OUT}		5		pF	All outputs

NOTES

1. All supply currents measured with outputs unloaded. These currents are not tested but are guaranteed by characterisation and a static current test.

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
CLOCK						
Clock period	t_{CP}	100			ns	See Fig. 5
Clock rise/fall time	t_{CR}/t_{CF}			20	ns	See Fig. 5
Clock high/low time	t_{CH}/t_{CL}	30			ns	See Fig. 5

(cont.)DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
ENCODER						
Encoder data setup time	t_{EDS}	15			ns	See Fig. 6
Encoder data hold time	t_{EDH}	15			ns	See Fig. 6
TXD1/TXD2 output propagation delay	t_{EPDR} t_{EPDF}			45	ns	See Fig. 6, Note 1.
DECODER						
RXD1/2 data setup time	t_{RS}	20			ns	See Fig. 7
RXD1/2 pulse width	t_{RW}	20			ns	See Fig. 7
CDR propagation delay	t_{CPDR}/ t_{CPDF}			45	ns	See Fig. 7, Note 1.
Decoder output propagation delay	t_{OPD}			45	ns	See Fig. 7, Note 1.and 2.
RESET AIS hold–off time	t_{RAHO}	15			ns	See Fig. 7
RESET AIS pulse width	t_{RAW}	15			ns	See Fig. 7
Reset AIS setup time	t_{RAS}	10			ns	See Fig. 7
AIS propagation delay	t_{APD}			55	ns	See Fig. 7, Note 1.

NOTES

1. All output propagation delays are measured with a 50pF load.
2. The t_{OPD} parameter applies to outputs Q, and DV, but does not apply to AIS.

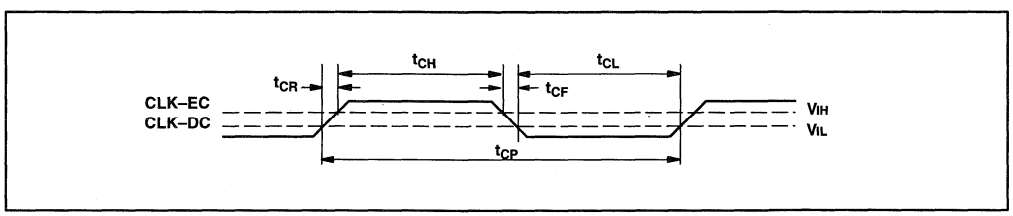


Fig. 5 Clock timing parameters

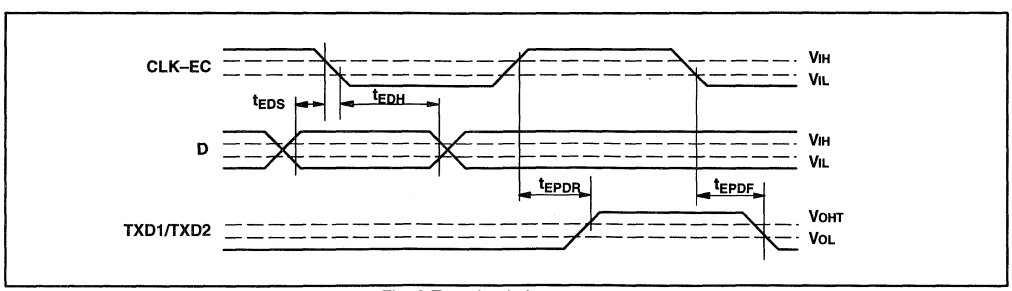


Fig. 6 Encoder timing parameters

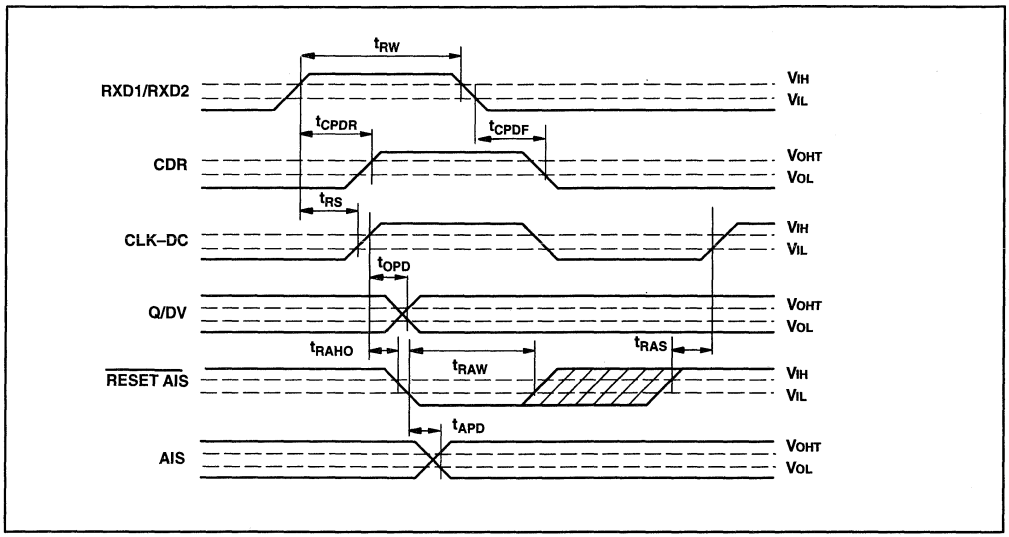


Fig. 7 Decoder timing parameters

PCM MACROCELLS

2.048MBit PCM-30 MACROCELLS for HDB3, CRC, TSO & TS16 FUNCTIONS

The following information outlines the functions available from a family of Telecom PCM Macrocells, contained within GEC Plessey Semiconductors' CLA60000 Semi-custom library. These cells have been designed around the most important functions required by a 2.048MBit PCM link operating in accordance with appropriate CCITT Recommendations. It is intended that these macrocells can be used in custom designs using the CLA60000 cell library, in the same manner as for the GPS MV1403 PCM Demonstrator chip. More information on the operation of each macrocell can be found in the descriptions contained in the MV1403 data sheet (page 2-33). For detailed data on each macrocell, reference should be made to the CLA60000 Design Manual.

TRANSMIT FUNCTIONS

The following macrocells provide the stated functionality for the transmit side of a PCM-30 link :-

TXTSZ = Time Slot Zero generator.
TXTS16 = Time Slot 16 data generator.
HDB3EC = High Density Bipolar 3 Encoder.
CRCGEN = Cyclic Redundancy Check data generator.

TXTSZ FEATURES

- Generates Time Slot Zero Sync Pattern.
- Inserts Signalling Data into the Spare Bits of TS0.
- Meets CCITT Recommendation G.704.
- Sync and Non-sync Identification Output.
- Scan Path Testability.

TXTS16 FEATURES

- Receives Signalling Data at 64kHz.
- Transmits Signalling Data at 2.048MHz in TS16.
- Derives TS16 Marker Output.
- Scan Path Testability.

HDB3EC FEATURES

- Inputs Data at 2.048MHz NRZ.
- Transmits Data as Pseudo-Ternary HDB3.
- Meets CCITT Recommendation G.703.
- Input NRZ Data Delayed Output.
- Scan Path Testability.

CRCGEN FEATURES

- Inputs Data at 2.048MHz NRZ.
- Generates 4 Bit CRC Data.
- Generates 6 Bit CRC Multiframe Sync Word with 2 User-Defined Data Bits.
- CRC or Signalling Data Inserted into TS0 Bit 1.
- Meets CCITT Recommendation G.704.
- Scan Path Testability.

RECEIVE FUNCTIONS

The following macrocells provide the stated functionality for the receive side of a PCM-30 link :-

RXTSZ = Time Slot Zero Receiver.
RXTS16 = Time Slot 16 data Receiver.
HDB3DC = High Density Bipolar 3 Decoder.
CRCCHK = Cyclic Redundancy Check data tester.

RXTSZ FEATURES

- Receives 2.048MBit Data Stream.
- Detects Time Slot Zero Sync Pattern.
- Meets CCITT Recommendation G.732.
- Time Slot Zero & Sync Frame Marker Outputs.
- Error, Loss of Sync & Remote Alarm Outputs.
- Extracts Signalling Data from TS0.
- Outputs 4KHz and 8KHz Clocks.
- Scan Path Testability.

RXTS16 FEATURES

- Receives Signalling Data at 2.048MHz in TS16.
- Outputs Signalling Data at 64kHz.
- Scan Path Testability.

HDB3DC FEATURES

- Receives Data as Pseudo-Ternary HDB3.
- Outputs Data at 2.048MHz NRZ.
- Meets CCITT Recommendation G.703.
- Double Violation & Loss Of Input Alarm Outputs.
- Outputs Logical 'OR' of Input Data to Assist Clock Recovery.
- Scan Path Testability.

CRCCHK FEATURES

- Input Data at 2.048MHz NRZ.
- Detects 6 Bit CRC Multiframe Sync Word & Outputs 2 User-Defined Data Bits.
- Compares Generated & Input CRC Check Data.
- Multiframe Sync Alarm & CRC Error Outputs.
- Outputs Frame 13 & Frame 15 Markers.
- Scan Path Testability.

MV1403

PCM MACROCELL DEMONSTRATOR

The MV1403 contains 8 PCM macrocells which can be configured so as to perform the common channel signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link, operating to the appropriate CCITT recommendations. The MV1403 also allows access to all the macrocells individually and is implemented in GPS CMOS technology utilising the CLA60000 series gate array, offering high performance, low power and fast turn-round. The following macrocells are included in the MV1403.

Timeslot Zero Transmitter - **TXTSZ**
Timeslot Sixteen Transmitter - **TXTS16**
Cyclic Redundancy Check Generator - **CRCGEN**
High Density Bipolar (HDB) 3 Encoder - **HDB3EC**
Timeslot Zero Receiver - **RXTSZ**
Timeslot Sixteen Receiver - **RXTS16**
Cyclic Redundancy Checker - **CRCCHK**
High Density Bipolar (HDB) 3 Decoder - **HDB3DC**

With the MV1403 set up to combine the internal macrocells, two demonstration modes are available, referred to as Transmit and Receive demonstration modes.

In Transmit demonstration mode, timeslot zero sync word (including user data bits and optional CRC check bits), timeslot sixteen data and 30 voice channels are combined and transmitted as pseudo-ternary HDB3 encoded outputs. The Transmit demonstration mode can also be set to generate CRC multiframe data in accordance with CCITT Recommendation G. 704.

In Receive demonstration mode, the pseudo-ternary HDB3 inputs are decoded back to NRZ form and frame synchronisation is achieved by detection of the Frame Alignment signal in the incoming data stream. This permits extraction of user data bits, timeslot sixteen data and voice channel data. An optional CRC mode generates CRC multiframe alignment and a cyclic redundancy check is carried out on the incoming data. In addition receive demonstration mode generates appropriate alarms for loss of input, double violation on the HDB3 inputs, loss of frame or CRC multiframe alignment, detection of erroneous frame alignment word, remote alarm received from the transmitter, and detection of a CRC error in either submultiframe 1 or 2.

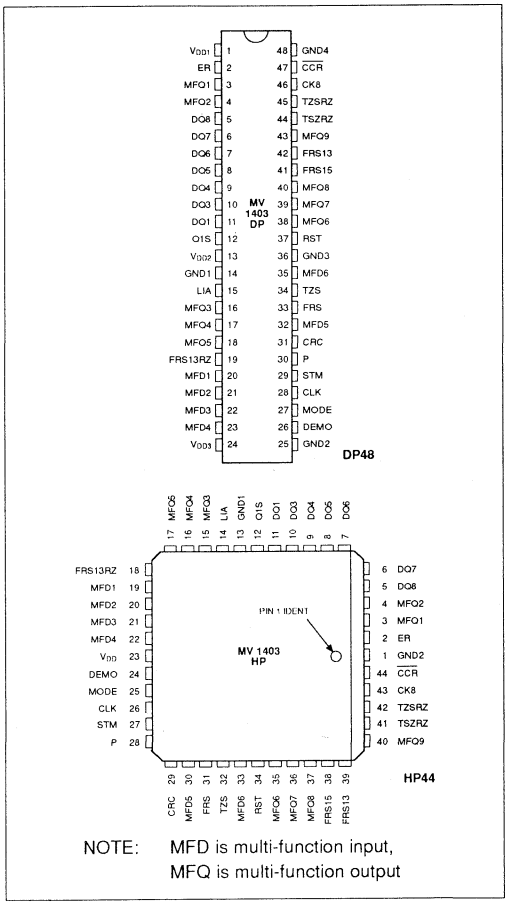


Figure 1: Pin connections - top view

FEATURES

- Single + 5V Supply
- All Inputs and Outputs TTL Compatible
- Selectable as PCM Transmitter or Receiver
- Allows Access to all 8 Macrocells Individually
- HDB3 Encoding and Decoding to CCITT Recommendation G. 703
- Transmitted Frame Structure to CCITT Recommendation G. 704
- Receiver Frame Synchronisation to CCITT
- Recommendation G. 732
- Selectable CRC Mode
- CRC Generation and Checking to CCITT Recommendation G. 704

FUNCTIONAL DESCRIPTION

The MV1403 PCM macrocell demonstrator contains a family of 4 Transmit PCM and 4 Receive PCM macrocells which may be configured to function individually, or be connected together to form demonstrations of their operation. In order to keep the pin count to a minimum, some of the input and output pins are shared. Pin functions thus depend upon whether the device is configured as a transmitter or receiver. The operational modes of the MV1403 are selected under control of the MODE and DEMO pins, as shown in Table 1. Note that the MODE pin selects either the transmit or receive set of macrocells and that the DEMO pins selects either individual or combined connections.

In addition the operation of the MV1403 is controlled by a further two control inputs, STM and CRC. The STM pin is used for device testing and should be tied low for normal operation. The CRC control pin selects whether or not the device-performs the CRC generation/checking procedure. A logic High' on this pin puts the device in Cyclic Redundancy Generate/Check mode.

More detailed information about all 8 macrocells can be found in the individual macrocell publications.

INDIVIDUAL TRANSMIT MODE, TX1

In this mode (MODE = 0, DEMO = 0) the four transmitter macrocells (TXTSZ, TXTS16, CRCGEN and HDB3EC) are all accessed individually. The functional diagram of the MV1403 in this mode is shown in Fig. 2. All four macrocells are synchronised to a common 2.048MHz clock, and the TXTSZ, TXTS16 and CRCGEN macrocells are also synchronised to a second timing input, FRS (Frame Sync). This is an 8 clock period high going pulse at 8kHz which masks timeslot zero to enable frame alignment. The function of each transmit macrocell is now described separately.

TIMESLOT ZERO TRANSMITTER

The Timeslot Zero Transmitter macrocell generates a Frame Alignment Signal (FAS) in accordance with CCITT Recommendation G. 704. This is combined with the international spare bit (the D1 input) and output on Q during timeslot zero of alternate frames, denoted sync frames. During the other interleaved frames, denoted non-sync frames, bit 2 is fixed at logic 1 to avoid imitation of the FAS. This bit is slotted together with the international spare bit (D1 input) and 6 user data bits (the D3N-D8N inputs) for output on Q.

A TZS output (Timeslot Zero Sync frame) is provided to denote whether a sync frame or non-sync frame is being output. It changes state one clock period after the end of timeslot zero and is high during timeslot zero of sync frames.

Fig. 3 shows the timing diagram for this macrocell.

TIMESLOT SIXTEEN TRANSMITTER

This macrocell takes in a continuous 64kbit data stream (D input) and outputs it in 8 bit packets at a bit rate of 2.048 Mbit during timeslot 16 of successive frames on its Q output. The position of timeslot 16 is determined from the FRS timing input, which masks timeslot zero. The TS16 output is an 8 clock period high going pulse at 8kHz, similar to FRS, but high during the 8 bits of timeslot sixteen.

Fig. 4 shows the timing diagram for this macrocell.

CYCLIC REDUNDANCY CHECK GENERATOR

This macrocell has two modes of operation, selected by its EN control input. When EN is 'high', CRC generation mode is selected. However, both modes are concerned with producing the data bit to be inserted into the international spare bit of timeslot zero (CCITT G. 704 structure). In non-CRC mode, this data is selected to be either the D1S (sync frames) or DIN (non-sync frames) input depending upon whether a sync or non-sync frame is about to be transmined (determined by the TZS input).

With CRC mode enabled, the macrocell generates CRC words and outputs this data during the international spare bit of sync frames. During non-sync frames, the 6 bit CRC Multiframe Alignment Signal is output along with the two user data inputs, DIS and D1N. This procedure is carried out in accordance with CCITT Recommendation G. 704. The CRC word is generated from the incoming data stream on the D input pin. CCITT Recommendation G. 704 defines the 16 frame CRC multiframe structure, not related to the possible use of a 16 frame multiframe structure in timeslot 16. Each 16 frame CRC multiframe is divided into two 8 frame sub-multiframes, denoted submultiframes 1 and 2 (SMF1 and SMF2). The CRC procedure is carried out on each sub-multiframe of data and the resulting 4 bit CRC word is output during the international spare bit of sync frames during the following sub-multiframe. All data is output on the Q output pin. Table 2 displays the CRC multiframe structure in more detail .

HIGH DENSITY BIPOLAR (HDB3)ENCODER

The HDB3 Encoder macrocell converts the incoming NRZ data on its D input pin into HDB3 pseudo-ternary form for transmission over a 2.048 Mbit PCM link in accordance with CCITT Recommendation G.703. The two TXD outputs represent the HDB3 data in pseudo-ternary form. They are always low during the high half cycle of CLK, but may be high or low during the low half cycle. The Q output represents the D input but delayed by one period. Fig. 5 shows the timing diagram of this macrocell.

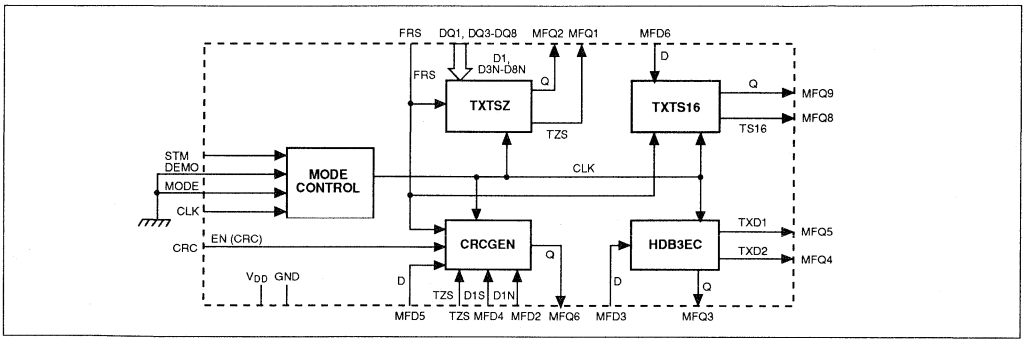


Figure 2: TX1 Individual Transmit mode functional diagram

Mode Name	MODE input	DEMO input	CRC input	STM input	Mode description
TX1	0	0	0/1	0	MV 1403 is configured as individual Transmit PCM macrocells
TX2	0	1	0/1	0	MV1403 is configured as a PCM Transmitter demonstration, using the Transmit macrocells
RX1	1	0	0/1	0	MV1403 is configured as individual Receive PCM macrocells
RX2	1	1	0/1	0	MV1403 is configured as a PCM Receiver demonstration, using the Receive macrocells
TX1/2	0	0/1	0	0	CRC generation mode of the CRCGEN macrocell is disabled
TX1/2	0	0/1	1	0	CRC generation mode of the CRCGEN macrocell is enabled
RX1/2	1	0/1	0	0	CRC mode of the RXTSZ macrocell is disabled
RX1/2	1	0/1	1	0	CRC mode of the RXTSZ macrocell is enabled
-	X	X	X	1	MV1403 is configured in device test mode. This mode should not be used for normal operation

Table 1: Operational modes of the MV1403

	CRC Multiframe															
	Sub-Multiframe 1 (SMF1)								Sub-Multiframe 2 (SMF2)							
Frame number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit one of timeslot zero	C1	0	C2	0	C3	1	C4	0	C1	1	C2	1	C3	D1S	C4	D1N

NOTES:
1. C1, C2, C3, C4 are the bits of the CRC word.
2. 001011 is the CRC Multiframe Alignment Signal (MAS).
3. Even numbered frames are denoted Sync frames; odd numbered frames are denoted non-sync frames.

Table 2: Structure of the CCITT CRC Multiframe

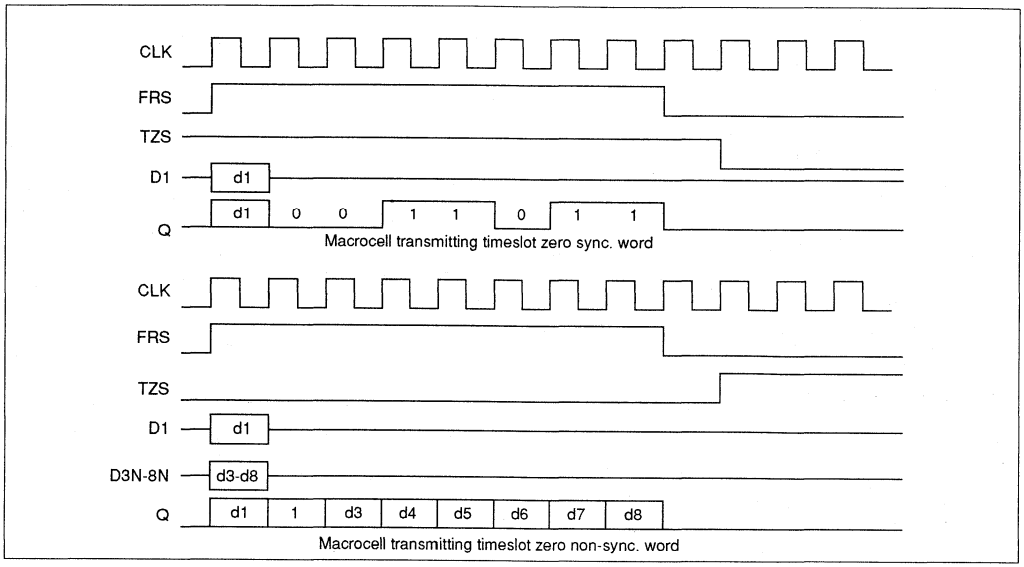


Figure 3: Timeslot zero transmitter timing

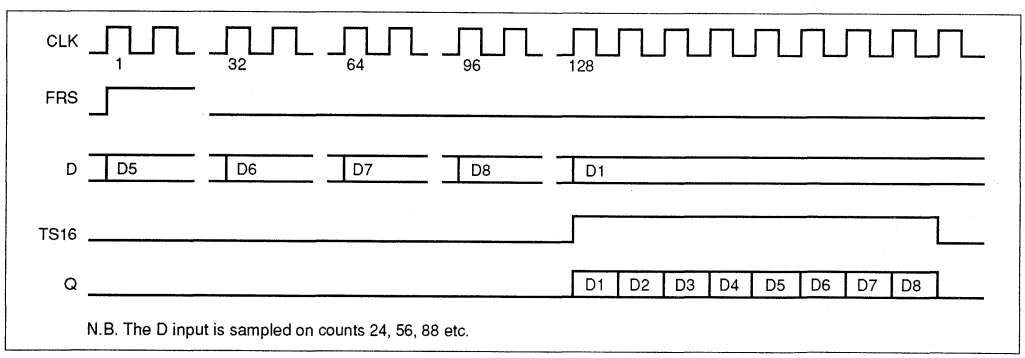


Figure 4: Timeslot sixteen transmitter timing

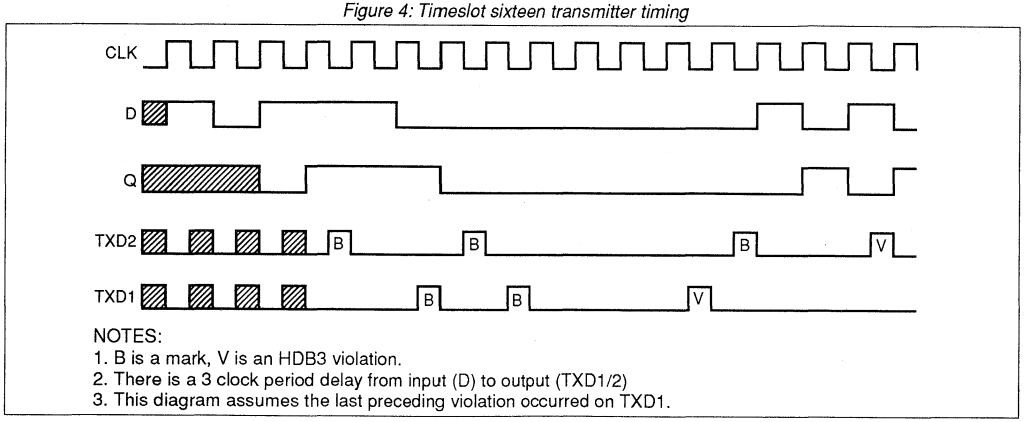


Figure 5: HDB3 encoder timing

TRANSMIT DEMONSTRATION MODE, TX2

Transmit demonstration mode (MODE =0, DEMO= I) uses the four transmitter macrocells connected together internally, to demonstrate how they may be utilised to perform the common channel signalling and error detection functions of a 2.048 Mbit 30 channel PCM transmitter. The functional diagram of the MV1403 in this mode is now as shown in Fig. 6. Again all four macrocells are synchronised to a common 2.048MHz clock with frame synchronisation achieved from the FRS input.

The Timeslot Zero transmitter alternately outputs sync words and non-sync words, during timeslot zero, denoting which by its TZS output. The user data bits of the nonsync word (D3N-D8N) are available as parallel data inputs. The Timeslot Zero data is used as one of the inputs to the transmission multiplexer.

The Timeslot Sixteen transmitter takes in the continuous 64kbit data stream from its D input and outputs this in 8 bit bursts during timeslot 16. This data along with the TS16 frame marker are also used as inputs to the transmission multiplexer, TMUX.

The transmission multiplexer forms a single PCM data stream at its Q output by multiplexing the timeslot zero and timeslot 16 data with the remaining 30 channels (timeslots 1-15 and 17-31) of voice data. This is controlled by the two frame marker inputs to the multiplexer, FRS and TS16.

The output from TMUX is input to the Cyclic Redundancy Check Generator and HDB3 Encoder macrocells.

When in CRC mode (EN=1), the CRC Generator macrocell performs its CRC procedure on this incoming data stream. In non-CRC mode, this macrocell uses its two data inputs, D1S and D1N, along with the timing input, TZS, to determine its output. However, in CRC mode the output consists ol the CRC word data bits interleaved with the CRC multiframe alignment word and the two user data bits, D1S and D1N, as previously displayed in Table 2. In either case, the output data is input directly to the international spare bit input of the Timeslot Zero Transmitter. The TZS input of the CRC generator is connected directly to the TZS output of the Timeslot Zero Transmitter.

The output data from the transmission multiplexer is also input to the HDB3 Encoder macrocell. This macrocell converts the incoming NRZ data into pseudo-ternary HDB3 transmission code, ensuring adequate clock recovery at the receiver. This data is output on the TXD1 and TXD2 output pins. The Q output of the HDB3 Encoder macrocell is a single period delayed version of its D input and as such allows the output from the transmission multiplexer to be observed.

Fig. 6 shows that all of the intemal connections except the output from TMUX, are also available as outputs from the MV1403, allowing the interaction of the rnacrocells to be observed.

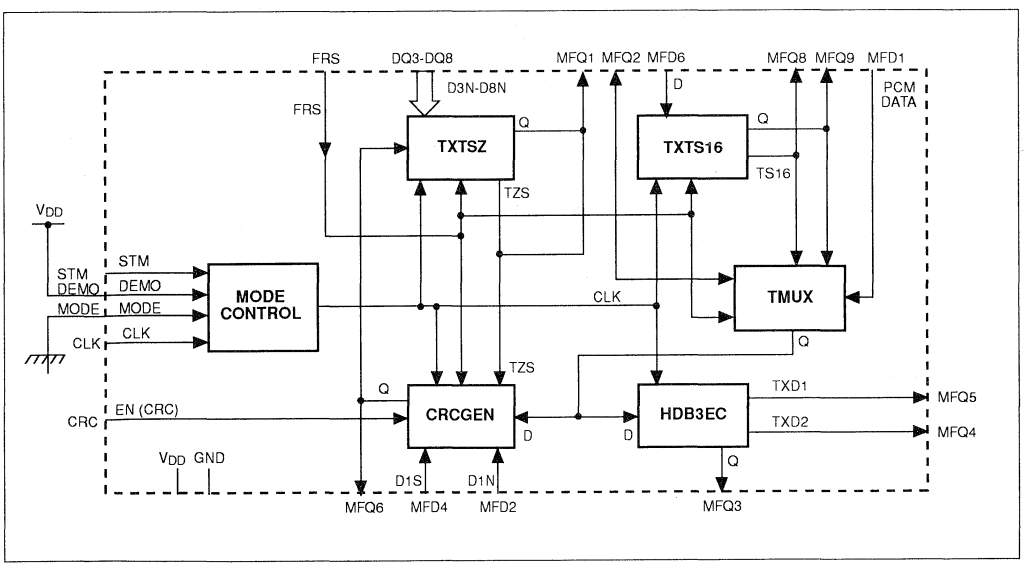


Figure 6: TX2 Transmit demonstration mode functional diagram

INDIVIDUAL RECEIVE MODE, RX1

In this mode (MODE = 1, DEMO = 0) the MV1403 allows access to the four receiver macrocells (HDB3DC, RXTSZ, RXTS16 and CRCCHK) individually. The functional diagram for the MV1403 in RX1 mode is shown in Fig. 7. The only common connection between the macrocells is the 2.048MHz clock used to synchronise the four macrocells. The function of each individual macrocell is now described separately.

High Density Bipolar (HDB3) Decoder

The HDB3 decoder macrocell decodes the HDB3 pseudo-ternary input data on its inputs, RXD1 and RXD2, into NRZ form to be output on a This process is carried out in accordance with CCITT Recommendation G. 703. In addition the macrocell provides two alarm outputs, DV and LIA and a clock recovery output, CDR.

The first of these, DV, is used to signal that a double polarity violation has occurred on one of the pseudo-ternary inputs, whilst the second, LIA (Loss of Input Alarm), signals that eleven consecutive zeros have been received on the inputs. The CDR output is provided to assist regeneration of the 2.048MHz clock. This output is essentially just a logical 'OR' function of the two RXD inputs.

Since either a regenerated clock from the input data or a clock local to the PCM receiver may be used to synchronise the receiver, the two input signals cannot be guaranteed to straddle a rising clock edge and as such the two inputs were made asynchronous by the use of set-reset type latches before the first synchronous storage elements on the inputs.

However, to ensure correct operation of the macrocell the rising edge of either of the RXD inputs should not occur within 50ns of the rising edge of CLK. The timing diagram for this macrocell is shown in Fig. 8.

Timeslot Zero Receiver

This macrocell is principally responsible for searching for and locking on to the Frame Alignment Signal (FAS) present in timeslot zero of the incoming data stream on the D input. This process is carried out in accordance with the loss and recovery of frame alignment strategy described in CCITT Recommendation G.732. When frame alignment has been achieved this macrocell outputs various timing reference signals for use by the other macrocells and external circuitry.

The most important reference signal is the TSZ (Timeslot Zero) output, which is equivalent to the FRS input signal required by the transmitter macrocells. It is an 8 clock period long active high pulse masking Timeslot Zero, allowing the other macrocells to achieve frame alignment. This output will free run when frame alignment is lost. The second timing output is TZS (Timeslot Zero Sync. frame). This 4kHz signal changes state once per frame, one period after the end of Timeslot Zero to identify sync and non sync frames. The TZS output is high during Timeslot Zero of sync frames.

Two timing outputs, $\overline{CCR}$ (Channel Reset) and CK8, are not used by the other macrocells but may be used by external circuitry. $\overline{CCR}$ is a low going pulse, one period wide, occurring immediately after each timeslot zero sync frame. CK8 is an 8kHz signal going low at the end of bit 7 in each timeslot zero and high at the end of bit 7 in each timeslot sixteen. The TZS, CK8 and $\overline{CCR}$ outputs also free run when frame alignment is lost.

Two alarm outputs are provided to signal errors in the incoming data stream. The first of these, is an error alarm, ER, which goes high for one frame following the frame in which a Timeslot Zero sync word, containing a corrupted alignment pattern, has been received. This alarm is only active whilst the receiver is in sync. Note that three consecutive errors of this type will put the receiver out of sync. Thus the second alarm output, SA (Sync. Alarm), goes high when the receiver is out of sync. In additon to the frame synchronisation process, the Timeslot Zero Receiver is also responsible for extracting the user data bits of non-sync words and the two international spare bits. The former of these are accessed via the parallel outputs Q3N-Q8N. The third bit of non-sync words (Q3N) is used as the remote alarm bit from the transmitter and a third alarm output RAI (Remote Alarm Indication), is derived from this bit. This alarm is a persistence checked version of Q3N and when the receiver is in sync, this alarm goes high when two consecutive (Q3N bits have been received as high.

In order to extract the international spare bits of Timeslot Zero, the macrocell must be in sync with CRC mode correctly enabled or disabled. This is done using the M input with a logic 'high' on this pin putting the macrocell in CRC mode.

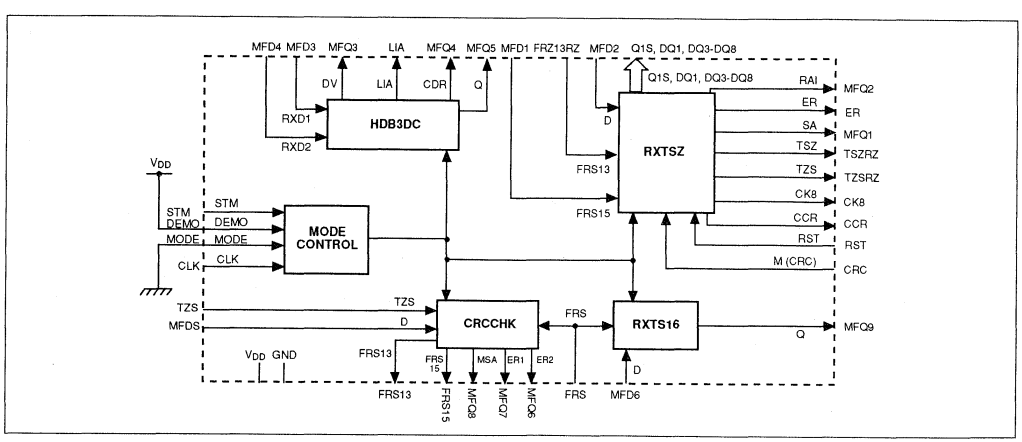
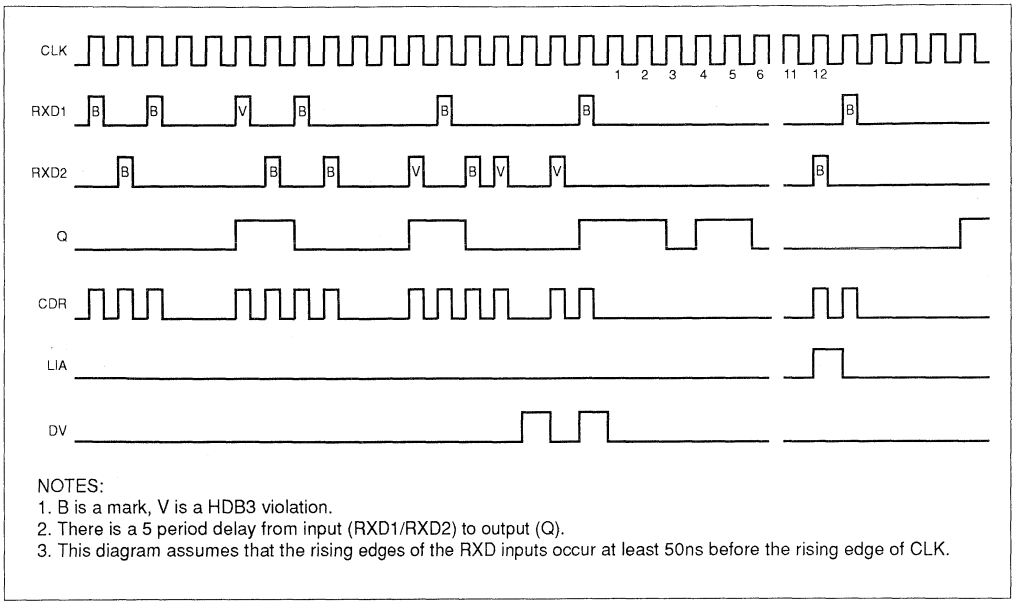


Figure 7: RX1 individual receive mode functional diagram



NOTES:
1. B is a mark, V is a HDB3 violation.
2. There is a 5 period delay from input (RXD1/RXD2) to output (Q).
3. This diagram assumes that the rising edges of the RXD inputs occur at least 50ns before the rising edge of CLK.

Figure 8: HDB3 decoder timing - macrocell decoding HDB3 data and detecting errors

When in non CRC mode the international spare bit outputs, Q1S and Q1N, represent data extracted from the bit position of all sync frames and non-sync. frames respectively. If CRC mode is enabled, these outputs now represent data extracted from the bit 1 position of frames 13 and 15 respectively of the CRC multiframe structure. In order to accomplish this, two timing inputs, FRS13 and FRS15, are required. These inputs are required to be high during bit 8 of the appropriate frame, low during bit 8 of any other non-sync frame and any state elsewhere. A final input to this macrocell, RST, may be used to reset the synchronisation process, putting the macrocell out of sync. Timing diagrams for the Timeslot Zero P(eceiver macrocell are shown in Fig. 10.

Timeslot Sixteen Receiver

The Timeslot Sixteen Receiver macrocell extracts the 8 bits of common channel signalling data present in Timeslot 16 of successive frames of PCM data input on D. This 2.048Mbit input data burst is stored and output as a continuous 64kbit data stream. A single timing input, FRS, also common to the CRCCHK macrocell, is required, this input being an 8 bit pulse masking Timeslot Zero. Fig. 9 shows the timing of this macrocell.

Cyclic Redundancy Checker

The Cyclic Redundancy Checker macrocell (CRCCHK) performs a cyclic redundancy check procedure on the received data in accordance with CCITT Recommendation G.704, this procedure being performed on the data input on its D input pin. The macrocell also extracts the first bit of each Timeslot Zero (the first bit of each frame) and searches for the CRC Multiframe Alignment Signal (MAS) in the bits from non-sync frames.

When the MAS has been found the macrocell synchronises to it. This process requires two timing inputs, FRS and TZS. The FRS input must be high only during timeslot zero and TZS must be high during timeslot zero of sync frames.

The macrocell generates CRC words from the input data and extracts the CRC bits being received in the first bit of sync frames. Each generated CRC word is compared with the CRC word received in the next sub-multiframe. Associated with this process are three alarm outputs, MSA, ER1 and ER2. The MSA (Multiframe Sync Alarm) output indicates whether multiframe synchronisation has occured. It is high whilst the macrocell is out of sync, and goes low after the beginning of frame 11 in which a correct alignment pattern has been received. The two error outputs, ER1 and ER2 indicate that CRC errors were detected in submultiframes 1 and 2 respectively. These two outputs can only change state on the first rising clock edge after the first bit of frames 0 and 8 respectively.

When in CRC multiframe alignment, the macrocell also produces two timing outputs, FRS13 and FRS15, to reference the positions of frames 13 and 15. These signals may be used to allow the Timeslot Zero Receiver macrocell to extract the international spare bits of these frames.

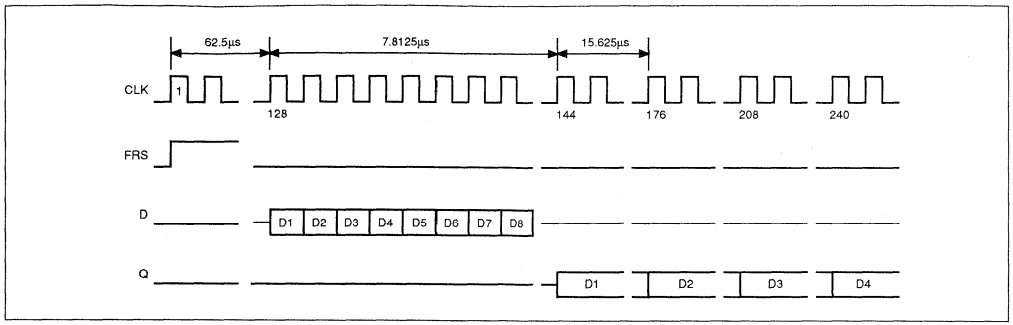


Figure 9: Timeslot sixteen receiver timing

RECEIVE DEMONSTRATION MODE, RX2

In the last mode (MODE = 1, DEMO = 1) the four receiver macrocells are connected together internally to demonstrate how they may be utilised to perform the required functions of a 2.048 MBit PCM receiver. The functional diagram of the MV1403 will now be as shown in Fig. 11.

The received pseudo-ternary HDB3 data is input to the HDB3 Decoder macrocell, which decodes this data and outputs it to the other three macrocells and external circuitry, as well as raising appropriate alarms as previously described for the individual receive mode.

The Timeslot Zero Receiver then synchronises itself to the Frame Alignment Signal present in this data stream and produces various timing outputs tor use by the remaining two receiver macrocells and external circuitry. In addition this macrocell also raises appropriate alarms as required.

The data being output by the HDB3 decoder is used as the D input to the Timeslot 16 Receiver macrocell which also uses the Timeslot Zero Receiver's TSZ output as its FRS timing input. From this the macrocell determines the position of timeslot 16 and extracts the 8 bits of signalling data from this timeslot. This data is then converted into a continuous 64kbit output data stream.

The Cyclic Redundancy Checker macrocell uses the HDB3 Decoder's output data and the Timeslot Zero Receivers timing outputs TSZ and TZS as its D, FRS and TZS inputs respectively. From this information the macrocell synchronises itself to the CRC multiframe alignment signal and performs its CRC check procedure on the incoming data. Its two timing outputs, FRS13 and FRS15, are input to the Timeslot Zero Receiver to allow it to extract the international spare bits of the CRC multiframe.

In non CRC mode, the Cyclic Redundancy Checker's error outputs are disabled by the alarm gating circuitry. When in CRC mode, this circuitry will also disable the ER1 and ER2 alarms whilst the macrocell is out of multiframe alignment.

In addition to the required outputs, all the internal timing signals are also available as outputs from the MV1403, allowing the interaction of the macrocells to be observed.

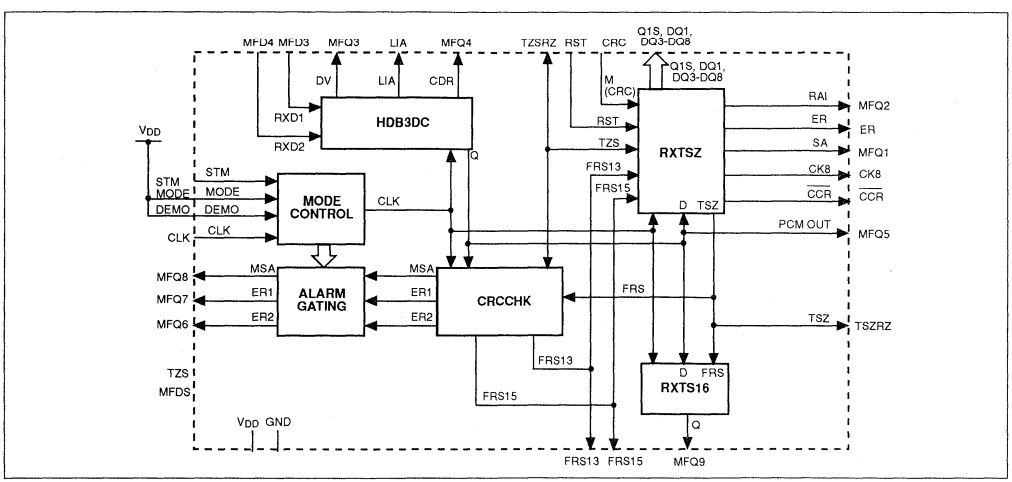


Figure 11: RX2 receive demonstration mode functional diagram

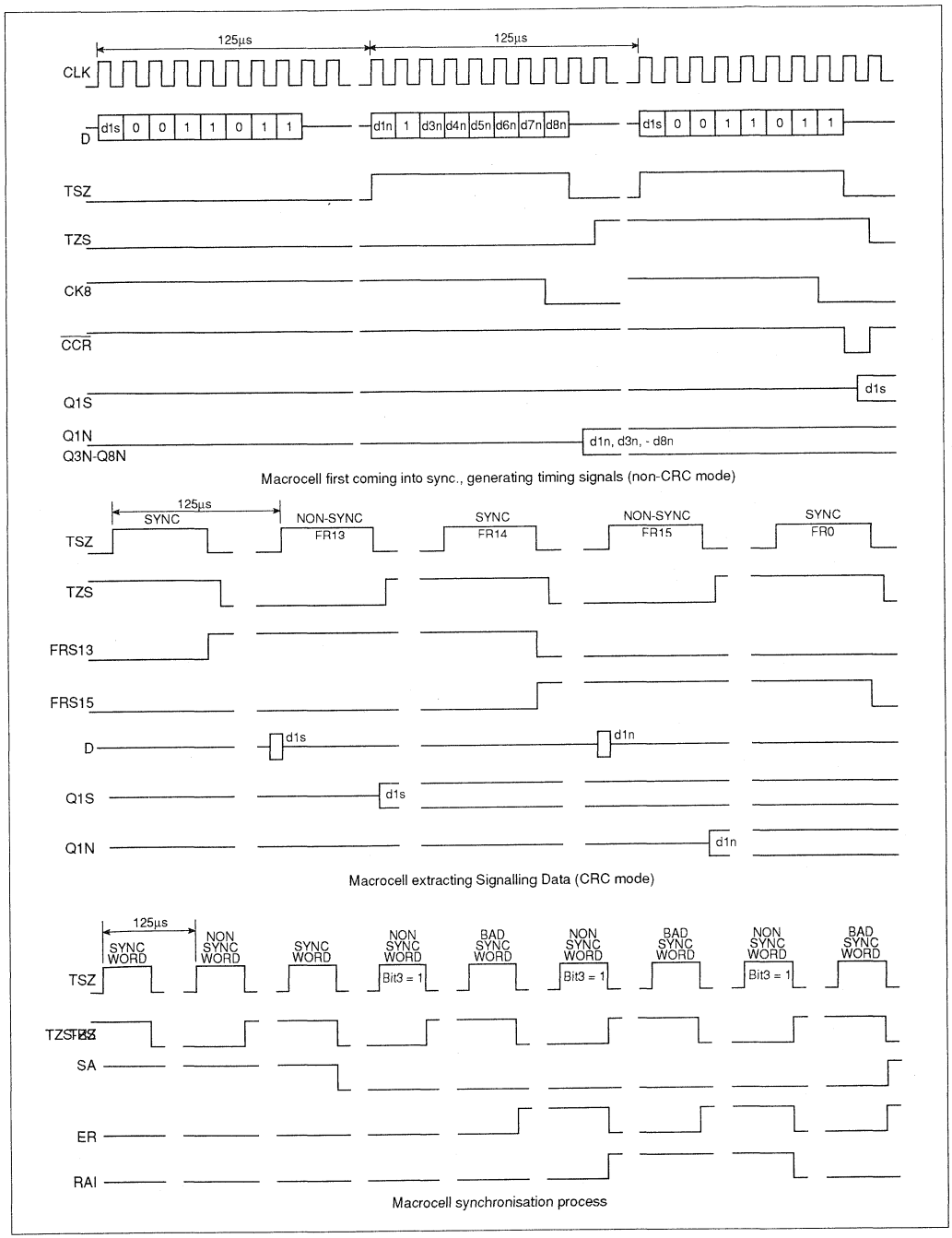


Figure 10: Timeslot zero receiver timing

PIN DESCRIPTIONS

Symbol	Pin No.		Mode name (see note 1)	Pin name and description
	DP48	HP44		
$V_{DD}1$			GLOBAL	Digital supply voltage. 5V (Note 2)
ER	2	2	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Sync Word Error Output (ER). This flag goes high for one frame immediately after detection of a bad timeslot zero sync word, whilst the macrocell is in sync. Three consecutive errors of this type will put the receiver out of sync. The last ER pulse of this sequence will be longer than 256 periods if a valid sync word is detected during the pulse.
MFQ1	3	3	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Synchronisation Alarm Output (SA). This error flag goes high when the macrocell is out of sync and only changes state at the end of a sync frame timeslot zero.
			TX	Timeslot Zero Transmitter (TXTSZ) Macrocell - Timeslot Zero Sync frame marker (TZS). This output is high during timeslot zero of sync frames and changes state at the beginning of timeslot one, bit 2 of every frame.
MFQ2	4	4	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Remote Alarm Indication Output (RAI) This is a persistence checked version of the Q3N output. When RXTSZ is in sync, this output goes high if the current and previous timeslot zero bit 3 of non-sync frames are both high. This output changes state at bit 1, timeslot 1 of non-sync frames. When the macrocell is out of sync this output is forced low in the non-sync frame following the last bad sync frame, and is held low until the macrocell comes back into sync.
			TX	Timeslot Zero Transmitter (TXTSZ) Macrocell - Data Output (Q). The sync word and signalling data word appear here in 8 bit bursts during timeslot zero. Bit 1 appears immediately after the rising edges of CLK and FRS. This output is low during all timeslots except timeslot zero.
DQ8 DQ7 DQ6 DQ5 DQ4 DQ3	5 6 7 8 9 10	5 6 7 8 9 10	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Data Outputs (Q8N-Q3N). These outputs are extracted from bits 8-3 of timeslot zero during non-sync frames respectively. These outputs change at the start of bit 1, timeslot 1 of non-sync frames .
			TX	Timeslot Zero Transmitter (TXTSZ) Macrocell Data Inputs (D8N-D3N). These data inputs are inserted into bits 8-3 of timeslot zero during non-sync frames respectively. This data must be set up prior to the rising edge of FRS.
DQ1	11	11	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Data Output (Q1 N). With CRC = 0, this output latches data from bit I, timeslot zero of non-sync frames. The output changes at the beginning of bit I, timeslot 1 of non-sync frames. With CRC=1, this output latches data from bit 1 of frame 15 of the CRC multiframe.
			TX1	Timeslot Zero Transmitter (TXTSZ) Macrocell - Data Input (D1). The data on this pin is inserted into the International spare bit (bit 1, timeslot zero of both sync and non-sync frames), and must be set up prior to the rising edge of FRS.
			TX2	This pin is unused since the DI input of the Timeslot Zero Transmitter is connected internally to the Q output of the CRC Generator.
Q1S	12	12	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Data Output (Q1S). With CRC = 0, this output latches data from bit 1, timeslot zero of sync frames. The output changes at the beginning of bit 1, timeslot 1 of sync frames. With CRC = 1, this output latches data from bit 1 of frame 13 of the CRC multiframe.
$V_{DD}2$	13	-	GLOBAL	Digital supply voltage. 5V (Note 2)
GND1	14	13	GLOBAL	Digital ground. 0V (Note 2)
LIA	15	14	RX	HDB3 Decoder (HDB3DC) Macrocell - Loss of Input Alarm Output (LIA). This alarm output goes high after 11 consecutive zeros have been detected on the HDB3 inputs. It is reset on detection of a mark (1) on either HDB3 input.

PIN DESCRIPTIONS (continued)

Symbol	Pin No.		Mode name (see note 1)	Pin name and description
	DP48	HP44		
MFQ3	16	15	RX	HDB3 Decoder (HDB3DC) Macrocell - Double Violation Alarm Output (DV). This pin goes high one period after detection of a double violation on either of the HDB3 inputs.
			TX	HDB3 Encoder (HDB3EC) Macrocell - Data Output (a). This output is a single period delayed version of this macrocells D input.
MFQ4	17	16	RX	HDB3 Decoder (HDB3DC) Macrocell - Clock Regeneration Output (CDR). This output is a logical 'OR' function of the two HDB3 inputs and may be used by external clock regeneration circuitry. This signal has a variable mark-to space ratio.
			TX	HDB3 Encoder (HDB3EC) Macrocell - HDB3 Encoded Output 2 (TXD2). This output is always low during the high half cycle of clock and is only high the low half cycle if a mark is to be output.
MFQ5	18	17	RX	HDB3 Decoder (HDB3DC) Macrocell - HDB3 Decoded Output (Q). This output is the HDB3 inputs decoded back to NRZ form.
			TX	HDB3 Encoder (HDB3EC) Macrocell - HDB3 Encoded Output 1 (TXD1). As TXD2 (MFQ4).
FRS13RZ	19	18	RX1	Timeslot Zero Receiver (RXTSZ) Macrocell - Frame 13 Marker Input (FRS13). In CRC mode, this input should be high during bit 8, Frame 13 of the CRC multiframe and low during bit 8 of all other non-sync frames.
			RX2	This pin is unused since the FRS13 input ol the Timeslot Zero Receiver is connected internally to the FRS13 output of the CRC Checker.
MFD1	20	19	RX1	Timeslot Zero Receiver (RXTSZ) Macrocell - Frame 15 Marker input (FRS15). In CRC mode, this input should be high during bit 8, Frame 15 ot the CRC multiframe and low during bit 8 of all other non-sync frames.
			RX2	This pin is unused since the FRS15 input of the Timeslot Zero Receiver is connected internally to the FRS15 output of the CRC Checker.
			TX1	No Connection.
			TX2	PCM Voice Channel Input. In Transmit Demonstration mode this pin is used as the serial data input to the Transmission Multiplexer.
MFD2	21	20	RX1	Timeslot Zero Receiver (RXTSZ) Macrocell - Data Input (D). This pin is used to input the 2.048 Mbit data stream to this macrocell.
			RX2	This pin is unused since the D input of the Timeslot Zero Receiver is connected internally to the Q output of the HDB3 Decoder.
			TX	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Signalling Data Input (D1 N). This pin is used to input the data to be inserted into bit 1 of non sync frames (CRC = 0) or bit 1 of frame 15 of the CRC multiframe (CRC = 1).
MFD3	22	21	RX	HDB3 Decoder (HDB3EC) Macrocell - Data Input 1 (RXD1). This input latches the incoming HDB3 encoded data and is rising edge sensitive. The rising edge of this input should not occur within 50 ns of the rising edge of CLK.
			TX1	HDB3 Encoder (HDB3EC) Macrocell - Data Input (D). This pin is used to input NRZ data for conversion into pseudo ternary HDB3 format.
			TX2	This pin is unused since the D input of the HDB3 Encoder is connected internally to the Q output of the Transmission Multiplexer.
MFD4	23	22	RX	HDB3 Decoder (HDB3DC) Macrocell - Data Input 2 (RXD2). As RXD1 (MFD3)
			TX	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Signalling Data Input (D1S). This pin is used to input the data to be inserted into bit 1 of sync frames (CRC = 0) or bit 1 of frame 13 of CRC multiframe (CRC = 1).
V_{DD3} V_{DD}	24 _	- 23	GLOBAL	Digital supply voltage. 5V (Note 2)

PIN DESCRIPTIONS (continued)

Symbol	Pin No.		Mode name (see note 1)	Pin name and description
	DP48	HP44		
GND2	25		GLOBAL	Digital ground. 0V (Note 2)
DEMO	26	24	GLOBAL	Demonstration pin. A logic high on this pin puts the MV1403 into demonstration mode, RX2 or TX2 with all the transmit or receive macrocells connected together internally. A low on this pin allows access to the macrocells individually (ie. RX1 or TX1 mode).
MODE	27	25	GLOBAL	Transmit/Receive Mode pin. A logic high on this pin places the MV1403 in Receive mode RX1 or RX2. A low places it in Transmit mode TX1 or TX2
CLK	28	26	GLOBAL	2.048MHz Master Clock input.
STM	29	27	GLOBAL	Scan Path Test Mode pin. A logic high on this pin places the MV1403 in scan test mode. For normal operation this pin should be tied low.
P	30	28	GLOBAL	Scan Test Data input. In Scan Path Test Mode, this pin is used as the input to the scan path.
CRC	31	29	GLOBAL	CRC Mode pin. This pin is used as the CRC mode input to the CRCGEN (EN input) or RXTSZ (M input) macrocells. A logic high on this pin will put the MV1403 into Cyclic Redundancy Check mode.
MFD5	32	30	RX1	Cyclic Redundancy Checker (CRCCHK) Macrocell - Data Input (D). This pin is used as the 2.048Mbit serial data input to this macrocell.
			RX2	This pin is unused since the D input ol the CRC Checker is connected internally to the a output of the HDB3 Decoder.
			TX1	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Data Input (D). This pin is the 2.048 Mbit data input to this macrocell.
			TX2	This pin is unused since the D input to the CRC Generator is connected internally to the a output of the Transmission Multiplexer
FRS	33	31	RX1	Frame Sync Input (FRS). This pin is the 8kHz timeslot zero frame marker input to the Timeslot Sixteen Receiver (RXTS16) and Cyclic Redundancy Checker (CRCCHK) macrocells. It is required to be high only during timeslot zero of each frame.
			RX2	This pin is unused since the FRS inputs to the CRC Checker and Timeslot 16 Receiver are connected internally to the TSZ output of the Timeslot Zero Receiver .
			TX	Frame Sync Input (FRS). This pin is the 8kHz timeslot zero frame marker input. It is required to be high only during timeslot zero of each frame.
TZS	34	32	RX1	Cyclic Redundancy Checker (CRCCHK) Macrocell - Timeslot Zero Sync Frame Marker Input (TZS). This 4KHz input is required to be high during timeslot zero of sync frames and change at the beginning of bit 2, timeslot 1 of every frame.
			RX2	This pin is unused since the TZS input of the CRC Checker is connected internally to the TZS output of the Timeslot Zero Receiver.
			TX1 .	Cyclic Redundancy Check Generator (CRCGEN) Macrocell Timeslot Zero Sync Frame Marker Input (TZS). This 4kHz input is required to be high during timeslot zero of sync frames and change at the beginning of bit 2, timeslot 1 of every frame.
MFD6	35	33	RX1	Timeslot Sixteen Receiver (RXTS16) Macrocell - 2.048Mbit Serial Data Input (D). The 8 bits of signalling data in timeslot t6 are extracted from this input during timeslot 16.
			RX2	This pin is unused since the D input of the Timeslot 16 Receiver is connected intermally to the (; output of the HDB3 Decoder.
			TX	Timeslot Sixteen Transmitter (TXTS16) Macrocell - 64kbit Signalling Data Input (D). The continuous stream of data to be output as 8 bit bursts during timeslot 16 is input on this pin.
GND3	36		GLOBAL	Digital ground,OV. (Note 2)

PIN DESCRIPTIONS (continued)

Symbol	Pin No.		Mode name (see note 1)	Pin name and description
	DP48	HP44		
RST	37	34	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Reset Input (RST). A logic high on this pin will reset the state machine of this macrocell, forcing the macrocell out of frame alignment. Due to the 100kΩ pull-up resistors on all the inputs, this pin should be tied low when not in use.
MFQ6	38	35	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Sub-multiframe 2 Error Alarm Output (ER2). A logic high on this output indicates the detection of a CRC error in sub-multiframe 2.
			TX	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Data Output (Q). This pin is used to output the data to be inserted into bit 1, timeslot 0.
MFQ7	39	36	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Sub-multiframe 1 Error Alarm Output (ER1). A logic high on this output indicates the detection of a CRC error in sub-multiframe 1.
			TX	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Scan Test Data Output (STQ). In scan test mode, this pin is the scan path output of this macrocell.
MFQ8	40	37	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Multiframe Sync Alarm Output (MSA). A logic high on this output denotes that the macrocell is out of CRC multiframe alignment.
			TX	Timeslot Sixteen Transminer (TXTS16) Macrocell - Timeslot 16 Marker Output (TS16). This output is high only during timeslot 16.
FRS15	41	38	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Frame 15 Marker Output (FRS15). When the macrocell is in CRC multiframe alignment, this output is high during frame 15 and low during all other non-sync frames.
FRS13	42	39	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Frame 13 Marker Output (FRS13). When the macrocell is in CRC multiframe alignment, this output is high during frame 13 and low during all other non-sync frames.
M FQ9	43	40	RX	Timeslot Sixteen Receiver (RXTS16) Macrocell - Signalling Data Output (Q). This pin is used to output the 8 bits of signalling data extracted from timeslot 16 as a continuous 64kbit data stream.
			TX	Timeslot Sixteen Transmitter (TXTS16) Macrocell - Signalling Data Output (Q). The 8 bit data bursts produced by this macrocell are output at 2.048MHz on this pin during timeslot 16. This output is low at all other times.
TSZRZ	44	41	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Timeslot Zero Marker Output (TSZ). This output goes high for the 8 periods of timeslot zero and is low at all other times.
TZSRZ	45	42	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Timeslot Zero Sync Frame Marker Output (TZS). This output is high during timeslot zero of sync frames and changes state at the beginning of bit 2, timeslot 1 of every frame.
CK8	46	43	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - 8kHz Clock Output (CK8). This output goes low at the end of bit 7, timeslot zero and high at the end of bit 7, timeslot 16.
$\overline{CCR}$	47	44	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Channel Reset Output ($\overline{CCR}$). This output pulses low for a single period during bit 1, timeslot 1 of sync frames.
GND4 GND2	48 1		GLOBAL	Digital ground. 0V (Note 2).

NOTES
1. TX refers to TX1 and TX2 modes. RX reters to RX1 and RX2 modes. GLOBAL refers to all modes.
2. All the V_{DD} and GND pins of the 48-pin device, and two GND pins of the 44-pin device are connected together internally and as such there is no need to connect up all these supplies. However, it is recommended that all supply pins are connected to facilitate supply decoupling.
3. Since the device is intended as a demonstrator allowing access to the individual macrocells, 100kΩ pull-up resistors have been included on all the input pins to prevent any unconnected inputs from floating.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)
Supply Voltage V_{DD} = 5V ± 0 .V, Ambient Temperature T_{amb} = 0 to 70°C

STATIC CHARACTERISTICS

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Low level input voltage	V_{IL}			0.8	V	
High level input voltage	V_{IH}	2.0		V_{DD}	V	
Low level output voltage	V_{OL}	0		0.4	V	I_{SINK} = 10mA
High level output voltage	V_{OH}	2.4		V_{DD}	V	I_{SOURCE} = 5mA
Input leakage current	I_{IL}	-20		-200	µA	$V_{IN} = V_{SS}$
		-10		+10	µA	$V_{IN} = V_{DD}$
Supply current	I_{CC}		1.5	3.0	mA	All outputs unloaded
Input capacitance	C_{IN}		5		pF	
Output capacitance	C_{OUT}		5		pF	

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Clock						
Clock frequency	f_{CLK}		2.048		MHz	
Clock rise time	t_{CR}			20	ns	See Fig. 12
Clock high time	t_{CH}	150			ns	See Fig. 12
Clock fall time	t_{CF}			20	ns	See Fig. 12
Clock low time	t_{CL}	150			ns	See Fig. 12
Outputs						
Output propagation delay	t_{OPD}			50	ns	See Fig. 17, note 1
CDR propagation delay	t_{CDRPD}			50	ns	See Fig. 18
Frame synchronisation & related inputs						
FRS rising hold time	t_{FRH}	50			ns	See Fig. 13
FRS rising setup time	t_{FRs}	100			ns	See Fig. 13
FRS falling hold time	t_{FFH}	50			ns	See Fig. 13
FRS falling setup time	t_{FFS}	100			ns	See Fig. 13
TZS setup time	t_{SFS}	50			ns	See Fig. 13
TZS hold time	t_{SFH}	50			ns	See Fig. 13
User data setup time	t_{UDS}	50			ns	See Fig. 13
International data bits setup time	I_{IDS}	100			ns	See Fig. 13
Timeslot Zero data hold time	t_{TZDH}	100			ns	See Fig. 13
Data inputs						
Data setup time	t_{DS}	50			ns	See Fig. 14, note 2
Data hold time	t_{DH}	50			ns	See Fig. 14, note 2
Timeslot 16 transmitter data setup time	t_{T16DS}	50			ns	See Fig. 15, note 3
Timeslot 16 transmitter data hold time	t_{T16DH}	50			ns	See Fig. 15, note 3
HDB3 input data setup time	t_{RXDS}	50			ns	See Fig. 16
HDB3 input data pulse width	t_{RXDW}	50		488	ns	See Fig. 16

NOTES
1. The output propagation delay, t_{OPD}, is valid for all outputs except CDR (from the HDB3DC macrocell) and is specified with FRS rising betore CLK. All output delays are measured with a 50pF load.
2. The data setup and hold parameters, t_{DS} and t_{DH}, apply to the following macrocell inputs: D (CRCGEN), D (HDB3EC) PCM DATA (TMUX), D (RXTSZ), FRS13,15 (RXTSZ), RST (RXTSZ), D (RXTS16), D (CRCCHK), P (GLOBAL)
3. Timeslot 16 transmitter data setup and hold times apply to the rising edge of clock cycles 24, 56, 88 etc (see Fig 4)

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings are limiting values above which opertaing life may be shortened or specified parameters may be degraded.

Positive supply voltage, V_{DD}	- 0.5 to + 7V
Inputs	V_{DD} + 0.3V to GND - 0.3V
Outputs	V_{DD} + 0.3V to GND - 0.3V

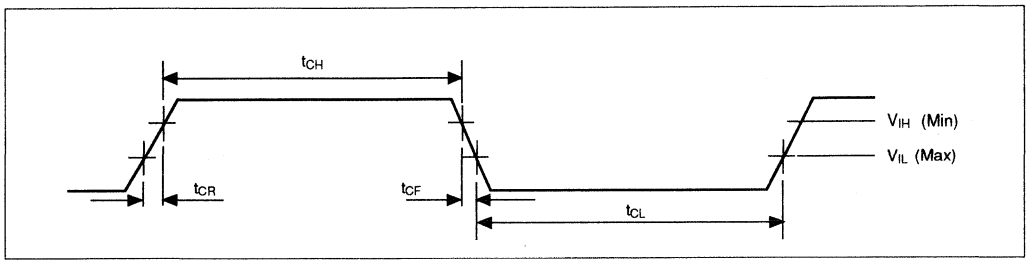


Figure 12: Timing - clock inputs

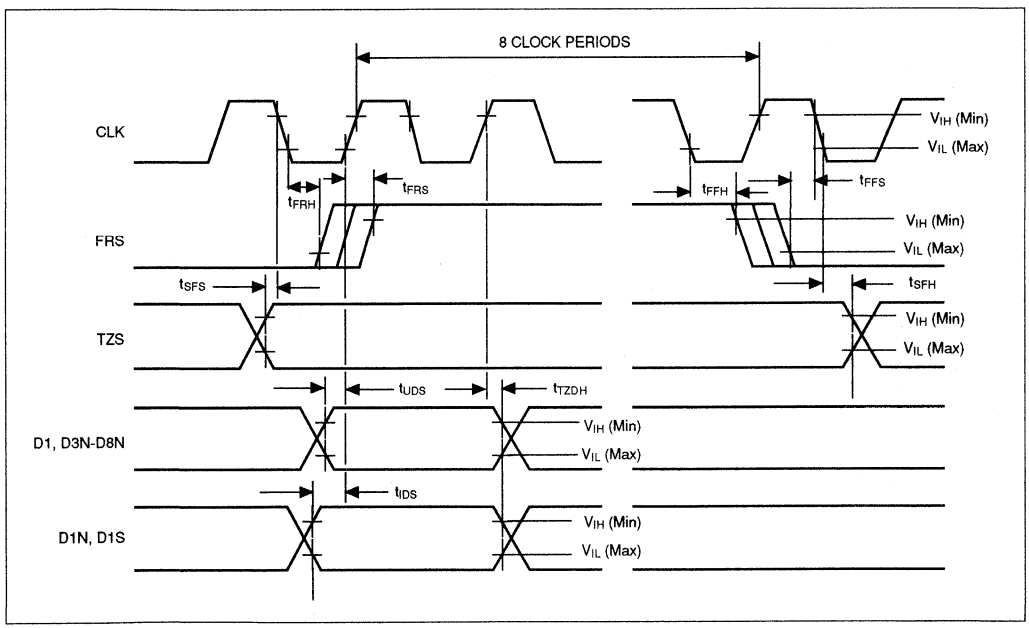


Figure 13: Timing - FRS and related parameters

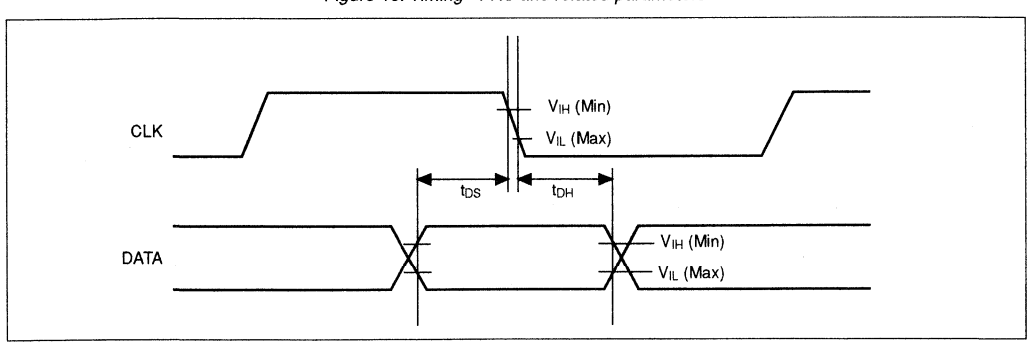


Figure 14: Timing - data inputs

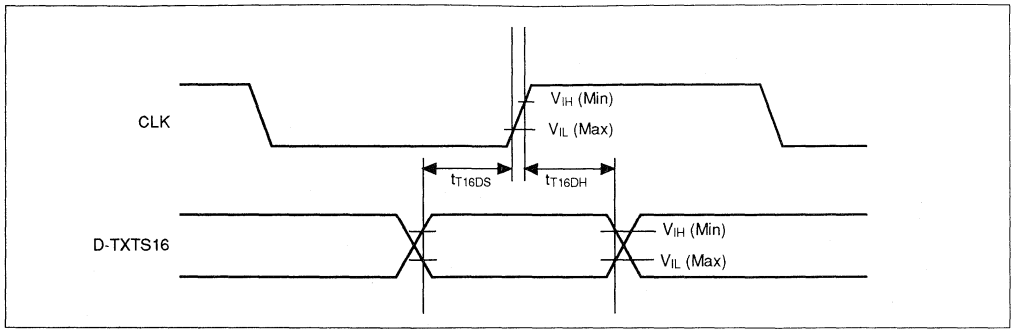


Figure 15: Timing - Timeslot 16 transmitter data input

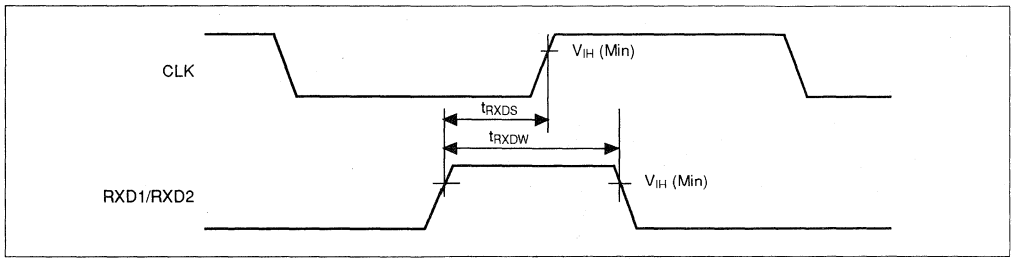


Figure 16: Timing - RXD inputs

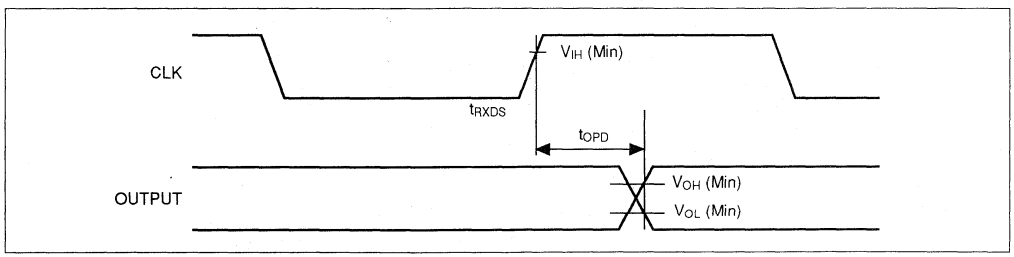


Figure 17: Timing - output propagation delay

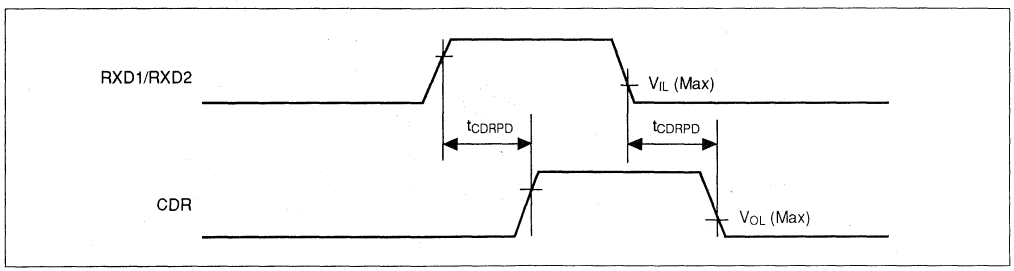


Figure 18: Timing - CDR propagation delay

PCBAN93

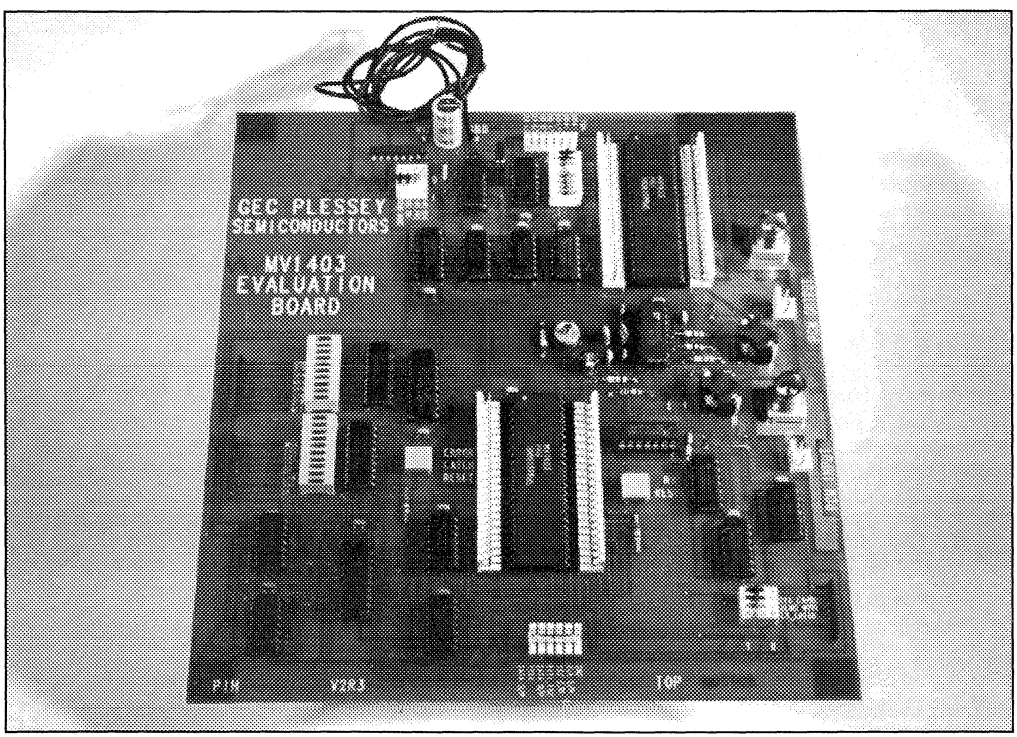
MV1403 PCM DEMONSTRATOR EVALUATION BOARD

Now available from GPS is an evaluation board tor the MV1403 PCM Demonstrator chip. The board contains two MV1403 devices. one used for transmit and the second used for receive PCM functions. In addition, a line interface circuit is included to provide a complete demonstration of all the available Telecom PCM Macrocells within the MV1403.

For more details of the evaluation board, reference should be made to Application Note AN93. The MV1403 Data Sheet contains descriptions of the individual macrocells, whilst detailed design data is available in the CLA60000 Design Manual.

FEATURES

- Contains Two MV1403 PCM Demonstrator Devices, One For Transmit and One For Receive Directions.
- Transmit Mode Provides TS0 Transmit, TS16 Transmit, HDB3 Encode and CRC Generator Functions.
- Receive Mode Provides TS0 Receive, TS16 Receive, HDB3 Decode and CRC Checking Functions.
- 75Ω Coax or 120Ω Twisted Pair Line Driver and Receiver Circuitry with Clock Recovery Contained On Board.
- Single and 8 Periods of Clock Sync Signals Available for Synchronisation of External COMBO/SLAC Devices.
- Internal or External Transmit Clock and Frame Sync Options.
- Generates and Monitors Spare Time Slot Zero Data Bits.
- Displays Status of all Receive Error, Violation and Sync Alarm Outputs.
- Application Note AN93 fully Describes the Operation and Uses of the Evaluation Board.



The PCBAN93 evaluation board.

MA808

FRAME ALIGNER WITH OPTIONAL TIME SLOT ZERO RECEIVER

The MA808 Frame Aligner chip has been primarily designed for use in equipment operating at the CCITT standard of 2048 kbit/s tor 30 channel PCM data signals.

The basic function of the device is to accept a 2048 kbit/s data signal, whose frame structure conforms to CCITT recommendation G732 and frame synchronously align it to a local exchange/system clock.

The frame aligner operation is such that once a synchronisation sequence, as defined in CCITT recommendation G732, is received from a distant source synchronisation is established. Consequently the data stream is delayed such as to align it to the timing required at the local source. Once three successive sync. words are received containing errors, synchronisation is lost. The chip will remain out of sync. until the synchronising sequence is received.

The device can also, when configured in the 'enhanced mode' perform the additional function of time slot zero recovery.

A number of facilities are also provided to simplify the testing of the device and associated system.

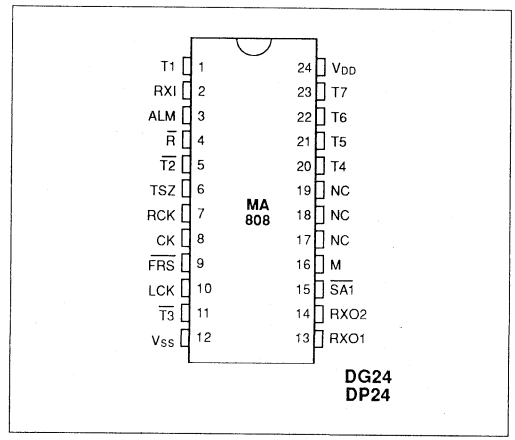


Figure 1: Basic Mode pin connections - top view. M tied to V_{SS}

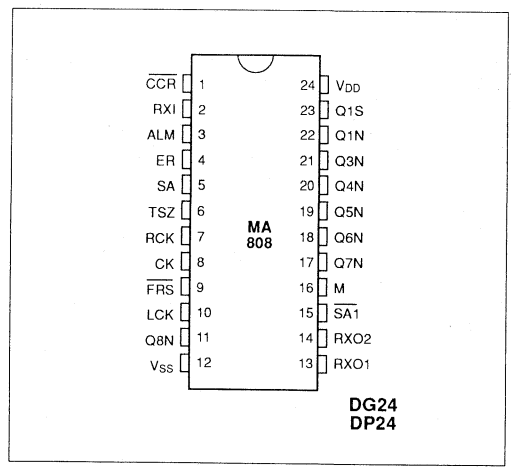


Figure 2: Enhanced Mode pin connections - top view. M tied to V_{DD}

FEATURES

- Fabricated in Low Power CMOS
- Optional Time Slot Zero Receiver
- Detection of Frame Alignment Signals for 30 Channel PCM Highways Operating at 2048 kbit/s in Accordance with CCITT Recommendations G732
- Delay Compensation and Clock Alignment between the Transmission Line system and the Exchange
- Compensation of Phase Jitter, Meeting the Requirements of CCITT
- Detection and Indication of Loss of Frame Alignment
- Provision of a Signal for Generation of AIS
- Slip Compensation
- Chip Functional Test Facilities
- TTL Compatible
- Operating Power Consumption 75mW max.
- Single + 5V Supply
- High Latch-up Immunity
- 256 kHz Clock Output

APPLICATIONS

- Digital Multiplex Equipment
- Interfaces between PCM Line and Switching Systems
- Concentrators

OPERATION IN BASIC MODE (M =V_{SS})

FRAME ALIGNMENT

The remote non-return-to-zero (NRZ) binary PCM data stream (RXI) required to be aligned must be applied to the frame aligner along with a synchronous clock (RCK). A time slot zero impulse (TSZ) as shown in Fig. 5 is also required to define the start ot the frame of input data.

A local clock (LCK) provides the timing from which the output data is clocked. Frame reset pulse ($\overline{FRS}$) is the data output timing pulse. The MA808 aligns the 16th bit of the incoming data to this pulse, as shown in Fig. 5, and the two NRZ binary outputs RXO1 and RXO2 are produced. RXO1 is purely a retimed version of the input data. RXO2 has the third bit of all time slot zero locations of the input data inverted, thereby deliberately corrupting the frame sync. and the frame sync. verification words. Once synchronisation has been established $\overline{FRS}$ may be removed. If synchronisation is lost, $\overline{FRS}$ must be reapplied in order to permit resynchronisation to be established.

SLIP COMPENSATION

Small differences in frequency between the local and remote clocks (LCK and RCK) are compensated for by the repetition of the previous frame, ('slipping in') or the omission of one complete frame of data ('slipping out').

INPUT ALARMS

Two input alarms ($\overline{SA1}$ and ALM) are provided which will set data output(s) to an 'all ones' condition. ALM sets only RXO2 and $\overline{SA1}$ sets both RXO1 and RXO2 high (Fig. 6).

TEST FEATURES

The operation of the internal memory of the MA808 is continuously monitored by performing a check sum comparison of the input and output data signals RXI and RXO1. When an error is detected, the time slot zero words of RXO1 and RXO2 are set 'high'.

When a 'low' is applied to test input T3, the outputs RXO1, RXO2 and CK are forced into a high impedance condition, thereby allowing associated circuitry to be tested independently of the MA808. Note that this facility is only available in the basic mode of operation.

OPERATION IN ENHANCED MODE (M=V_{DD})

When configured in the enhanced mode the chip performs time slot zero (TS0) recovery in addition to the frame alignment function. TS0 recovery may also be performed independently.

FRAME ALIGNMENT

The operation of frame alignment is essentially the same as the basic mode, except that the TSZ pulse is an output rather than an input, in accordance with the operation of the TS0 receiver, as shown in Fig. 7. The operation of the input alarms to set the output data 'high' is the same as described in the basic mode (Fig. 6).

TIME SLOT ZERO RECEIVER

Two output signals (TSZ and $\overline{CCR}$) are provided so that the time slot zero receiver may be used independently of the frame alignment function. $\overline{CCR}$ is a channel reset pulse (as shown in Fig. 7) which goes 'low' for one RCK period following a sync. word (every alternate frame) when the device is in sync. When the device is out of sync. the reset pulse occurs after each time slot zero.

The TS0 receiver accesses information contained within time slot zeros and processes it to offer the facilities of synchronisation alarm (SA), error output (ER) and time slot zero spare bits (Q1S, Q1N, Q3N-Q8N).

SYNCHRONISATION ALARM (SA)

SA indicates loss of sync. as shown in Fig. 8. With the frame aligner operating in sync., SA will be 'low'. Following the receipt of 3 successive sync. words containing errors, SA will become active. SA will remain 'high' until the correct synchronising sequence as defined in CCITT recommendations G732 has been received.

ERROR OUTPUT (ER)

A logic signal, ER, indicating errors in sync. words, is provided as shown in Fig. 8, from which an AIS alarm may be generated. ER is activated at the beginning of the second bit of time slot 1 two frames after the receipt of a sync. word containing errors. If successive sync. words contain errors, the signal will remain active.

If synchronisation is lost, ER will remain active but will go 'low' for one period of the remote clock during the second bit of time slot 1, two frames after the receipt of the last valid sync. word, as long as synchronisation is not regained at this time.

If synchronisation is regained, ER will go 'low' for the two frames following the sync. word which caused synchronisation to be regained. The signal indicating an error in the sync. word two frames prior to synchronisation being regained will be delayed by one further sync. frame period. Consequently, it may be concluded that all errors in sync. words are accounted for in this signal, hence error monitoring in accordance with CCITT recommendation G732.3.1.6.1 may be performed.

TIME SLOT ZERO SPARE BITS

The spare bits contained in both time slot zero words are converted from serial to parallel format (Q1N, Q3N-Q8N inc. and Q1 S) are shown in Fig. 9.

PIN DESCRIPTIONS - BASIC MODE

Pin	Def.	Function	Description
1	T1	Test input	Active high. To be tied to logic low during normal operation.
2	RXI	Data input	Recovered distant data input.
3	ALM	Alarm input	A logic high on this input sets RXO2 to an all 1 s condition.
4	R	Reset input	'Low' resets the device tied 'high' normally.
5	$\overline{T2}$	Test input	Active low. To be tied to logic high during normal operation.
6	TSZ	TSO input	Remote TS0 timing signal.
7	RCK	Clock input	Recovered distant clock in sync. with RXI.
8	CK	256kHz output	256kHz square wave clock output synchronous with LCK.
9	$\overline{FRS}$	Timing input	Data output timing pulse coincident with 16th bit of the local clock.
10	LCK	Clock input	Local clock input.
11	$\overline{T3}$	Test input	Active low. To be tied to logic high during normal operation.
12	V_{SS}	Negative supply	Nominally 0V.
13	RXO1	Data output	Retimed data output to LCK.
14	RXO2	Data output	As RXO1 except that bit 3 of each TS0 word is inverted.
15	SA1	Set to all 1s input	A logic low sets RXO1 and RXO2 to an all 1s condition.
16	M	Mode input	Connected to Vss for basic mode operation.
17	NC	No connection	To be left O/C during normal operation.
18	NC	No connection	To be left O/C during normal operation.
19	NC	No connection	To be left O/C during normal operation.
20	T4	Test input	Active when clocked by LCK (pin 10). To be tied to logic low during normal operation.
21	T5	Test input	Active when clocked by RCK (pin 7). To be tied to logic low during normal operation.
22	T6	Test output	To be left O/C during normal operation.
23	T7	Test output	To be left O/C during normal operation.
24	V_{DD}	Positive supply	Nominally + 5V.

PIN DESCRIPTIONS - ENHANCED MODE

Pin	Def.	Function	Description
1	$\overline{CCR}$	Channel reset	An output used to reset other devices within the system.
2	RXI	Data input	Recovered distant data input.
3	ALM	Alarm input	A logic high on this input sets RXO2 to an all 1 s condition.
4	ER	Error output	A TS0 word error is signalled when ER goes to logic high.
5	SA	Sync. alarm O/P	Loss of sync. is signalled when SA goes to logic high.
6	TSZ	TSO output	Remote TS0 output signal, (internally connected to the on-chip frame aligner).
7	RCK	Clock input	Recovered distant clock in sync. with RXI.
8	CK	256kHz output	256kHz square wave clock output synchronous with LCK.
9	$\overline{FRS}$	Timing input	Data output timing pulse coincident with 16th bit of the local clock.
10	LCK	Clock input	Local clock input.
11	Q8N	Output signal	Signal corresponding to bit 8 of the TS0 sync. verification word.
12	V_{SS}	Negative supply	Nominally 0V
13	RXO1	Data output	Retimed data output to LCK
14	RXO2	Data output	As RXO1 except that bit 3 of each TS0 word is inverted.
15	SA1	Set to all 1s input	A logic low sets RXO1 and RXO2 to an all 1s condition.
16	M	Mode input	Connected to V_{DD} for enhanced mode operation.
17	Q7N	Output signal	Signal corresponding to bit 7 of the TS0 sync. verification word.
18	Q6N	Output signal	Signal corresponding to bit 6 of the TS0 sync. verification word.
19	Q5N	Output signal	Signal corresponding to bit 5 of the TS0 sync. verification word.
20	Q4N	Output signal	Signal corresponding to bit 4 of the TS0 sync. verification word.
21	Q3N	Output signal	Signal corresponding to bit 3 of the TS0 sync. verification word.
22	Q1 N	Output signal	Signal corresponding to bit 1 of the TS0 sync. verification word
23	Q1 S	Output signal	Signal corresponding to bit 1 of the TS0 sync. word.
24	V_{DD}	Positive supply	Nominally +5V.

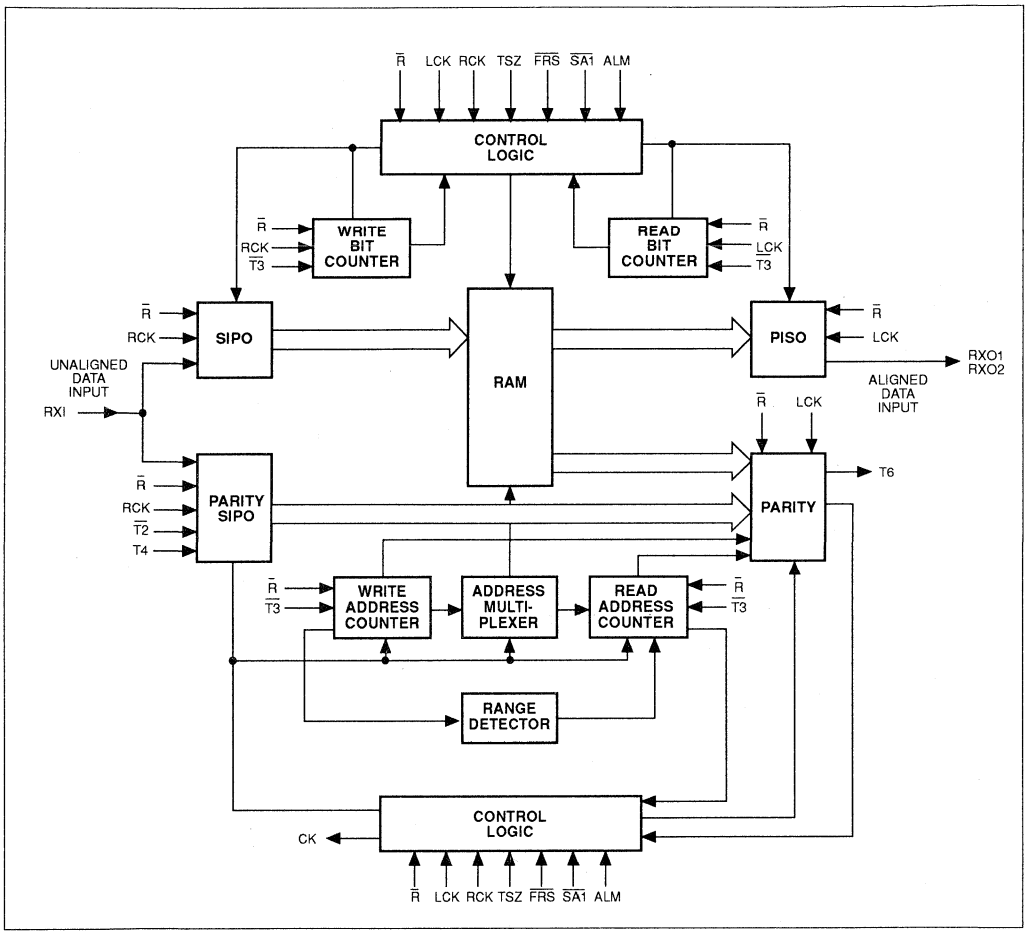


Figure 3: Frame aligner block diagram

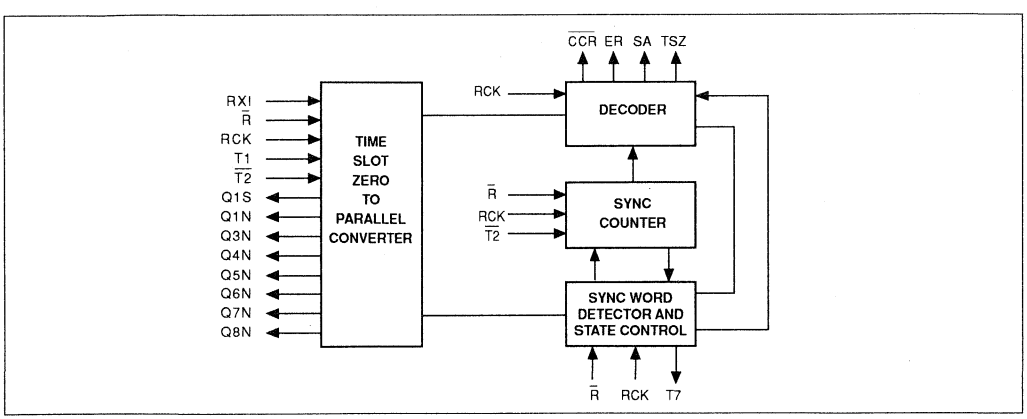


Figure 4: TSO receiver block diagram

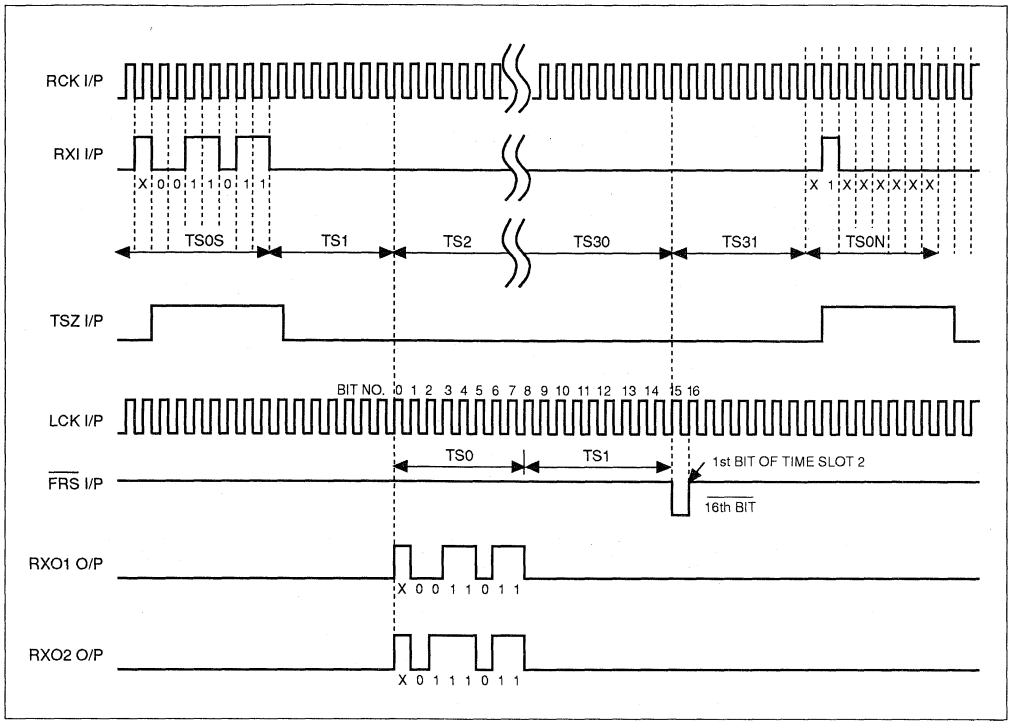


Figure 5: Timing diagram - basic mode: general operation of frame alignment

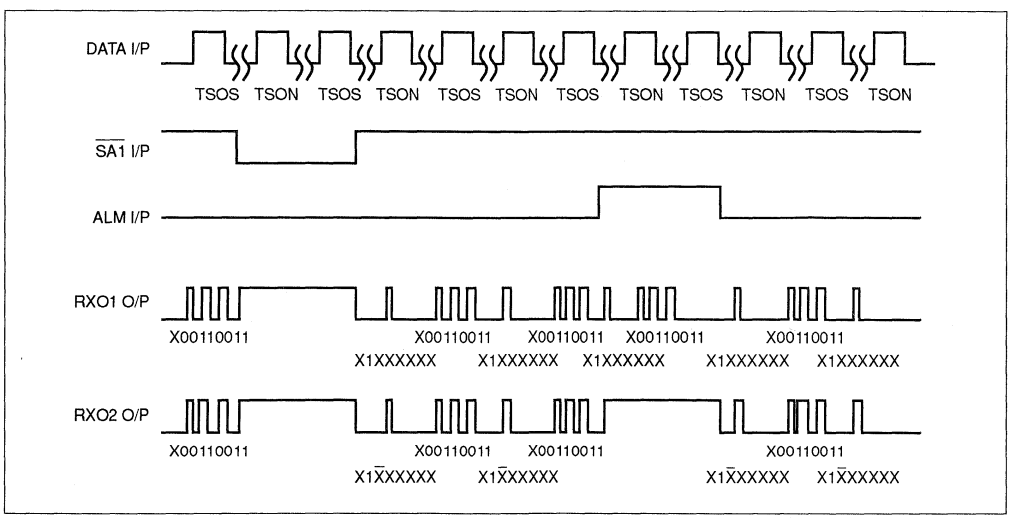


Figure 6: Timing diagram: protocol timings of the alarm signals

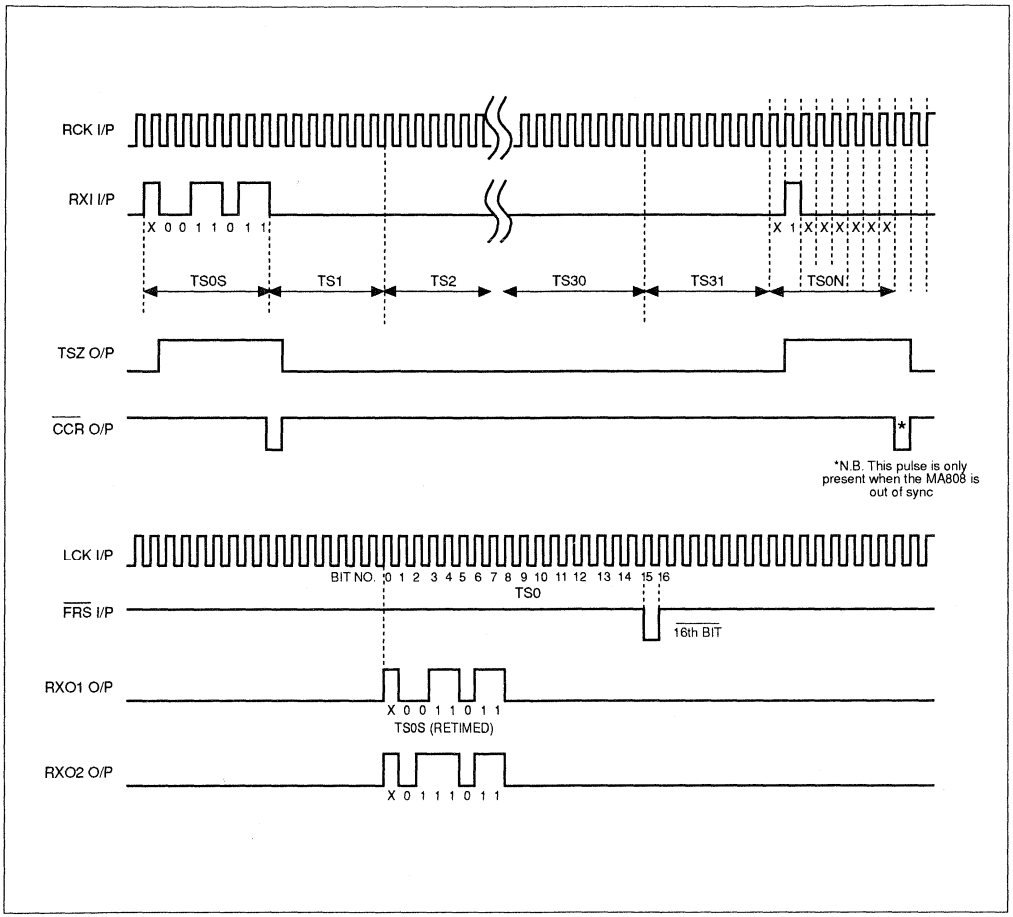


Figure 7: Timing diagram - enhanced mode: general operation of frame aligner

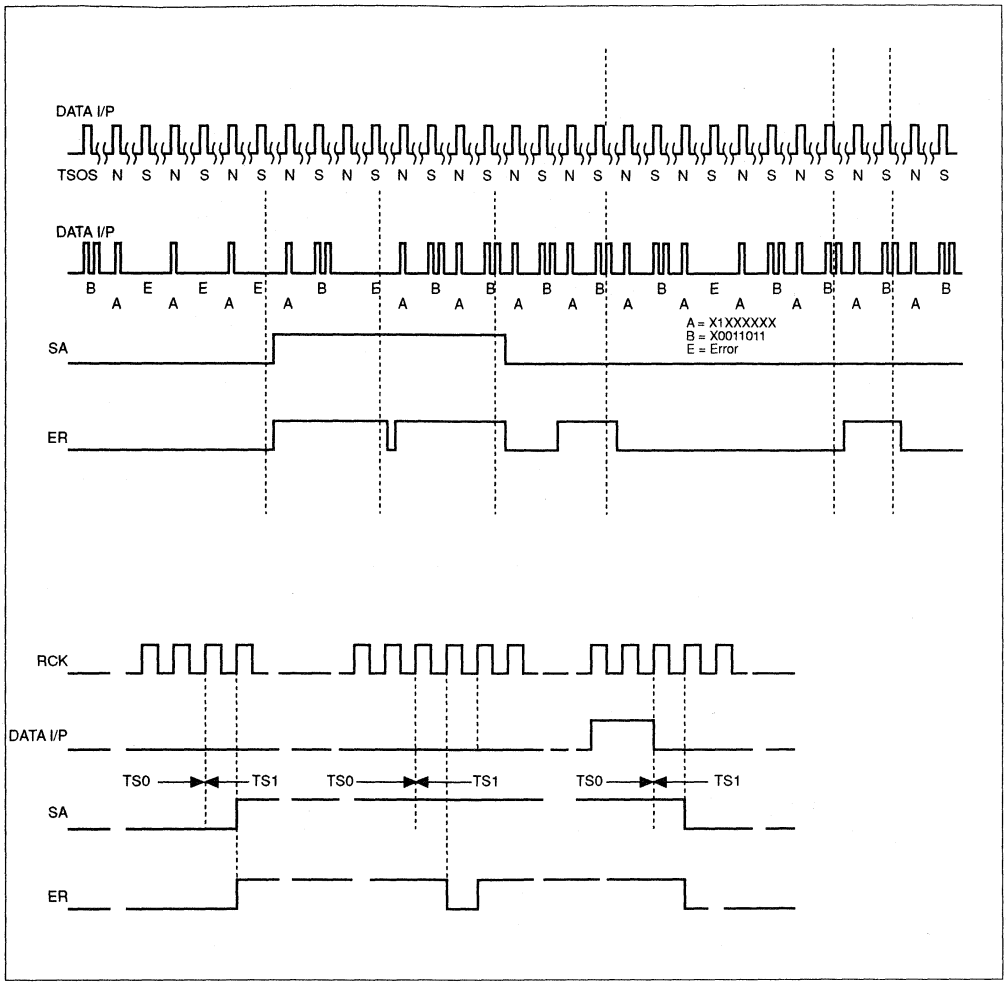


Figure 8: Timing diagram - enhanced mode: protocol timings of TSO receiver alarms

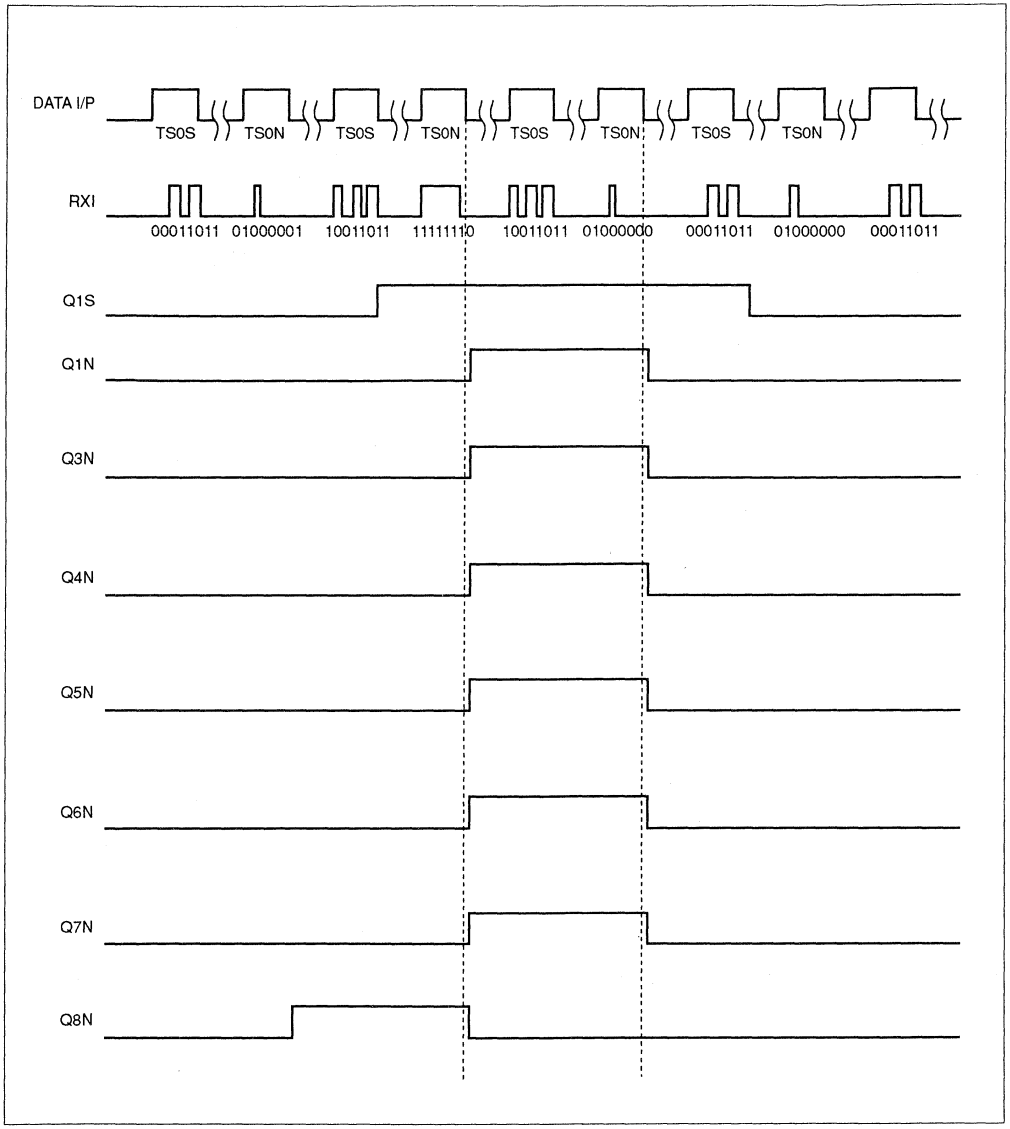


Figure 9: Timing diagram - enhanced mode: protocol timings of the signal lines

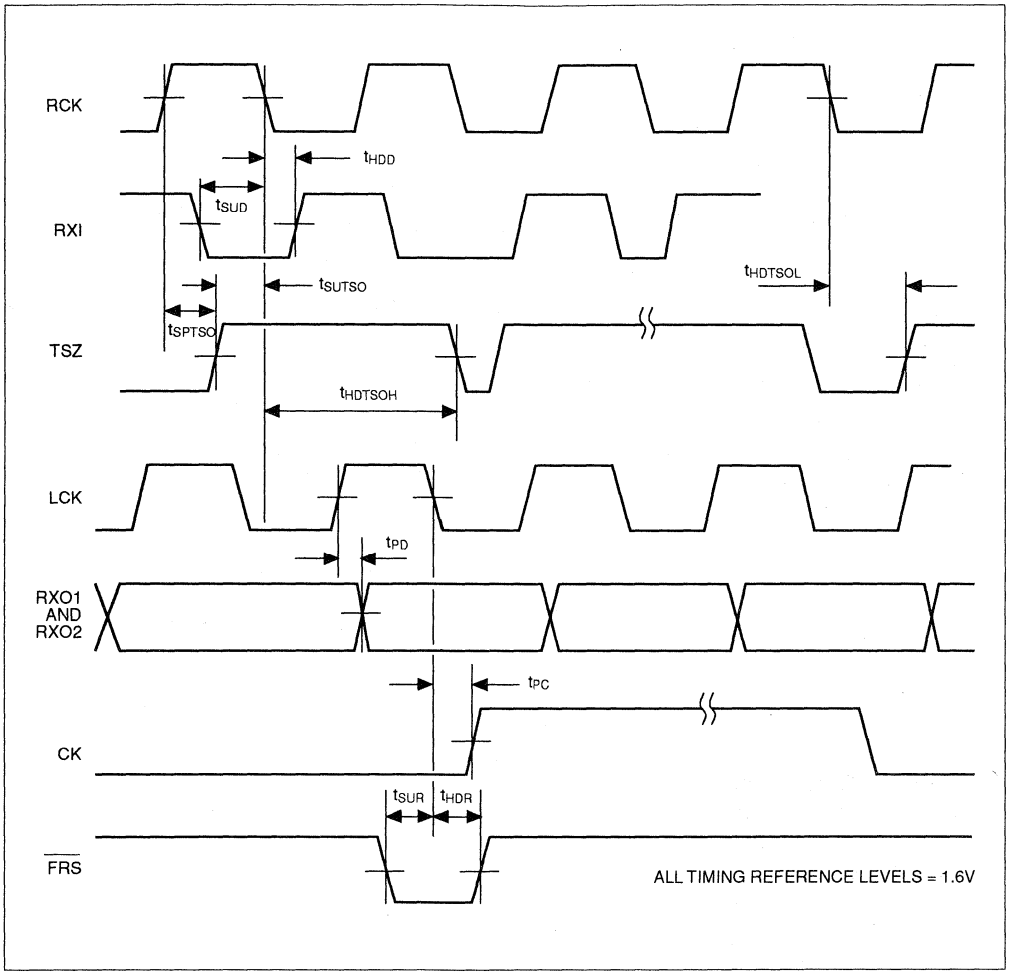


Figure 10: Timing diagram - basic and enhanced mode timing waveforms

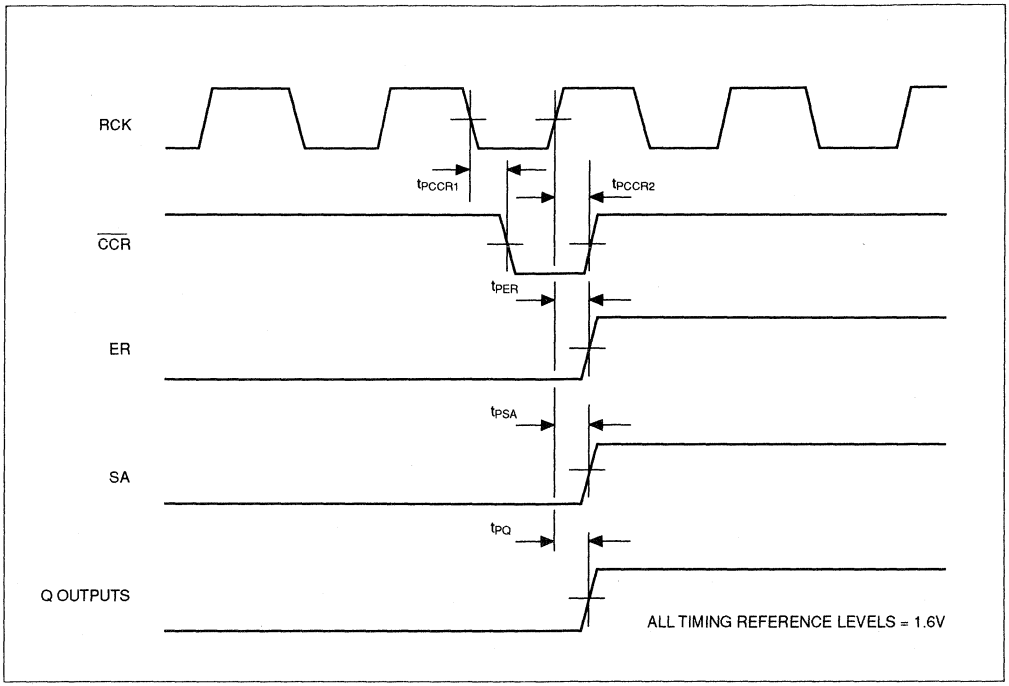


Figure 11: Timing diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)

T_{AMB} = + 25 ° C

DC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Low level input voltage	V_{IL}			0.8	V	V_{DD} = 4.75V
High level input voltage	V_{IH}	2.4			V	V_{DD} = 5.25V
Low level input current	I_{IL}			10	µA	$V_{IN} = V_{SS}$. V_{DD} = 5.25V
High level input current	I_{IH}			10	µA	$V_{IN} = V_{DD}$ = 5.25V
Low level output voltage	V_{OL}			0.5	V	I_{OL} = 2mA, V_{DD} = 4.75V
High level output voltage	V_{OH}	2.8				I_{OH} = 0 2mA V_{DD} = 4.75V
Output leakage current	I_{OL}			±10	µA	$V_{SS} < V_{OUT} < V_{DD}$, V_{DD} = 5.25V
Dynamic supply current	I_{DDD}			15	mA	
Static supply current	I_{DDS}			1	mA	

AC TIMING CHARACTERISTICS (REFER TO FIGS. 10 AND 11)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Set up time RXI to RCK (H→L)	t_{SUD}	25			ns	
Set up time TSZ to RCK (H→L)	t_{SUTSO}	20			ns	
Set up time $\overline{FRS}$ to LCK (H→L)	t_{SUR}	150			ns	
Data hold time wrt RCK (H→L)	t_{HDD}	100			ns	
TSZ (L) hold time wrt RCK (H→L)	t_{HDTSOL}	50			ns	
TSZ(H) hold time wrt RCK (H→L)	t_{HDTSOH}	100			ns	
$\overline{FRS}$ hold time wrt LCK (H→L)	t_{HDR}	150			ns	
Nominal frequency	f		2.048		MHz	
Propagation delay, LCK to RXO1 and RXO2	t_{PD}	30		150	ns	
Propagation delay, LCK (H→L) to CK	t_{PC}	0		175	ns	
Propagation delay, RCK (H→L) to $\overline{CCR}$ (H→L)	t_{PCCR1}	0		150	ns	Outputs loaded
Propagation delay, RCK (L→H) to $\overline{CCR}$ (L→H)	t_{PCCR2}	0		200	ns	to10pF,
Propagation delay, RCK (L→H) to TSZ	t_{PTSO}	20		200	ns	f_{CLOCK}=2.048MHz
Propagation delay, RCK (L→H) to ER	t_{PER}	20		200	ns	
Propagation delay, RCK (L→H) to SA	t_{PSA}	20		200	ns	
Propagation delay, RCK (L→H) to Q8N-Q3N, Q1N and Q1S	t_{PQ}	20		200	ns	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}-V_{SS}	- 0.3 to + 7.0V
Voltage on any pin (V_{IN}) (See note 1)	V_{SS} - 0.3V to V_{DD} + 0.3V
Current through any pin (See note 1)	± 20mA
Storage temperature	-55°C to + 125°C
Operating temperature range	-10°C to+55°C

NOTES

1. Guaranteed no latch-up conditions.
2. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

MA8112

DIGITAL SWITCH MODULE (DSM)

The MA8112 is a CMOS device providing digital switching for up to 256 8-bit channels as used in PCM or data systems. 8-bit words are received and transmitted at 2.048 Mb/s on each of eight input and eight output lines respectively either in a parallel format whh 256 consecutive channels or in serial format with 32 channels multiplexed on to each of the eight lines.

The device operates unidirectionally and allows 8-bit words from any incoming channel to be switched to any outgoing channel, under the control of an on-chip connection memory, which may be updated or interrogated via an external control interface. The control interface and addressing facilities are designed to allow easy expansion to provide greater switching capacity.

Applications include PCM switching systems in which up to 32 x 64Kb/s speech/data channels are time division multiplexed onto a single line in accordance with CCITT Recommendation G732 2.048Mb/s format.

Alternatively, the device can be used as a high speed data switch at data rates up to 2.048 Mb/s and can be used to convert 8-bit channels from serial to parallel format or vice versa.

The MA8112 is pin-compatible with the MS2002.

FEATURES

- Single 5V Supply
- Low Power CMOS Design
- Inputs and Outputs TTL Compatible
- Compatible with CCITT 32-Channel 2.048 Mb/s Format (Rec. G732)
- 256 Input/256 Output Channels
- Inputs and Outputs can be Serial or Parallel
- Variable Input/Output Frame Delay
- Designed to allow Easy Expansion into Larger Switches Matrices

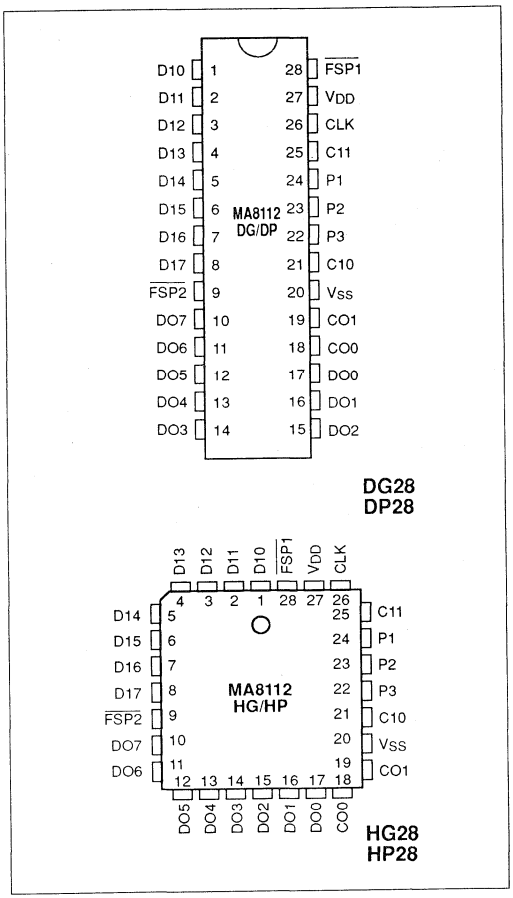


Figure 1: Pin connections - top view

FUNCTIONAL DESCRIPTION

The MA8112 Digital Switch Module is designed to provide switching for 256 x 8-bit PCM encoded speech or data channels operating at rates upto 2.048 Mb/s. The input and output data is handled in frames containing 256 8-bit channels in either serial or parallel format and repeating at a rate of up to 8 kHz. The format of these frames is shown in Fig.3. When operating at 2.048 Mb/s in serial input/output mode, 32 channels each operating at a rate of 64 kb/s are multiplexed on to each line according to CCITT specifications for PCM transmission (Recommmendatbn G732).

The input frame to output frame delay is variable (up to one frame perbd) with the input channel data stored on chip until being sent to the appropriate output channel. The switching of any input channel is independent of any other channel and once set up, the connection between an input channel and an output channel is maintained until a new connection is specified via the control interface.

Switching is achieved as follows:

The MA8112 contains two read/write memories- the SPEECH (i.e. PCM) memory and the CONNECTION memory.

In the speech memory, there is one 8-bit location dedicated to each of the 256 8-bit PCM (speech) input channels. In each frame of incoming data, each 8-bit PCM word will be written to a location in the speech memory according to its input channel. This operation is repeated in successive frames.

In the connection memory, there is one location dedicated to each of the 256 PCM output channels. Each of these locations contains an 8-bitt word which is used to address one of the 256 locations in the speech memory (and hence one of the 256 input channels). The PCM word contained in this location is then sent to the output channel concerned. Thus switching of an 8-bit word between an input channel and an output channel is achieved.

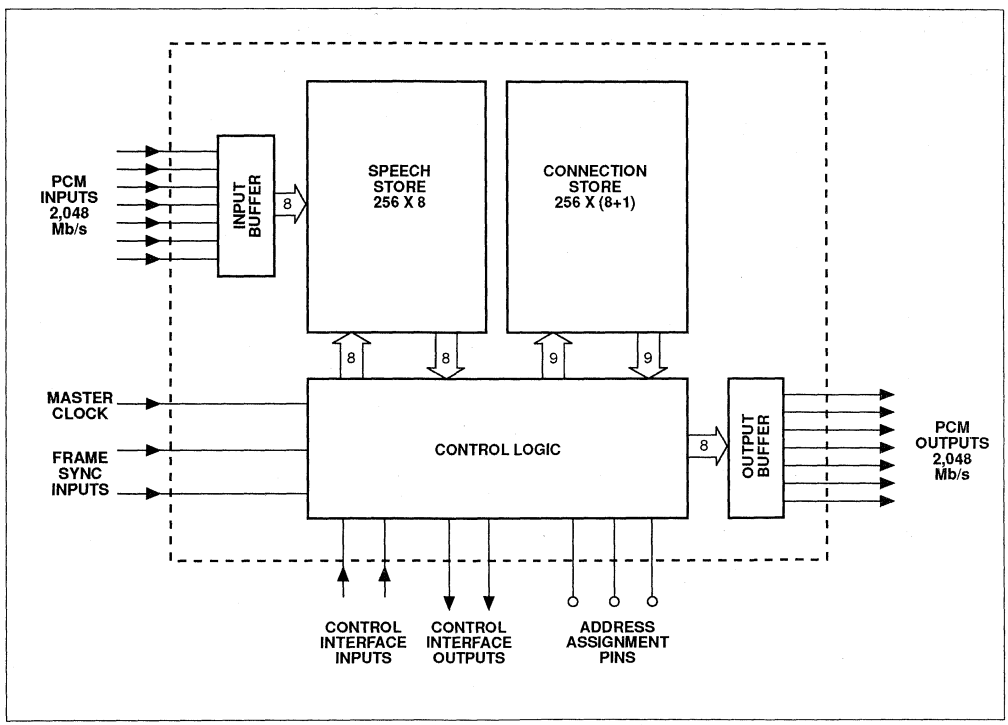


Figure 2: MA8112 block diagram

PIN DESCRIPTION

No.	Name	Function and Description
1- 8	DI0- DI7	SPEECH DATA INPUTS. These inputs carry the 256 8-bit channels (containing PCM encoded speech or datal in either serial or parallel format for switching. All eight input lines must be bit and timeslot synchronous. The start and format (i.e. serial or parallel) of an input frame is determined by the input frame synchronisation pulse on Pin 28($\overline{FSP1}$). Input and output channels are formatted and numbered as shown in Fig. 3 and the input channel timing is shown in Fig. 4.
10 - 17	DO7 - DO0	SPEECH DATA OUTPUTS. These outputs carry the 256 8-bit channels containing PCM encoded speech or data) in either serial or parallel format after switching. All eight output ines are bit and timeslot synchronous. The timing of the output frame relative to the input frame is determined by the input to Pin 9 (FSP2). These outputs are open-drain type and should be tied externally to V_{DD} using 1Kohm resistors.
9 28	$\overline{FSP2}$ $\overline{FSP1}$	FRAME SYNC PULSE INPUTS. A frame sync pulse input on $\overline{FSP1}$ provides a frame datum for the incoming data (on both the speech and control inputs) and indicates the active edges of the system clock. In addition the duration of the sync pulse low period determines the speech data input and output formats (i.e. serial or parallel) as shown in Table 1. The $\overline{FSP2}$ input is used to define the start of the output frame. If no frame sync pulse is provided on FSP2, the output frame will automatically start 21 bits after $\overline{FSP1}$ (mode 1), and will be timed by the negative clock edges alternate to those used for clocking the input frame.
22 - 24	P3 - P1	ADDRESS ASSIGNMENT PINS. These pins are each hardwired to V_{DD} Or V_{SS} in order to assign a unique address for up to eight DSMs in a matrix. This allows several DSMs to share the same control interface lines (CI0, CI1 and CO0, CO1).
21, 25	CI0, CI1	CONTROL INTERFACE INPUTS. These are serial control inputs into which all instructions and data regarding the addressing of the DSM, routing of the PCM inputs and outputs and channel insertion and extraction are entered. CI1 is the control instruction input. 8-bit words entered on CI1 correspond to, and control the 8-bit words entered synchronously on CI0, the control data input.
18, 19	CO0, CO1	CONTROL INTERFACE OUTPUTS. These are serial outputs which respond to the words received on the control interface inputs. There is a fixed response time of 21 bit periods between a control interface input word and the corresponding control interface output word. The control instruction output CO1 carries 8-bit words which refer to the words carried on the control data output CI0. These outputs are used to extract data from either the speech or connection memories. CO0 and C01 are open drain outputs and should be tied high externally using 1Kohm resistors.
26	CLK	MASTER CLOCK INPUT. This input requires a 4.096 MHz TTL level clock. All input signals are strobed on alternate falling clock edges (the active edge is assigned by the position of the input frame sync pulse FSP1). All output data is clocked out on the opposite alternate negative edges of the clock.
20	V_{SS}	NEGATIVE POWER SUPPLY PIN. Connect to 0v.
27	V_{DD}	POSITIVE POWER SUPPLY PIN. Connect to + 5v.

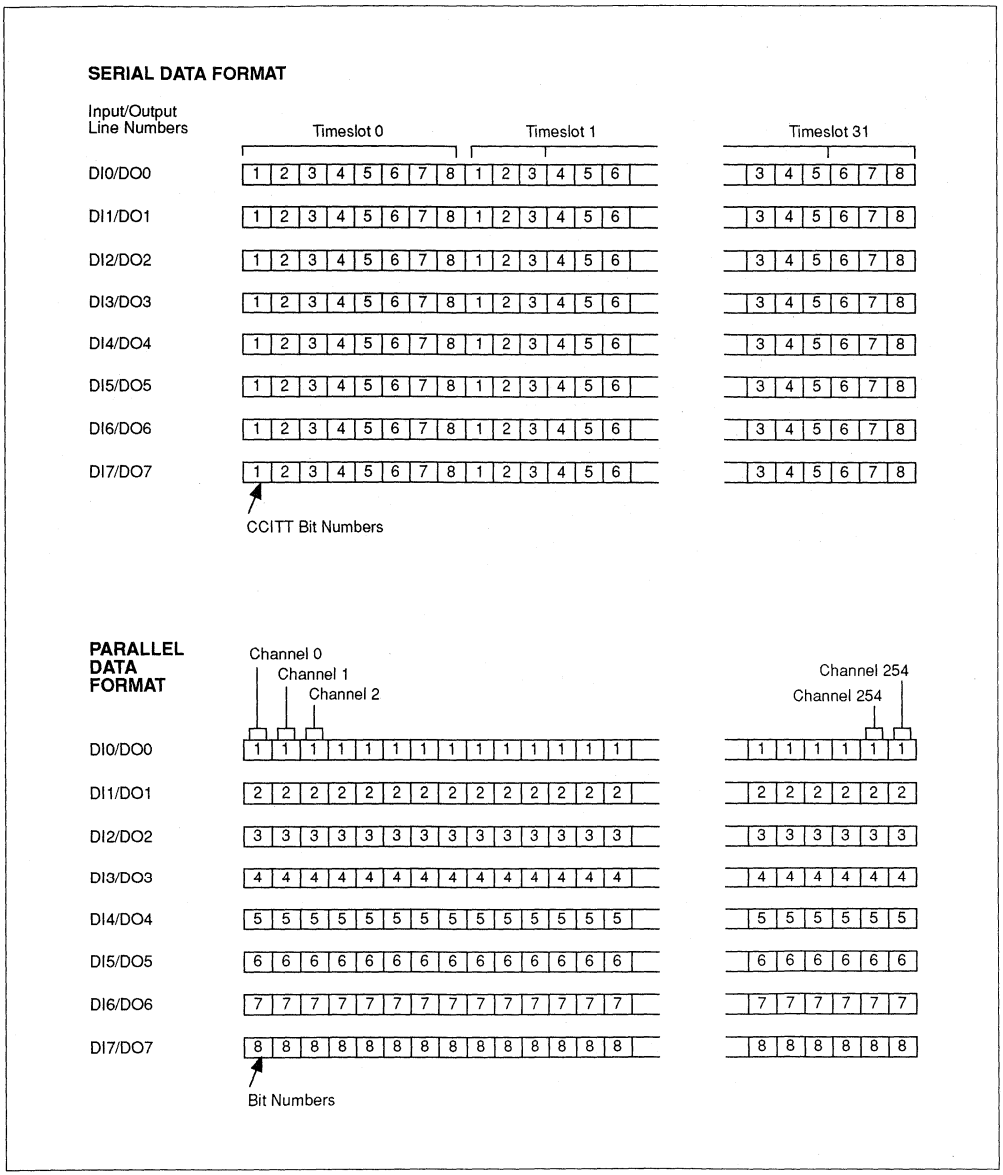


Figure 3: Input and output data formats

INTERFACE DESCRIPTION

TIMING INTERFACE

The following timing information signals must be provided to the MA8112:

(a) A 4.096 MHz master clock on CLK (Pin 26).

(b) An input frame synchronisation pulse on $\overline{FSP1}$ (Pin 28). This pulse must repeat every 125µs (i.e. every 512 master clock periods).

(c) (Optional).An output frame synchronisation pulse on FSP2 (Pin 9) which repeats every 125µs (512 master clock periods). If this is not provided, the MA8112 will default to assuming a start time for the output frame 21 bit periods after $\overline{FSP1}$.

The master clock is used to strobe all data into and out of the DSM. Data is clocked in on the speech data inputs (DI0-7) and the control interface inputs (CI0, CI1) on alternate falling edges of the master clock. The first active edge of the master clock in each frame is assigned by the timing of the input frame sync pulse $\overline{FSP1}$, as shown in Fig. 4.

$\overline{FSP1}$ also indicates a frame datum for the speech data inputs and control interface inputs, thereby allowing an input channel to be identified by its input line and/or input timeslot (Fig.4). The length of the frame sync pulse low period is used to determine the format of the data on the speech data inputs and outputs.

The input and output formats are explained in the Data Interface description.

The input frame sync pulse must repeat every 512 master clock periods to denote the start of each input frame.

The output frame sync allows the start of each output frame to be denoted in the same way as the input frames. If no pulse is provided on $\overline{FSP2}$, then the output frame starts 21 bits after the $\overline{FSP1}$ automatically. As $\overline{FSP2}$ is internally tied high by a resistor, it may be left open circuit.

Zero frame delay is achieved by tying $\overline{FSP2}$ to $\overline{FSP1}$.

The length of the pulse on $\overline{FSP2}$ has no relevance to the operation of the MA8112.

Length of FSP1 low period (clock periods)	Format
1	Serial In, Serial Out (SISO)
2	Serial In, Parallel Out (SIPO)
3	Parallel In, Serial Out (PISO)
4	Parallel In, Parallel Out (PIPO)

Table 1

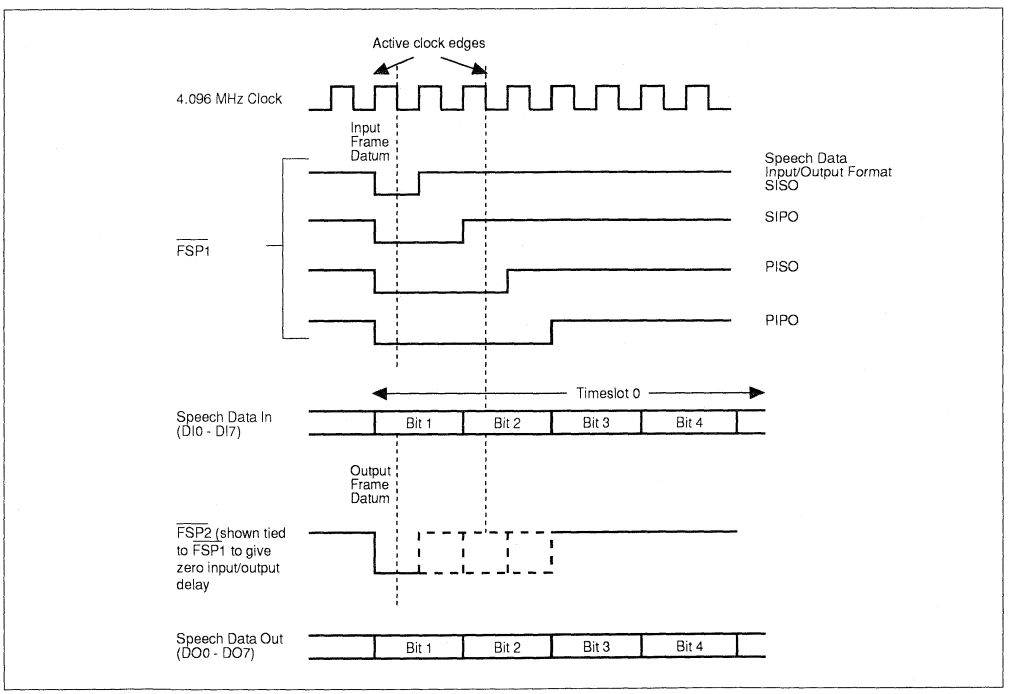


Figure 4(a): DSM timing diagram

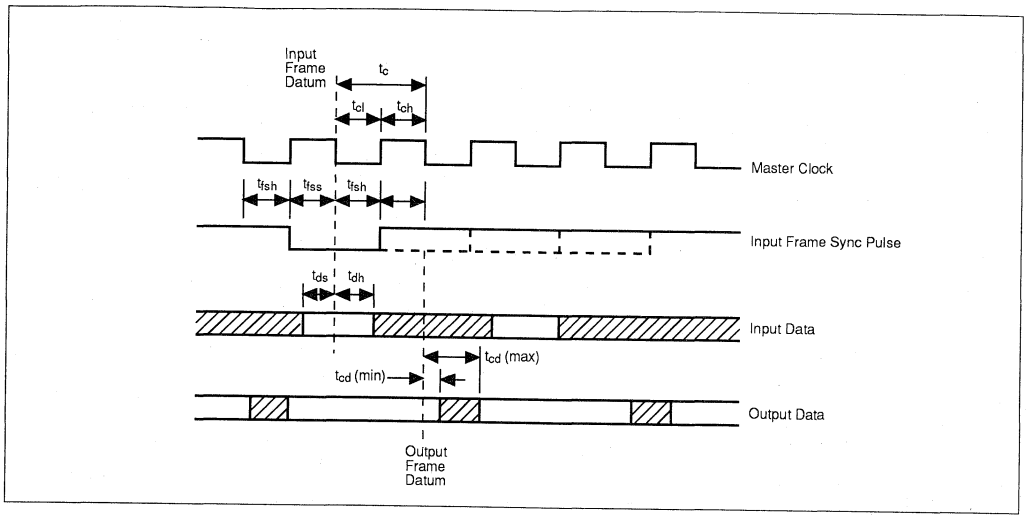


Figure 4b: Timing diagram

DATA INTERFACE

The data interface consists of eight input lines DI0-7 and eight output lines DO0-7. Input and output lines carry data at a rate of 2.048Mb/s. This allows 256 8-bit PCM or data channels repeating at a rate of 8 kHz to be switched from the input lines to the output lines.

The data on both the input and output lines is in frames arranged either as 32 serial 8bit channels on each of the eight input or output lines or, as 256 consecutive 8-bit parallel words on the eight input or output lines. These formats and the numbering scheme for the channels are shown in Fig.3. Any combination of parallel or serial input or output formats is possible and may be selected by the length of the input frame sync pulse on $\overline{FSP1}$ as explained in the timing interface description.

The input frames are clocked in by alternate negative edges of the master clock. All input lines must be both bit and channel synchronous with each other. The output frames are clocked on the other altemate negative edges to the input frames.

Outputs are open drain type and should be connected via a 1kohm resistor to V_{DD}. This allows several DSMs to be wire-ORed on to the same PCM lines in a matrix configuration.

CONTROL INTERFACE

The control interface consists of two input lines (CI0 and CI1) and two output lines (CO0 and CO1). The operation of the control interface is summarised in Table 2.

Control Interface Inputs

The two input lines receive data in the form of serial 8-bit words at the same rate, and synchronised with the data input lines DI0-DI7. Thus, 32 8bit words are received per frame.

Each 8-bit control instruction word received on CI1 corresponds to and controls the processing of the 8-bit control data word received in the same timeslot on CI0.

(a) Control Instruction word

The control instruction word format is shown in Fig. 5-

Each control instruction word refers to a specific connection memory location (and hence, also to a specific output channel). The connection memory location is addressed by a combination of the timeslot number in which the word is received and the three bits A0, A1, A2 within the control instruction word.

Bits S3, S2 and S1 are used to identify a particular DSM in an array. These bits are compared to the hardwired address assignment pins, P3, P2 and P1. If they match, the control instruction word is intended for this particular DSM and the DSM will respond accordingly (this is the normal mode in an application using only one DSM).

However, if P3 and S3 match, but either or both S2 and S1 do not match P2 and P1, the DSM will recognise that the message is intended for another DSM which shares the same control interface and speech data lines within a matrix (see Application note). This does not mean that the message is completely ignored. If the message specifies a write operation to a location in another DSM's connection memory, then this DSM will fill its corresponding location with all 1s(including B_{INT}) in order that its speech data output will go open drain on the same output line and timeslot as that of the addressed DSM. This facility allows a DSM matrix to operate particularly efficiently, as several DSMs can be wire-ORed onto the same control lines and when a new connection on to an output channel is made, previous connections from other DSMs are automatically removed.

In the case of a mismatch between S3 and P3, the control instruction word and the control data word are completely ignored as it is assumed that the message is for a DSM with outputs connected to other lines.

The R/$\overline{W}$bit is the read/write bit. H R/$\overline{W}$ = 0 the operation is a write operation then (subject to an address match on S3, S2 and S1) new data will be written to the appropriate connection memory location. This new data will consist of the 8-bit control data word loaded synchronously on CI0 and the external busy bit, B_{EXT} trom the control instruction word. B_{EXT} then becomes the internal busy bit B_{INT}, a ninth bit attached to the eight data bits in each connection memory location. If B_{INT} = 0, then an input channel to output channel connection is made, the location of the word in the connection memory indicating the output channel and the 8 bits at that location (loaded on CI0) indicating the input channel to be switched to the output channel. H B_{INT} = 1, the 8 bits in the connection memory are switched directly to the output channel. This facility allows an idle code to be inserted via the control interface when an output channel is unused.

(b) Control data word

Fig.5 shows the three possible formats for the control data word loaded synchronously with the control instruction word. If R/$\overline{W}$ = 0 and B_{EXT}= 0 in the CIW, one of the first two formats should be used (depending upon whether the speech data format is serial or parallel). If B_{EXT} = 1, the third format should be used as this is data to be sent to an output channel.

H R/W = 1 in the corresponding control instruction word, then the operation is a read and the data on CO0 is irrelevant.

Control Interface Outputs

The two control interface output lines, C01 and CO0 (Pins 19 and 18) transmit data in the form of serial 8-bit words in response to messages received on the control instruction input CI1. The outputs operate at the same data rate as the inputs(i.e.328-bit words per frame) and are synchronous with each other, each control instruction output word transmitted on C01 corresponding to the accompanying control data output word on CO0.

The delay time from input messages on CI0 and CI1 to the response messages on CO0 and C01 is 21 bit periods (the outputs are clocked on the other alternate falling edges of the master clock to the inputs). This is a fixed delay and does not vary with the input/output frame delay.

(a) Control Instruction output word

The format of the control instruction output word is shown in Fig.6. The information carried on C01 relates to the data on CO0. As explained earlier, each pair of control interface words on CI0 and CI1 refer to as pecific connection memory location, therefore, the control interface output words which form a response will also refer to the same connection memory location.

If the S3 bit in the control instruction word input on CI1 does not match P3, then the input message is ignored and the control interface outputs, C01 and CO0 will go open - drain (i.e. all 1 s) during the response timeslot.

When S3 = P3 on CI1, then the response word on C01 will always contain a reflection of the connection memory addressing bits A0, A1 and A2 and the R/$\overline{W}$ (read/write) bit on CI1. This information, together with the timeslot during which the output words are transmitted, provides the information on whether the input message was a read or write operation and which connection memory location (and, therefore, output channel) is being referred to. The remaining bits of the control instruction output word and the data contained in the corresponding word on COO will depend upon the operation being performed and the contents of the connection memory.

When R/$\overline{W}$ = 0 on CI1 (i.e. a write operation), then the corresponding control data output word on CO0 will reflect the new connection memory contents at the specified location and B_{INT} will, similarly, be reflected on C01. If the new contents of the connection memory location is all 1s, including B_{INT} (because either the input message was addressed to another DSM in a matrix or because all 1 s were specifically written to this location in this DSM) this will be reflected by the control data output CO0 going open - drain during the relevant timeslot. Also the S1, S2 and S3 bits on C01 will be set to one. If the word on CI1 was specifically addressed to this DSM and the connection memory location contents is not all 1 s, then S1, S2 and S3 will reflect the address of this DSM (i.e. P1, P2 and P3). As only one DSM in a matrix can have anything other than all 1 s in corresponding connection memory locations (because only one device can be active in a PCM output channel at a time) this arrangement ensures that only this DSM responds with the address in the relevant timeslot.

When R/$\overline{W}$ = 1 on the control instruction word on CI1 (i.e. a read operation) the data input on CIO is irrelevant. It is not necessary to specify which DSM is to be read from by matching S1 and S2 to P1 and P2 because when used on a matrix, only one of the DSMs with output lines wired together will contain any data other than all 1s in the connection memory location which is to be read. Therefore, only one DSM will respond to the read instruction by transmitting data on CO0 and a reflection of its address on C01 - other DSMs will go open-drain at the appropriate time. The status of the B_{EXT} bit in the control instruction input word determines whether the read operation refers to reading the word in the connection memory location or reading the PCM output channel associated with this location. If B_{EXT} = 0, the connection memory is read. If B_{EXT} = 1, the output channel word is read - this may be the word from the speech memory addressed by the contents of the connection memory or the word from the connection memory itself, depending upon the status of B_{INT} appended to this location.

(b) Control data output word

The four possible control data output word formats are shown in Fig. 6. Which format is applicable is determined by the information requested, and the format in which this data is stored on chip.

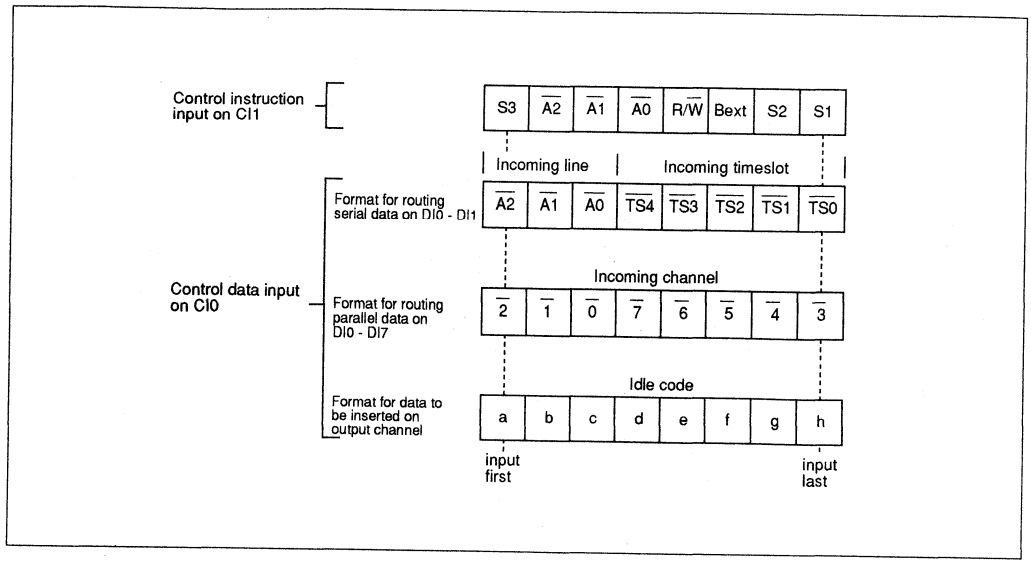


Figure 5: Control interface input message formats

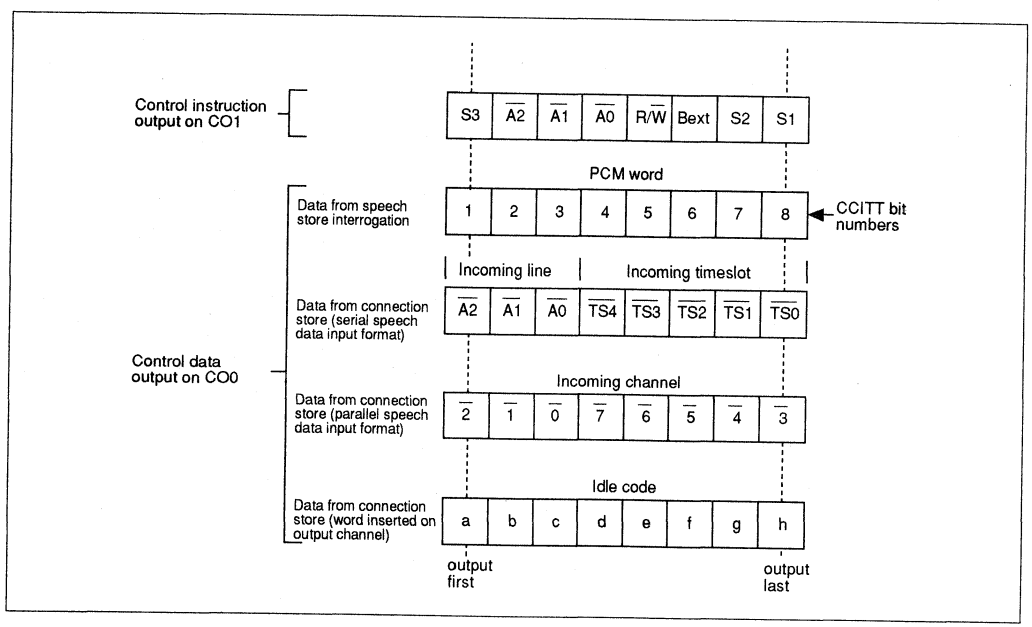


Figure 6: Control interface output message formats

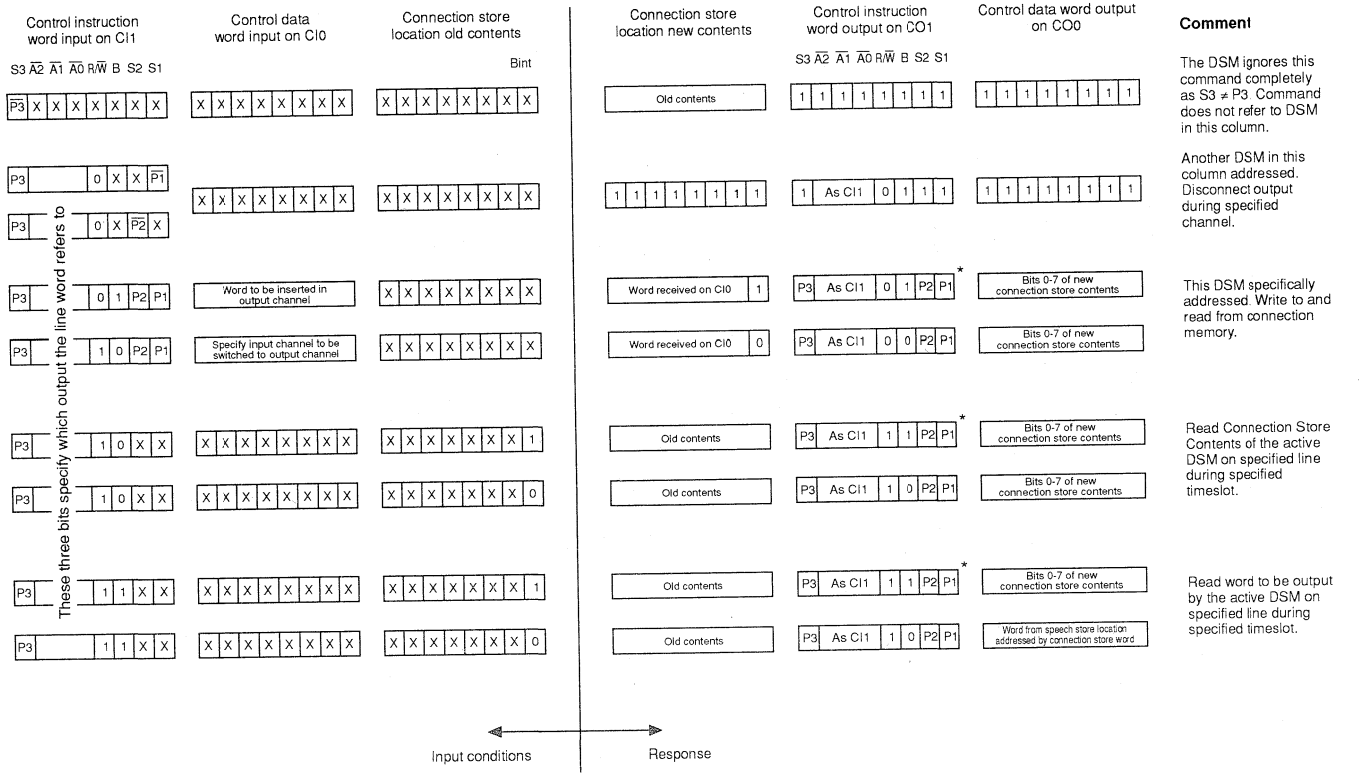


Table 2: Control interface operation

* Except when addressed connection store location contains all 1s. In this case S1, S2, S3 = 1.

X = Don't Care.

ADDITIONAL NOTES

CHANNEL NUMBERING

When the DSM is operated in a mixed input/output format mode, i.e. Serial In, Parallel Out, or Parallel In, Serial Out, it is necessary to be able to equate channel numbers.

MSB							LSB
TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0

In serial mode, a channel number is identified by taking the line number and timeslot number and assembling them as follows:

MSB							LSB
TS4	TS3	TS2	TS1	TSO	A2	A0	A1

DSM INTERNAL DELAYS

There is a fixed minimum internal delay through the DSM for PCM words which is that produced by format conversion and the memory read/write cycle within the DSM. This delay is 21 bit periods (i.e. 42 master clock periods) and is the shortest period in which an input word can be sent to an output channel.

If the $\overline{FSP2}$ input is left open circuit, then the fixed delay will be 21 bit periods, but if an output frame sync pulse is provided, the fixed delay will be up to 255 bit periods longer, dependent upon the timing of the $\overline{FSP2}$ relative to $\overline{FSP1}$.

The total delay tor any particular channel is equal to this fixed delay plus a variable delay determined by the time spent in the speech memory waiting for the relevant output timeslot.

The overall delay is given by the following relation:

$$D = F + (N - M) \text{ for } N \geq M$$
$$D = F + 256 + (N - M) \text{ for } N < M$$

} PIPO format

$$D = F + \left(\text{INT}\frac{N}{8} - \text{INT}\frac{M}{8}\right) \times 8 \text{ for } N \geq M$$
$$D = F + 256 + \left(\text{INT}\frac{N}{8} - \text{INT}\frac{M}{8}\right) \times 8 \text{ for } N < M$$

} SISO format

where

D = total delay in bit periods (488ns)
F = fixed delay in bit periods (21 bits or specified by FSP2)
M = Incoming channel number
N = Outgoing channel number

APPLICATIONS INFORMATION

Fig.7 shows how a 1024-channel DSM matrix can be constructed, providing four times the switching capacity of a single DSM. Note that the control interface allows DSMs connected to the same PCM output lines to be wire-ORed to common interface lines without additional logic.

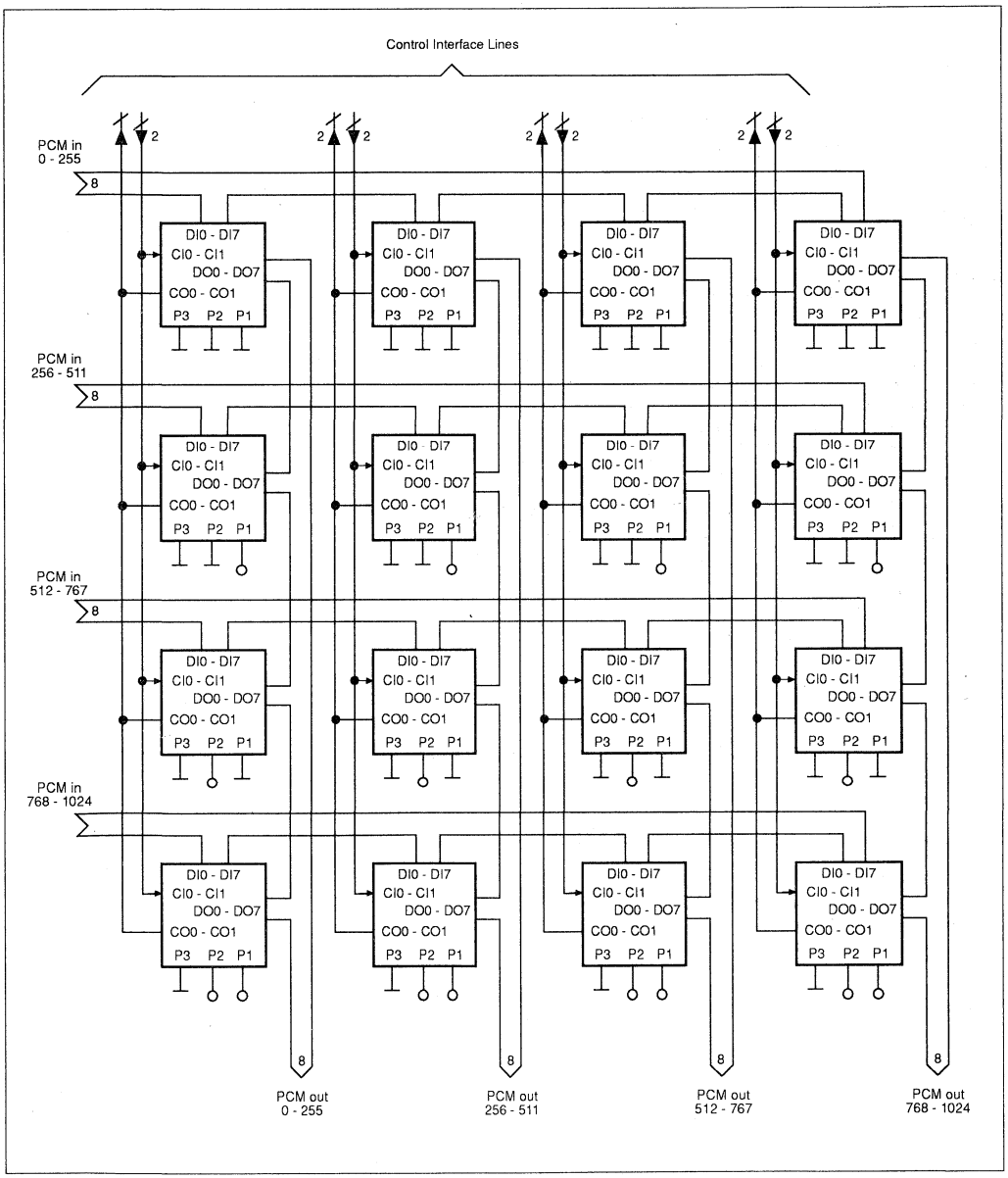


Figure 7

ABSOLUTE MAXIMUM RATINGS*

	Max	Units	Min
Supply voltage V_{DD}	-0.3	6.5	V
Voltage on any pin	V_{SS}-0.3	V_{DD}+0.3	V
Operating temperature	0	70	°C
Storage temperature	-55	+ 125	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS at V_{DD} = 5V ±%, Ambient temperature = 25°C

	Symbol	Min	Typ	Max	Units	Conditions
High level input voltage	V_{IH}	2.0			V	
Low level input voltage	V_{IL}	-0.3		0.8	V	
Supply current			<5	10	mA	CLK=4.096 MHz
Input current	I_{IH}			10	µA	$V_{IH} = V_{DD} + 0.3V$
	I_{IL}			10	µA	-0.3V V_{IL} 0.8V except Pin 9
				100	µA	-0.3V V_{IL} 0.8V Pln 9
Low level output voltage	V_{OL}			0.4	V	Rpu = 1 Kohm
High level output voltage	V_{OH}	2.8			V	Rpu = 1 Kohm
Input capacitance	C_i			5	pF	
Output capacitance	C_O			5	pF	

AC ELECTRICAL CHARACTERISTICS † at V_{DD} = 5V ±5%, Ambient temperature 0 to + 70°C

	Symbol	M in	Typ	Max	U nits	Conditiom
Master clock period	t_c	240	244	2400	nS	
Master clock low period	t_{cl}	80			nS	
Master clock high period	t_{ch}	80			nS	
Frame sync period	t_f	512		512		Master clock periods
Frame sync set up time	t_{fss}	50			nS	
Frame sync hold time	t_{fsh}	50			nS	
Input data set up time	t_{ds}	50			nS	
Input data hold time	t_{dn}	50			nS	
Master clock to output delay	t_{cd}	5		150	nS	

† See Fig. 4(b)

Section 3
Line Card Circuits

GEC PLESSEY
SEMICONDUCTORS

Subscriber Line Interface Circuit (SLICs) - Selection Guide

Functional Features	SL376 (p.199)	SL377 (p.227)	SL379 (p.254)
Line Feed Regulator	✓	✓	✓
Constant Current Feed (Normal, Active Region)		✓	✓
Resistive Feed (Normal, Active Region)	✓		
Off-Hook Detector (OHD)	✓	✓	✓
Off-Hook Detector Hysteresis			
Standby Mode	✓	✓	✓
Ring Trip Detector (RTD)	✓	✓	✓
Ground Key Detector (GKD)	✓	✓	✓
Detector Select Input, E1 (OHD/GKD)	✓	✓	✓
Detector Output Pin Enable Input, E0	✓		✓
Polarity Reversal (Active and Standby Modes)	✓	✓	✓
Meter Pulse Capability	✓		
Test Relay Driver		✓	
Ring Relay Driver	✓	✓	✓
On-chip Substrate Resistor	✓		✓

Functional Features	SL376 (p.199)	SL377 (p.227)	SL379 (p.254)
Standby Current Level	$K_{LIM} \times I_{DET}$	$K_{LIM} \times I_{DET}$	$K_{LIM} \times I_{DET}$
2-Wire Dynamic Range	±6V	±3V	±3V
Nominal Transmit Gain	-6dB	0dB	0dB
V_{CC} Supply Range	+5V ± 5%	+5V ± 5%	+5V ± 5%
V_{EE} Supply Range	-5V ± 5%	-5V ± 5%	-5V ± 5%
V_{BB} Supply Range	-44/ -52V	-40.5/ -64V	-40.5/ -64V
Off-Hook Threshold/s	350 ÷ R_{TH}	350 ÷ R_{TH}	350 ÷ R_{TH}
Line Voltage Saturation Guard (VSG)	16.5V	15V	15V

Current Package Options
DG28 (28-lead ceramic DIL) - Standad for SL376
DP28 (28-lead plastic DIL) - Optional for SL377 and SL379
HP32 (32-lead quad plastic J lead) - Standard for SL379
For details of optional and other types of packaging, please contact your local Customer Service Centre.

SL376

METERING SUBSCRIBER LINE INTERFACE CIRCUIT

The SL376 is a Subscriber Line Interface Circuit (SLIC) for use at the telephone exchange or PABX end of a telephone line.

It provides power feed, transmits and receives voice signals, controls ringing and detects Ground Key or Off-Hook conditions. These functions can be programmed to provide the flexibility required for different telephone networks. In addition, the SL376 allows injection of high frequency Meter Pulse signals on to the telephone line.

The SL376 is fabricated using bipolar technology.

FEATURES

- Low Power Line Feed via Regulator
- Constant Voltage Feed/Programmable Resistive Feed Independent of Battery
- Programmable AC Termination Impedance
- Good Longitudinal Balance
- Ground Key and Ring Trip Detection
- Programmable Off-Hook Detection
- Disconnect and Low Power Disable Modes
- A-Leg Disconnect, B-Leg Disable Mode
- Normal or Reversed Line Polarity Operation
- Supports High Frequency Meter Pulse Injection
- Ring Relay Driver
- Thermal Shut-Down Protection

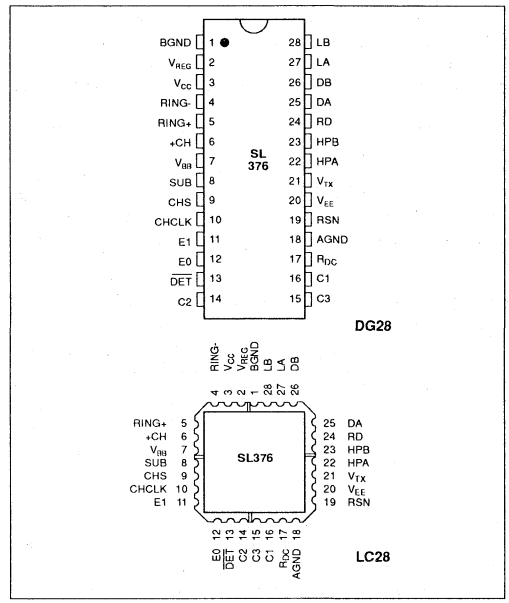


Figure 1: Pin connections - top view (not to scale)

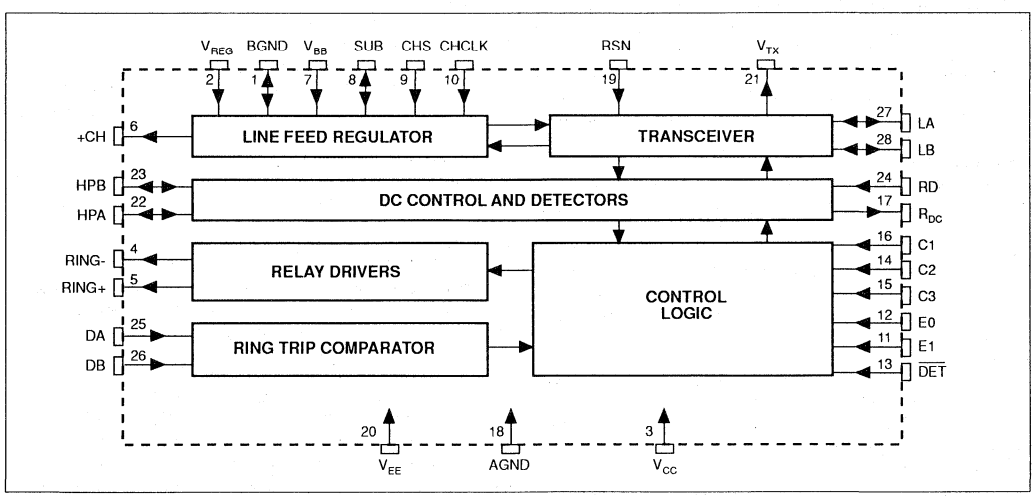


Figure 2: Functional block diagram

FUNCTIONAL OVERVIEW

The SL376 Metering Subscriber Line Interface Circuit (MSLIC). together with some external components, provides most of the line interface functions for ordinary or PABX line connections in a telephone network. It performs the interface between the two wire line and an ALAP (Analogue Line Audio Processor)/COMBO, such as the GEC Plessey Semiconductors MV3010-1 SLAC (Subscriber Line Audio Circuit) DSP device.

The MSLIC circuit contains several functional blocks to achieve the design aims (Fig.2). Firstly, the Transceiver consists of the two wire port, pins LA and LB. These pins are fed from the 4-wire input (RSN) controlling AC conditions, and from the Line Feed Regulator and DC Control blocks, controlling DC conditions. The 2-wire transverse AC signal is fed onto the 4-wire transmit output, V_{TX}.

Power dissipation is minimised, under varying line conditions, by the Line Feed Regulator which adjusts the internal high voltage supply to that required for line feed. It consists of a switching regulator, which can be synchronised to a 256kHz clock.

DC line conditions at the 2-wire interface are determined by the DC Control block. These DC conditions (modes of operation) are set by the Control Logic, which also monitors line status (On/Off-Hook) via the DC Control block detectors (Loop/Ground Key/Ring Trip comparator). The control logic also controls the Ring Relay Driver for Ringing mode of operation .

A brief outline of the device functionality is given below, before a more detailed discussion of the MSLIC circuitry in the Functional Description section.

LINE FEED

Line loop (pins LA & LB) feeding is obtained from the battery supply (pin 7) by means of an internal power circuit, which can be set to different modes of operation (refer to table 2). These modes are as follows:

Disable Mode

Disable mode is the MSLIC's low power mode in which the battery feed circuit limits the DC loop current to a level just sufficient to enable the MSLIC to detect current above the On/Off-Hook threshold. This mode is used when the subscriber is On-Hook, to save power, and is only used briefly when Off-Hook is detected (see Line Feed Regulator). Both the Loop and Ground Key detectors work in this mode.

Disconnect A and B Leg

This mode programs the SLIC such that the A and B leg output amplifiers are turned off, preventing current flow to the line.

Disconnect A, Disable B Leg

This is the MSLIC Disable mode with the A Leg amplifier turned off, so that current can only flow in the B Leg. In this state it is only possible to detect the application of a ground to the B Leg.

Active Mode

This is the normal operating mode with a call in progress. The MSLIC is used as a constant current feed device, (unbalanced DC line feeding is performed), with the feed current being set by external resistors.

Polarity reversal

The polarity of the feeding voltage at the MSLIC can be reversed on command, in Active and Disable modes. All Active and Disable conditions apply equally to the respective reverse conditions. In these conditions the polarity of any DC parameter is reversed.

Ringing

This mode enables the Ring Relay output and selects the Ring Trip comparator. It does not provide DC line feed or AC ringing voltage which must be supplied externally (via the Ring Relay).

SUPERVISION

The MSLIC provides an Off-Hook (or loop) Detector (OHD), Ring Trip Detector (RTD) and a Ground Key Detector (GKD). These are described below, in addition to the MSLIC on-chip thermal protection.

Off-Hook Detector

The Off-Hook Detector recognises the loop status by means of a threshold circuit. The OHD operates in Disable and Active modes (with or without polarity reversal), and in the presence of longitudinal currents. The detector threshold is nominally the same in Disable and Active modes, the actual level being externally programmable.

Ring Trip Detector

This detects when a subscriber goes off-hook during the application of a ringing signal (normally 25Hz) within a maximum delay of 150ms (determined by external components - see Applications section). The detector is active when the Ring Relay Driver is activated.

Ground Key Detector

The GKD circuit detects a current path from the A or B Leg to ground. It can be used in Disable, Active and Disconnect A Disable B modes.

Thermal Protection

In conditions which cause the chip junction temperature to rise above a critical level (around 140°C), the thermal protection will operate. This switches off the line current and therefore reduces the power dissipation

TRANSMISSION

The signal transmission functions include 2 to 4-wire and 4 to 2- wire conversions.

The 2-wire termination impedance of the MSLIC is programmed by external components. Transmit and Receive Gain are fixed and are nominally both unity (OdB). with the 2-wire port terminated in a matched load.

All the transmission parameters apply when the MSLIC is operating in the presence of longitudinal currents, as specified in the Electrical Characteristics.

CONTROL

The MSLIC is provided with a digital interface for controlling the 2-wire line status and passing line status information to the line card/system hardware. The operating characteristics can be selected by hardware with external components (see Digital Interface).

SIGNALLING (METER PULSE INJECTION)

The injection of high frequency Meter Pulses (SPM) can be carried out through the MSLIC. This signal is added to the normal 4 wire receive signal at the RSN pin (pin 19). It could be externally switched into the receive path under control of an ALAP/SLAC digital output.

The 4 wire transmit output, VTX, will include any meter pulse signalling. It may be necessary to add an external SPM notch filter in the final application solution, to prevent overload of the dynamic range of the ALAP/SLAC analog input.

RINGING

The application of the ringing voltage to the subscriber line can be via a relay or suitable high voltage crosspoint, external to the MSLIC. This component is driven by the on-chip Ring Relay Driver. The relay is connected between RING + and a + 5V supply with RING- grounded, or between RING- and VBAT with RING + connected to a supply voltage between BGND and V_{CC}. When the MSLIC is set to RING mode, the Ring Relay Driver output will be activated to energise the ring relay. The relay should be connected so as to cause the line to be disconnected from the MSLIC and connected to a suitable ringing supply (continuous) voltage. Ring cadence can then be obtained by de-energising and re-energising the relay as required.

OVERVOLTAGE PROTECTION

Overvoltage protection is required to protect the SLIC from such line phenomena as lightning strikes, and induced AC signals from, or direct contact with, power lines. This protection can be realised with components external to the SL376 (refer to SLIC Application Note AN82).

TEST ACCESS

The testing of the subscriber line is achieved using components external to the SL376.

INTERFACES

The SL376 has three main interfaces to external circuitry. These are the 2-wire, 4-wire and Digital interfaces which are described below.

Subscriber Line Intertace (2-wire port)

Pins LA and LB form the Subscriber Line Interface providing line feed, signalling supervision and voice transmission between the subscriber's apparatus and exchange. It exhibits very good balance about ground to minimise the crosstalk between adjacent pairs in the local cable and noise from longitudinal interference. The termination impedance is set externally by Z_{TX} (see Fig. 3 and Functional Description).

The 2-wire port is designed to offer a low impedance to any longitudinal signals that appear on the subscriber line and the resulting signal level at the 4-wire output port is minimised. It is able to handle longitudinal currents on the subscriber line in all modes of operation, except Disconnect, Ringing and Disconnect A Disable B modes when the MSLIC 2-wire port is no longer connected to the line.

Analog 4-wire intertace

Two pins of the MSLIC (V_{TX} and RSN), together with associated grounds, provide the 4 wire interface to an ALAP or COMB0 device. Both the transmit (V_{TX}) and receive (RSN) signals are unbalanced and have fixed gain settings. The V_{TX} pin has a low output impedance, whilst the RSN pin is a low impedance virtual earth input. The input current is normally a combination of the receive voice signal from the ALAP, line feed current programmed by the RDC pin (see Applications

Pin designation	Pin description
C1	Data input
C2	Data input
C3	Data input
E0	Detector data output enable
E1	Detector select input
$\overline{DET}$	Detector data output

Table 1: Digital interface pin designation

Mode	C3	C2	C1	E0	DET output status (Note 2)	
					E1 = 0	E1 = 1
Disconnect A & B Legs	0	0	0	1	(Invalid)	(Invalid)
Ringing	0	0	1	1	Ring Trip (Note 3)	-
Active (non-ringing)	0	1	0	1	Loop Detect	Ground Key
Disable	0	1	1	1	Loop Detect	Ground Key
Disconnect A, Disable B	1	0	0	1	Ground Key	(Invalid)
Reserved	1	0	1	1	-	-
Active, polarity reversed	1	1	0	1	Loop Detect	Ground Key
Disable, polarity reversed	1	1	1	1	Loop Detect	Ground Key
As selected by C1 - C3, E1 (note 1)	0/1	0/1	0/1	0	1 (off)	1 (off)

NOTES

1. C1, C2, C3 still change MSLIC status even though $\overline{DET}$ output is forced to 1 (5V).
2. $\overline{DET}$ = 1 for On-Hook (high line impedance), $\overline{DET}$ = 0 for Off-Hook (low line impedance).
3. $\overline{DET}$ = 1 for Voltage DA > DB, $\overline{DET}$ = 0 for Voltage DA < DB.

Table 2: Digital interface functional description

section), termination of the V_{TX} pin and injected Meter Pulse signals.

Hybrid Balancing is not provided on the SL376. This can be done by an ALAP such as the MV3010-1 SLAC which uses DSP techniques, including an Adaptive Echo Cancellation feature.

Digital Interface

This is a parallel interface providing control of all the MSLIC operating modes and indication of line status information. It consists of the 6 pins as listed in Table 1, the functions of which are described in Table 2.

FUNCTIONAL DESCRIPTION

VOICE TRANSMISSION AND RECEPTION

It is conventional to assign the signal directions from the point of view of the served telephone set. The receive direction is towards the served telephone and the transmit direction is from it.

The basic voice circuit for the device is shown in Fig.3. The current which flows on the line, into LA and out of LB, is 1000 times the current which flows into RSN and through the device to AGND.

The AC voice current flowing into RSN is composed of the current from V_{RX} through Z_{GR}, which controls the signal received at the remote telephone and a current from VTX through Z_{TX} which controls the termination impedance and a current from V_{RM} through Z_{GM} for injection of Meter Pulse signals. There is also a DC current at RSN which is analysed later in the discussion on DC line feed.

The 2-wire termination impedance is $Z_{AB}=(Z_{TX} \div {}^1/_2\alpha)$ where a ($\cong$1000) is the current gain between RSN and I_L (see Fig.3). This can be checked by setting V_{RX} to zero. The factor of $^1/_2$ is due to the nominal Transmit Voltage Gain of -6dB, which prevents overload of the dynamic range during Meter Pulse signalling.

The receive gain, for normal voice signals (at V_{RX}). is inversely proportional to Z_{GR}. The actual value, which is negative, can be obtained by setting $(V_L)_{ac}$ equal to zero in Fig.3. This gives:

AC voltage between LA and LB $(V_{LA}-V_{LB})_{ac}$

$= (V_{LA}-V_{LB})-(V_{HPA}-V_{HPB})$

$= (I_L)_{ac} \times \{Z_{AB}||Z_L\}$

$$= -\left(\frac{Z_L \times \frac{Z_{TX}}{{}^1/_2\alpha}}{Z_L + \frac{Z_{TX}}{{}^1/_2\alpha}}\right)\frac{V_{RX}}{\frac{V_{GR}}{\alpha}}$$

i.e. minus the ratio of the line and terminating impedances (Z_L and $Z_{TX} \div {}^1/_2\alpha$) in parallel, to the receive impedance divided by the current gain ($Z_{GR} \div \alpha$). This expression simplifies to:

$$= \frac{-2\alpha Z_L Z_{TX} V_{RX}}{(\alpha Z_L + 2Z_{TX})Z_{GR}}$$

To obtain receive gain for the meter pulse input, V_{MT}, this will have a similar expression except that Z_{GM} is substituted for Z_{GR}.

In the transmit direction, the voltage at V_{TX} is the superposition of the voltage from the line, with the voltage produced on the line from V_{RX}, i.e:

$$V_{TX} = {}^1/_2\left[\left(\frac{\frac{Z_{TX}}{{}^1/_2\alpha}}{Z_L \div \frac{Z_{TX}}{{}^1/_2\alpha}}\right)V_L - \left(\frac{Z_L \times \frac{Z_{TX}}{{}^1/_2\alpha}}{Z_L \div \frac{Z_{TX}}{{}^1/_2\alpha}}\right)\frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}\right]$$

This expression simplifies to :-

$$V_{TX} = \frac{[(V_L)_{ac}Z_{GR} - \alpha Z_L V_{RX}]Z_{TX}}{(\alpha Z_L + 2Z_{TX})Z_{GR}}$$

This equation can be used to determine the transmit gain from $(V_L)_{ac}$ to V_{TX}, by setting $V_{RX} = 0$, which gives $(Z_{TX}) \div (\alpha Z_L + 2Z_{TX})$ Alternatively, by setting $(V_L)_{ac} = 0$ we obtain the 4-wire to 4 wire gain, V_{RX} to V_{TX}, giving the expression $-\alpha Z_L Z_{TX} \div [(\alpha Z_L + 2Z_{TX})Z_{GR}]$. If fuse resistors are included in the 2-wire loop, then Z_L is modified to become $(Z_L + 2R_F)$ in the above equations.

The transmission circuitry also contains a longitudinal feedback circuit, such that the MSLIC appears as typically 25Ω resistors from LA and LB to a bias voltage (see DC Line feed section). This bias voltage comes from the DC feed circuitry. The feedback circuit attenuates longitudinal signals from the transmit path, and has no effect on transverse signals.

DC LINE FEED (ACTIVE MODE)

DC line feed (loop) current $I_L = {}^1/_2|I_A-I_B|$ is provided by the device when it is in non-ringing modes. In ringing mode, DC line feed and AC ringing voltage are normally applied through the ring relay which is controlled by the device. The line feed current is reduced during standby operation.

In Active mode, Power feed is controlled by the resistance R_{DC} between the R_{DC} pin and the RSN pin (Fig.4). Again, the current in the 2 wire loop will be 1000 times the current into RSN. Operation of the DC feed circuitry is described with reference to Fig.4, which shows a conceptual model.

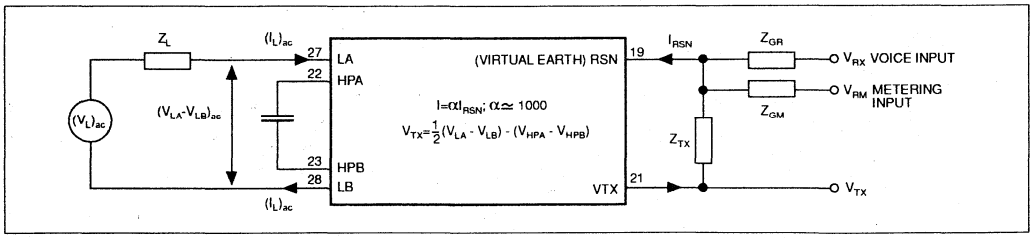


Figure 3: Voice circuit

For the normal line feed region, a voltage V_{DC}, of magnitude (50—$|V_{DCT}|$) ÷ 20 (where $V_{DCT} = |V_{LA} - V_{LB}|$) is produced at the R_{DC} pin (Pin 17), the sign of which determines normal or reverse polarity operation. If negative, normal polarity is established and if positive, reverse polarity will occur (polarity is set by control logic see Table 2). This normal line feed region exists when $|V_{BAT}|-|V_{DCT}| \geq V_{SG}$ (V_{SG} = 15V nominally, $V_{DCT} = |V_{LA}-V_{LB}|$), else the Saturation Guard circuit is active (described later).

Note that the internal resistors, RHP, and external capacitor, C_{HP}, form a low pass filter network (this is discussed further in Application Note AN82, Applications General Considerations section). During the action of reversing polarity, the resistors R_{HP} are momentarily shorted to reduce the time taken for the DC voltage on C_{HP} to change sign.

The combination of the 1/20 Op Amp and the x1000 virtual earth input current amplifier, means that the feed resistance is determined by (R_{DC} ÷ 50). i.e. $R_{FEED} = R_{DC} \div 50 = [(R_{DC1} + R_{DC2}) \div 50]$. If fuse resistors are included in the 2-wire loop, then the actual feed resistance will be:-

$$R_{FEEDTOT} = 2R_{FUSE} + R_{FEED} = 2R_{FUSE} + [(R_{DC}) \div 50]$$

As an example, to set $R_{FEEDTOT}$=840Ω, then if the resistors R_{FUSE} = 20Ω, then $R_{DC1} = R_{DC2}$ = 20kΩ, since:-

$$(R_{DC1} + R_{DC2}) = [R_{FEEDTOT}-2R_{FUSE}] \times 50$$
$$=[840 - 40] \times 50 = 40k\Omega$$

The values of R_{DC1} and R_{DC2} should be kept equal, forming a low pass filter network with C_{DC} to reduce chopper noise from the R_{DC} pin (see also discussion in AN82 Applications General Considerations section). The time constant of this network (C_{DC} and R_{DC1} // R_{DC2}) also affects the time taken for a polarity reversal, and it is normally ≈1.5ms.

The remaining circuitry models the action of the saturation guard circuit. This operates to reduce the voltage at the R_{DC} pin when:- $|V_{BAT}|-|V_{DCT}| < V_{SG}$. V_{SG} is a notional threshold voltage which is the headroom between the value of V_{DCT} and the battery voltage, at the point where Saturation Guard becomes active (this includes the diode drop in series with the V_{BAT} supply, D_2 Fig. 7). Thus, when the comparator determines the above condition, the magnitude of the difference is used to reduce the voltage at R_{DC}.

The total line feed characteristic is shown graphically in Fig. 6a and 6b. The nearly constant voltage region (V_{DCT} constant) is due to the action of the saturation guard circuit. Fig. 6b plots the loop current value as a function of line resistance R_L The example shown is that of an 800Ω feed resistance, the graphs being obtained by using the simple models of Figs. 5a and 5b (0Ω) fuse resistors). Figs. 6a and 6b also show the action of V_{BAT} on the line characteristics.

With the saturation guard inactive, normal line feed conditions apply such that the feed and line/loop resistance determine I_L by the following relationship:

$$I_L = 50 \div (R_L + R_{FEEDTOT})$$

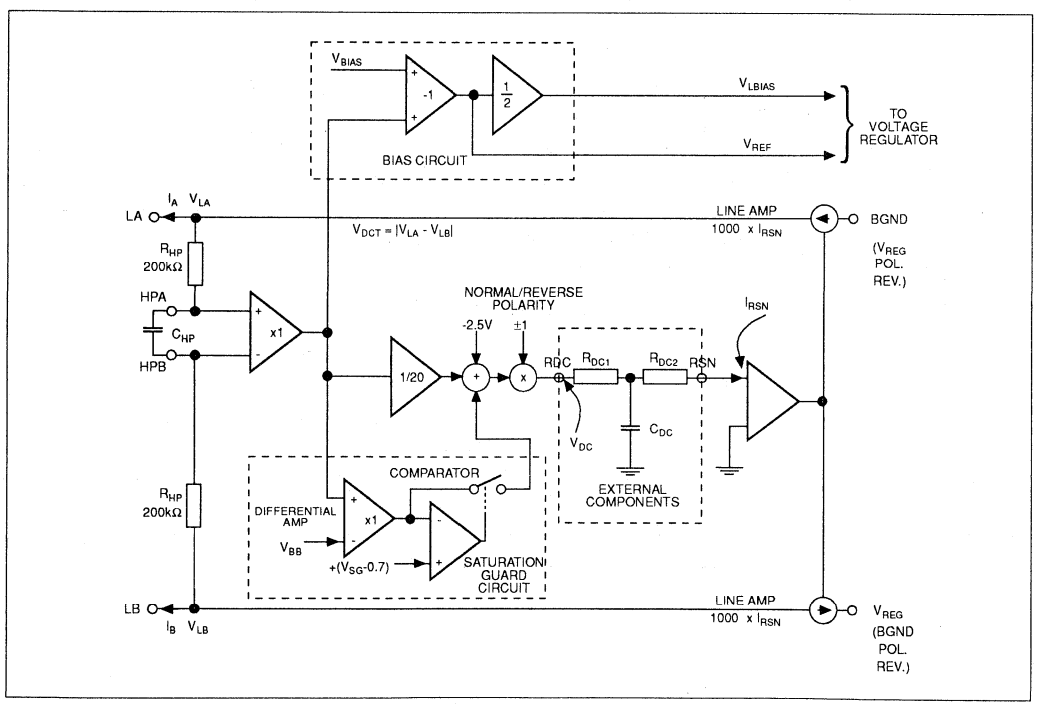


Figure 4: DC power feed circuit model

The line voltage is then simply determined by the relationship $V_L = I_L \times R_L$. This gives the example shown in Fig. 6a and 6b.

When the saturation guard is active, then the line voltage is effectively held constant due to the reduction of the voltage at the RDC pin. Thus, line conditions are set by the following:

$$I_L = [(|V_{BAT}|-V_{SG}) \div (R_L + 2R_{FUSE})]$$

To determine the line resistance (R_{LSG}) and current (I_{LSG}) at which the saturation guard becomes active, these parameters are obtained by equating the two expressions for Normal and Saturation Guard regions. Thus :-

$$I_{LSG} = \frac{50\,(50 + V_{SG}-|V_{BAT}|)}{R_{DC}}$$

$$R_{LSG} = \frac{(|V_{BAT}|-V_{SG})R_{DC}}{(50 + V_{SG}-|V_{BAT}|)50} - 2R_{FUSE}$$

The resultant line voltage (V_{LSG}) that occurs is obtained by the ohmic relationship of I_{LSG} & R_{LSG} (see Fig. 6a). This will become $V_{LSG} = (|V_{BAT}|- V_{SG})$ when $2R_{FUSE} = 0$. The open circuit line voltage $V_{LOC} \approx (|V_{BAT}|-V_{SG})$ at $R_L = \infty\Omega$ will always be greater than V_{LSG}. even when $2R_{FUSE} = 0\Omega$. This change in voltage between V_{LSG} and V_{LOC} will be greater at lower battery voltages. Fig. 6a shows the nominal effect.

DC LINE FEED (DISABLE MODE)

For Disable mode, the DC current is limited to a value just sufficient for the loop Detector to sense Off-Hook.

Normally this threshold (I_{DET}) is set externally by a resistor, R_{TH} (see Control and Signalling section). The limited loop current (I_{LIM}) is also determined by R_{TH} via a conversion factor K_{LIM} (nominally 1.7, see Electrical Characteristcs) such that:

$$I_L \leq I_{LIM} = K_{LIM} \times I_{DET}$$

The slope impedance of this characteristic is almost a constant current, as shown in Fig. 6a Since $K_{LIM} > 1$, the current level is still sufficient to detect the Off-Hook threshold (see Control and Signalling section).

LINE POLARITY

Normal polarity (in active or Disable modes) consists of the LA pin DC voltage near BGND and the LB pin DC voltage near V_{BB}. Under these conditions. $I_L = +{}^1/_2(|I_A-I_B|)$ and the voltage at the R_{DC} pin is negative. Reverse polarity will give the LA pin DC voltage near to V_{BB}, LB pin DC voltage near to BGND, $I_L = -{}^1/_2(|I_A-I_B|)$ and the R_{DC} pin voltage is positive.

BIAS CIRCUIT

The Bias circuit (Fig 4) produces two reference voltages, both referred to ground. These are V_{REF}, being related to the 2-wire transverse DC voltage and V_{LBIAS} approximately half V_{REF}.

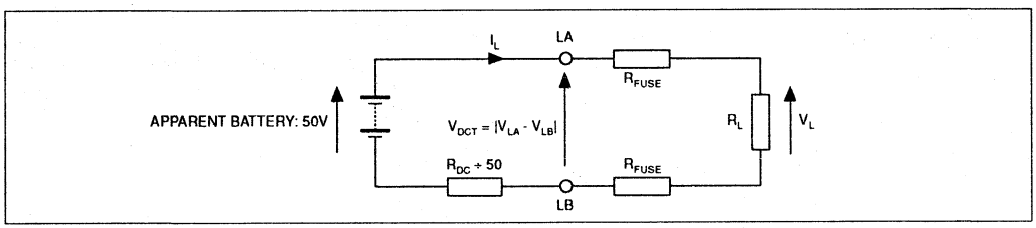


Figure 5a: Simple power feed model (normal line feed)

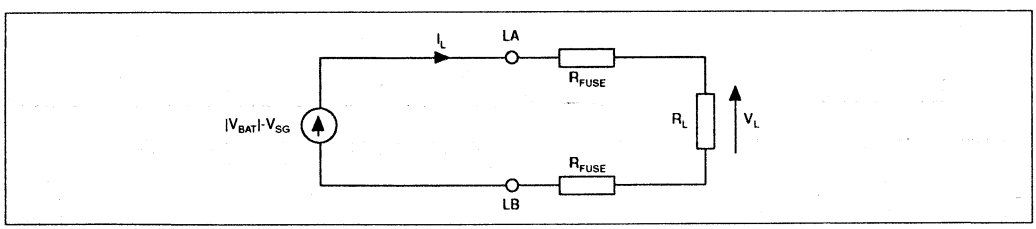


Figure 5b: Simple power feed model (saturation guard active)

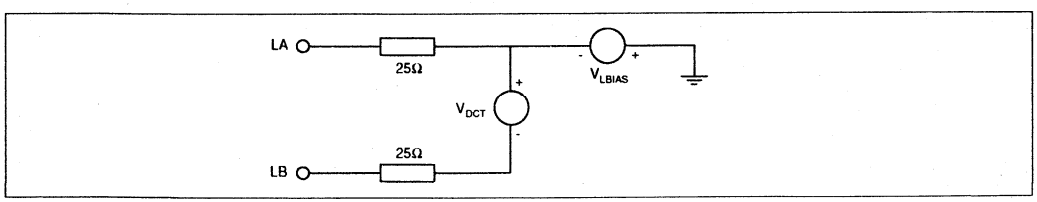


Figure 5c: Longtitudinal bias circuit

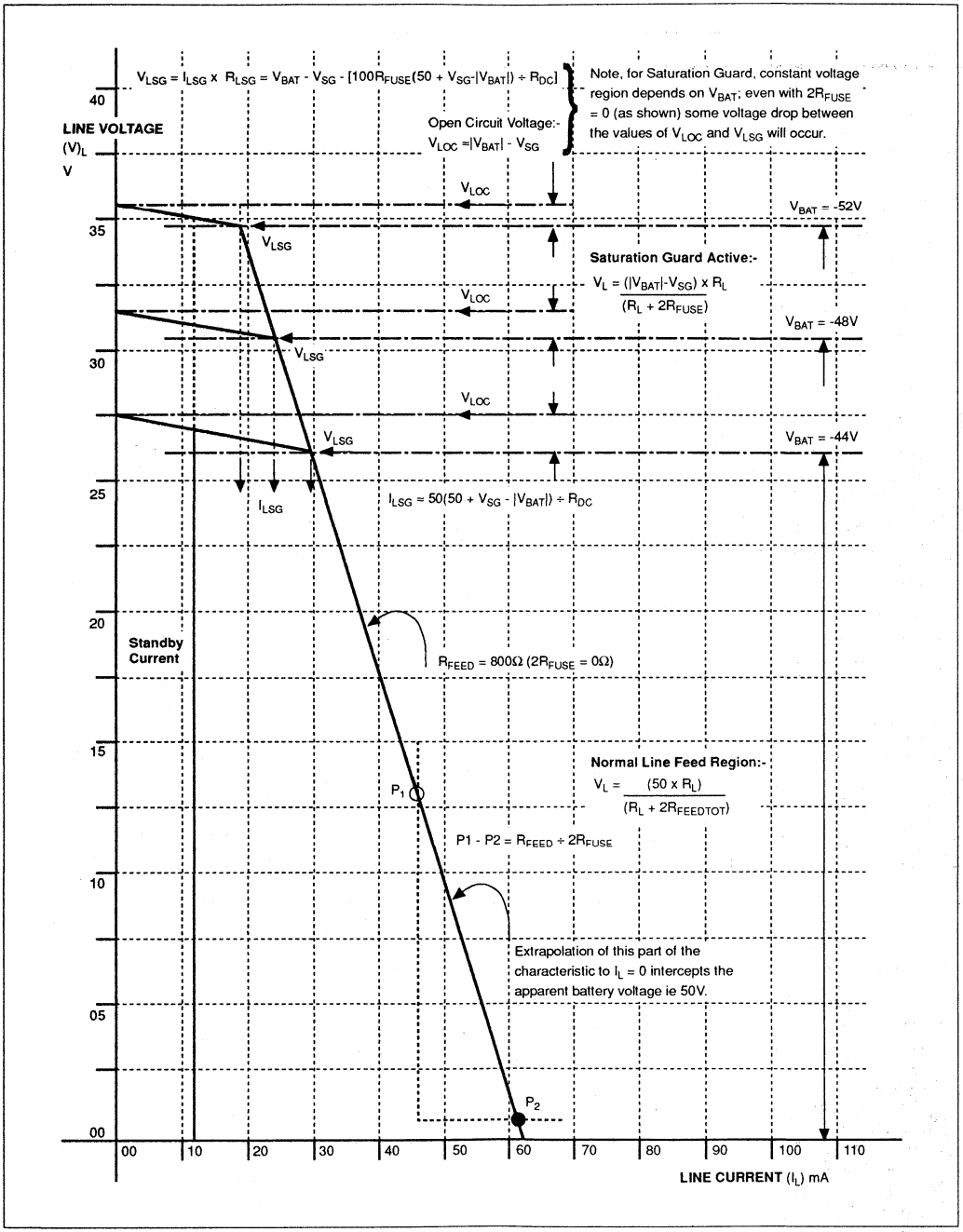


Figure 6a: Line feed characteristic, V_L vs I_L

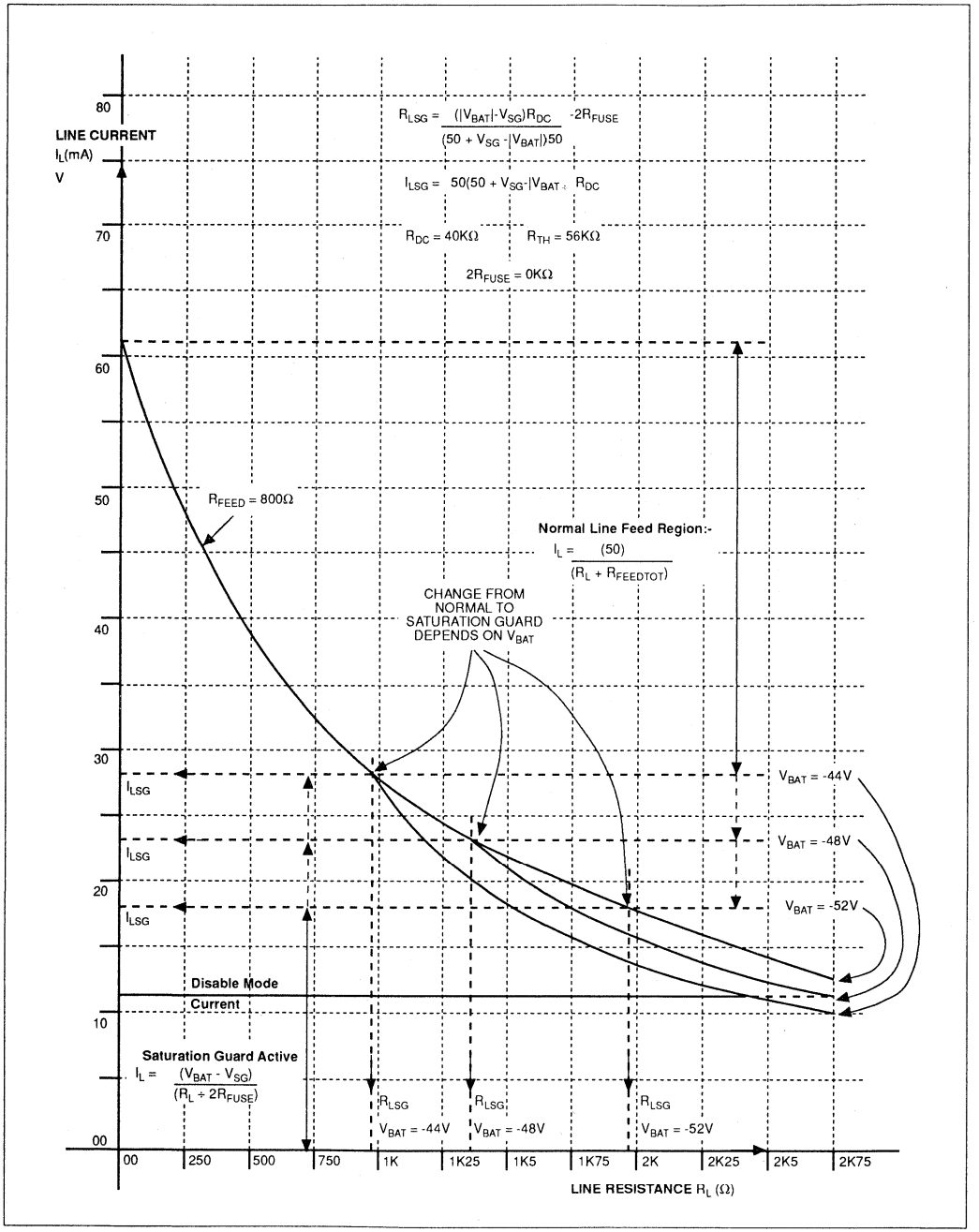


Figure 6b: Line Feed Characteristic, I_L vs R_L

V_{REF} controls the line feed regulator and V_{LBIAS} sets the 2-wire feed balance voltage (centre point voltage of the lines). The longitudinal control loop achieves an input impedance of approximately 25Ω per line for longitudinal signals, as shown in Fig. 5c.

LINE FEED REGULATOR

The DC voltage between LA and LB will vary with the DC loop resistance. Unless the voltage supplied to the chip can be varied to match that on the line there will be a voltage drop across the chip along the path taken by the feed current. This could cause significant power dissipation. The purpose of the line feed regulator is to minimise this power dissipation by regulating the voltage supplied to the line amplifiers.

Regulated voltage is supplied to the line amplifiers on V_{REG} and unregulated voltage is supplied on V_{BB}. The chip switches V_{BB} onto +CH when more power is required at the V_{REG} pin. V_{REG} is the voltage used by the device to power the 2-wire interface, and it is adjusted to follow a reference voltage V_{REF} (from Power Feed). This reference voltage is determined as follows:

$$V_{REF} = -\{ | V_{DCT} | + V_{BIAS} \}$$

and is such to set V_{REG} to the minimum required to power the line interface, thus minimising power dissipation. The voltage V_{BIAS} is needed to keep the amplifier response linear when audio signals are transmitted.

Fig. 7 shows the external components associated with the power supply aspect of the voltage regulator. +CH is the positive terminal of the regulator switch that connects to V_{BB}. When the switch is turned on, current in L_1 and C_1 increases, thus increasing stored energy. When the switch turns off, this stored energy sustains L_1 current which flows in D_1.

The voltage at +CH is thus a square wave of up to 50V p-p making this node sensitive to PCB layout. Note that the inductor should be capable of taking twice the line current without saturating. The regulator will work with a wide range of inductor resistance, although if this is too large, long line drive capability and regulator efficiency will be reduced. Since there are large current fluctuations from V_{BB} through the switch, C2 provides filtering of the VBB pin, whilst D_2 isolates the V_{BAT} supply should the LA/LB pins be taken negative of the V_{BAT} supply.

The chip senses the voltage at V_{REG}, compares it to its requirements and switches power from V_{BB} to +CH, using the variable mark/space method, to give appropriate matching. The rate of switching can be governed by CHCLK (pin 10) or allowed to free run, its stability ensured by the network on CHS (pin 9), i.e. C_3, R_1, C_5. Since noise is produced by the switching, a decoupling node is provided at SUB (pin 8).

Note that the regulator is powered down in Disable mode to further reduce power dissipation. It is intended that the SLIC will be put into active mode once Off-Hook has been detected, since in this state excessive power dissipation may result. This is discussed further in AN82.

CONTROL AND SIGNALLING

The mode of operation of the SL376 is determined by the digital interface pins, as described in Tables 1 and 2. These pins enable ringing or non-ringing modes of operation, controlling line status, line polarity, relay driver and selection of line detector.

The line status is selected by use of the C1 - C3 pins, Table 2, to determine the modes as listed. The function of these modes has already been described in the 'Overview' and 'DC Line Feed' sections; more detail of the device detectors is given on the following page (refer to Fig. 8).

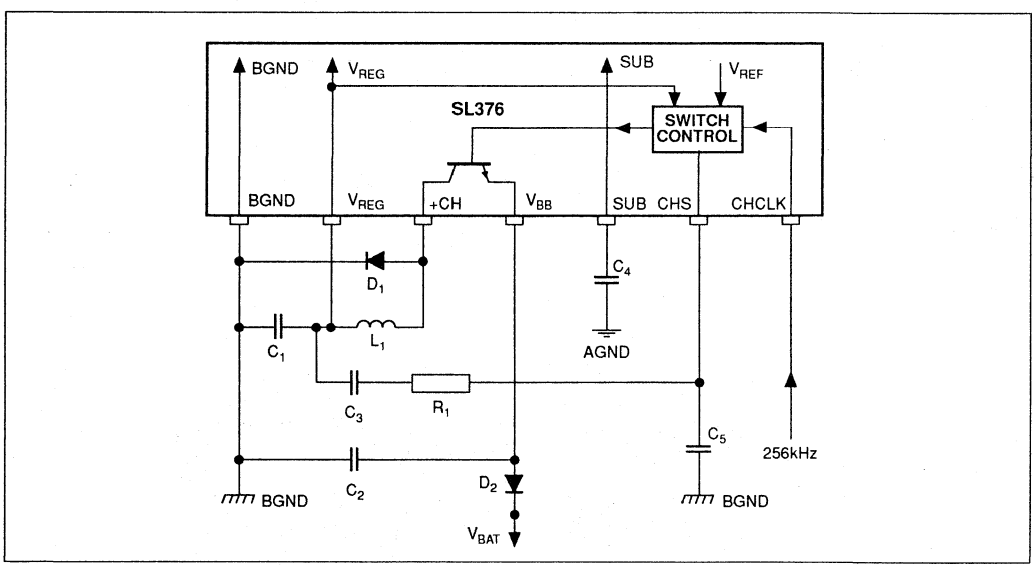


Figure 7: Voltage regulator power supply circuit

Loop Detect

This detector is used in Active and Disable modes (with/without polarity reversal). The loop current at which the detector indicates the Off-Hook condition, is set by the comparator at pins 24 (RD) and 20 (V_{EE}). Normally a resistor, R_{TH}, is connected between these pins, such that Off-Hook line current threshold (I_{DET})is set by:

$$I_{DET}=350 \div R_{TH}$$

This is due to the fact that the current out of the RD pin is equal to the loop current IL=($^1/_2|I_A-I_B|$) divided by ~280. This will create a voltage across R_{TH} at the RD pin. Off-Hook is given by a logic low at the $\overline{DET}$ output pin (when detector is selected) when this voltage rises above the internal 1.25V reference.

Ground Key Detector

This detector is selected by the E1 pin of the Digital Interface. It can be used in Active and Disable modes (with/without polarity reversal), as well as Disconnect A Disable B mode.

Operation of the detector is via an internal threshold and the longitudinal current $I_{LL}= I_A+I_B$ of the 2-wire loop. Ground Key detection is indicated when either the midpoint of the A and B legs is connected to ground, or the B leg (A leg, polarity reversed) is connected to ground. The resistance values for which Ground Key detection is valid are given in the Electrical Characteristics section.

Ring Trip Detector

This consists of a comparator connected to the DA and DB pins, and indicates Ring Trip when the voltage at DA < DB. Selection of Ringing mode operates the Ring Relay and enables the Ring Trip Detector. The external ringing supply must consist of DC line feed in addition to the AC ringing voltage. In order that the Ring Trip Detector senses Ring Trip in ringing mode, a resistance bridge network is used in association with pins DA, DB, line and ring source. This network is described in the Applications section and discussed further in AN82.

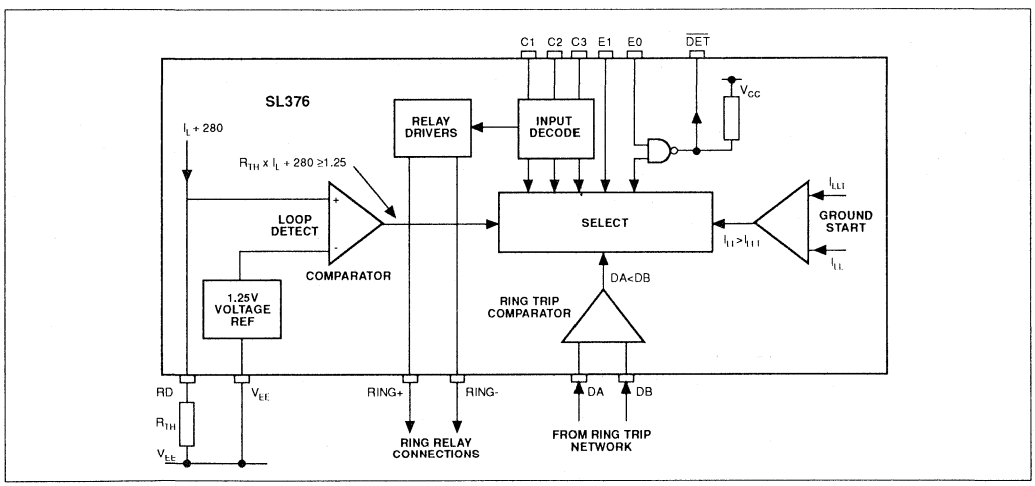


Figure 8: Detector circuits

FUNCTIONAL PARAMETER SUMMARY

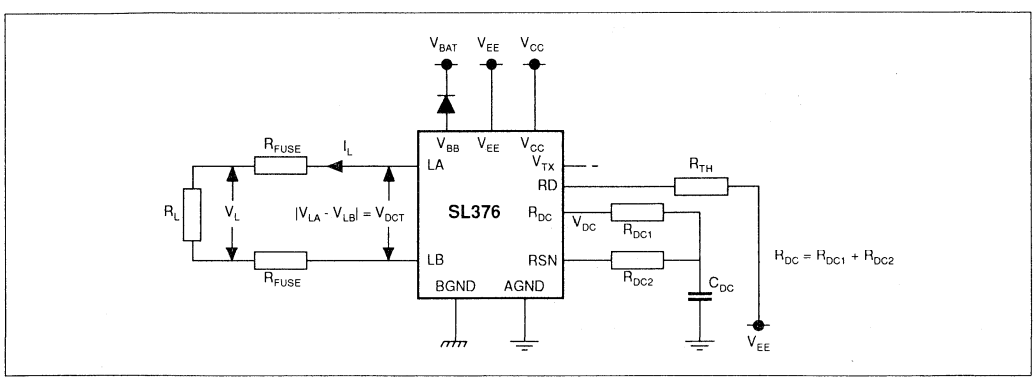


Figure 9: DC parameters and components for the SL376

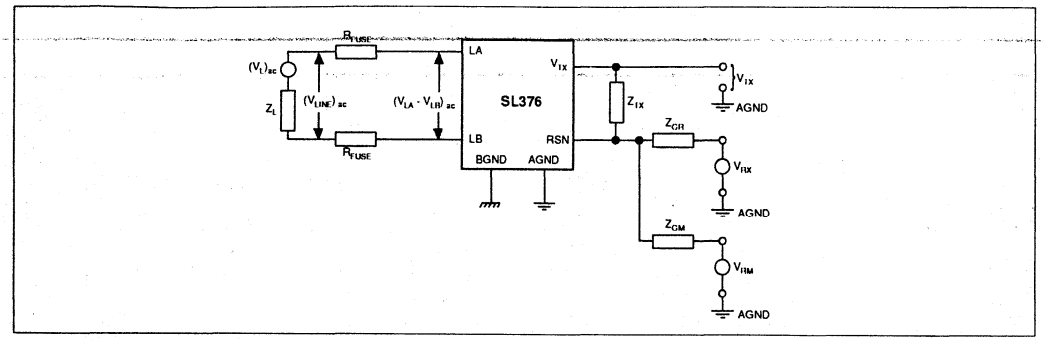


Figure 10: AC parameters and components for the SL376

LIST OF DEFINITIONS

1. Loop Current is defined as :- $I_L = \pm{}^1/_2|I_A-I_B|$

   I_A = current out of LA pin, I_B = current out of LB pin, + ⇒ normal line polarity and - ⇒ reverse line polarity.

2. Longitudinal Current is defined as :- ILL = $(I_A + I_B)$

   I_A = current out of LA pin, I_B = current out of LB pin.

3. Normal Line Feed Region when $|V_{BAT}|-|V_{DCT}| > V_{SG}$ which gives $I_L = I_{FEED} = 50 \div (R_L \div R_{FEEDTOT})$
   where $R_{FEEDTOT} = 2R_{FUSE} + (R_{DC} \div 50)$

4. Saturation Guard Threshold when $|V_{BAT}|-|V_{DCT}| = V_{SG} = 16.5V$ such that :-

   $I_L = I_{LSG} = 50\ (50+V_{SG}-|V_{BAT}|) \div (R_{DC})$ and
   $R_{LSG} = \dfrac{[(|V_{BAT}|-V_{SG}) \times (R_{DC})]-[2R_{FUSE}]}{(50 + V_{SG}-|V_{BAT}|)50}$ $V_{LSG} = I_{LSG} \times R_{LSG}$ which will equal $|V_{BAT}|-V_{SG}$ with $2R_{FUSE} = 0$

5. Saturation Guard feed Region when $|V_{BAT}|-|V_{DCT}| < V_{SG}$ with $I_L = [|V_{BAT}|-V_{SG}] \div [R_L + 2R_{FUSE}]$

6. Note that V_{LSG} is referred to as the value of the line voltage, V_L, at the point where Saturation Guard becomes active. This will differ from the value of $|V_{LA}-V_{LB}|$ (i.e. V_{DCT}) if $2R_{FUSE} \neq 0$. V_{SG} is used as a notional threshold voltage which is the internal headroom between the $|V_{LA}-V_{LB}|$ voltage and the battery supply, at this same point.

7. Open Circuit Line Voltage V_{LOC} at $R_L=\infty\Omega$ such that :- $V_L=V_{LOC} \approx [|V_{BAT}|-V_{SG}]$

   V_{LOC} will be $\geq V_{LSG}$ even with $2R_{FUSE}=0$. The voltage drop from V_{LOC} to the defined V_{LSG} point will be greater at lower values of V_{BAT}

8. Disable Mode DC Feed Current $I_L \leq I_{LIM} = K_{LIM} \times I_{DET} \approx 600 \div R_{TH}$

9. 2 Wire Termination Impedance $Z_{AB} = (Z_{TX} \div {}^1/_2\alpha) = (Z_{TX} \div 500)$

   Note that Z_{TX} is normally set to $[{}^1/_2\alpha(Z_L \div 2R_{FUSE})]$ where Z_L is the desired termination impedance.

10. Receive Gain from V_{RX} to $(V_{LA}-V_{LB})_{ac}$ or $(V_{LINE})_{ac}$ is set by Z_{GR} after setting Z_{TX}. Thus, with $(V_L)_{ac} = 0$:-

$$\frac{(V_{LA} - V_{LB})_{ac}}{V_{RX}} = \frac{-2\alpha Z_L Z_{TX}}{[\alpha(Z_L) + 2Z_{TX}]Z_{GR}} \text{ with } 2R_{FUSE} = 0; \quad \frac{(V_{LINE})_{ac}}{V_{RX}} = \frac{-2\alpha Z_L Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + 2Z_{TX}]Z_{GR}} \text{ with } 2R_{FUSE} \neq 0$$

11. Resultant Transmit Gain is then :-

$$\frac{V_{TX}}{(V_L)_{ac}} = \frac{Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + 2Z_{TX}} \text{ with } V_{RX} = 0$$

12. Resultant 4 Wire-4 Wire Gain is then :-

$$\frac{V_{TX}}{V_{RX}} = \frac{-\alpha(Z_L + 2R_{FUSE}) + Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + 2Z_{TX}]Z_{GR}} \text{ with } (V_L)_{ac} = 0$$

13. Metering Gain is determined by Z_{GM} in association with Z_{TX}, thus for the receive direction:-

$$\frac{(V_{LA} - V_{LB})_{ac}}{V_{RM}} = \frac{-2\alpha Z_L Z_{TX}(0.66)}{[\alpha(Z_L) + 2Z_{TX}]Z_{GM}} \text{ with } 2R_{FUSE} = 0; \quad \frac{(V_{LINE})_{ac}}{V_{RM}} = \frac{-2\alpha Z_L Z_{TX}(0.66)}{[\alpha(Z_L + 2R_{FUSE}) + 2Z_{TX}]Z_{GM}} \text{ with } 2R_{FUSE} \neq 0$$

and for the 4 wire to wire path:-

$$\frac{V_{TX}}{V_{RM}} = \frac{-\alpha(Z_L + 2R_{FUSE}) + Z_{TX}(0.66)}{[\alpha(Z_L + 2R_{FUSE}) + 2Z_{TX}]Z_{GM}} \text{ with } (V_L)_{ac} = 0$$

Note that the figure of 0.66 is due to the device intrinsic gain at metering frequencies (12kHz - 16kHz) and it will vary from this figure depending on PCB layout.

14. Off-Hook Threshold is set by R_{TH} at :- $I_L = I_{DET} = 350 \div R_{TH}$.

15. Ring Trip Threshold is set by the bridge associated with pins 25 .. 28 and the 2 Wire Line, thus :-

$R_L = R_{LTH} = R_{B4}(2R_F) \div (R_{B4}\text{-}R_{B1})$ assuming $R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$ and $R_{FEED1} = R_{FEED2}$ for the bridge components (balanced ringing). R_{B1}.....$R_{B4} \approx$ a few 100KΩ and $R_{FEED1} \approx$ a few 100Ω .

16. AC ringing voltage at DA (DB by the same amount) is reduced by a factor of :- $[1 + (2\pi f_r t_r)^2]^{1}/_{2}$

f_r is the ringing frequency and t_r is determined by the bridge components including C_B, thus :- $t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$ for balanced ringing.

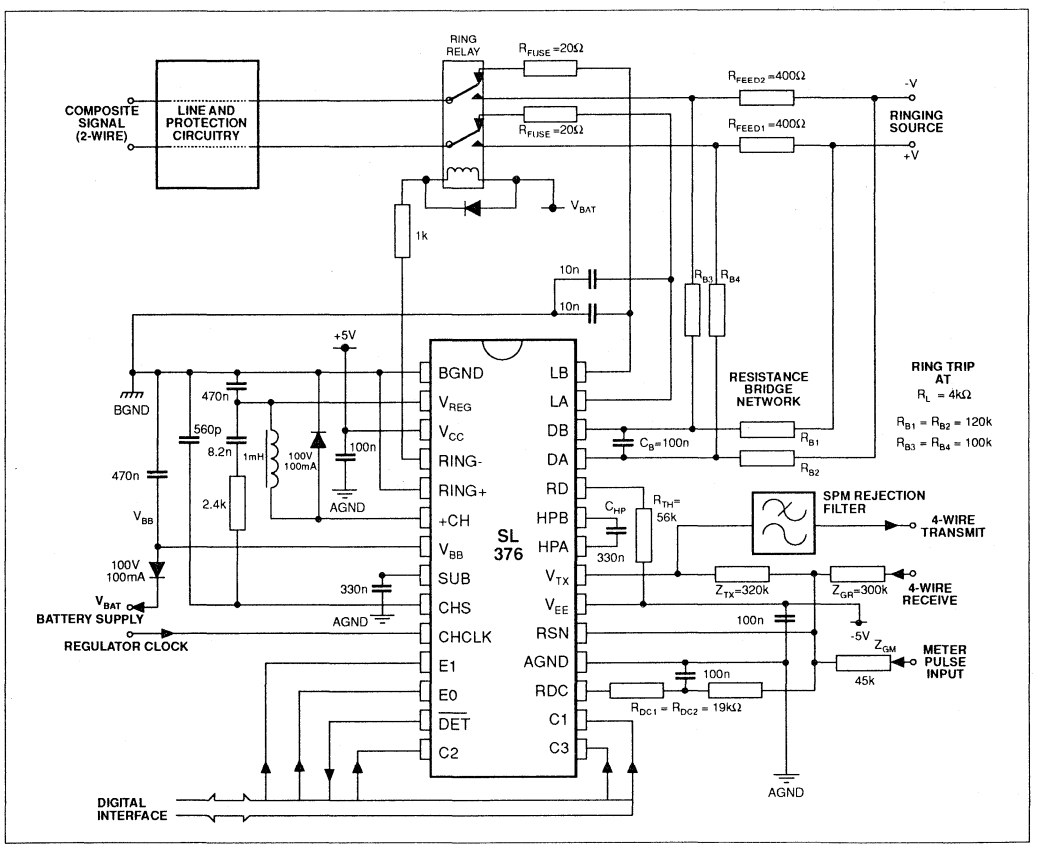


Figure 11: Application circuit

APPLICATIONS

The requirements for the subscriber line interface vary considerably from one telephone administration to another. The SL376 is designed to have the flexibility to meet these varying requirements. For simplicity, only a single example is given to illustrate how the device is connected. Fig. 11 shows the circuit which can be used to evaluate the device. Further Applications information is given in AN82-2 SLIC Applications Note.

The DA and DB pins are connected to a resistance bridge network (R_{B1} to R_{B4}) This allows the change in line resistance to be sensed when the remote telephone goes off-hook during ringing (Ring Trip). The details of this network (and C_B) are given later (see Ring Trip section). The resistors R_{FEED1} and R_{FEED2} provide feeding of the ringing source onto the line during ringing mode. The Ring Relay Driver is shown connected through a current limiting resistor.

Connections to the LA and LB pins are shown, and include the resistors R_{FUSE} in addition to the ring relay. These resistors have a value around 20 to 30 ohms, depending on the application, and provide current line protection.

Overvoltage and protection circuitry may consist of slew-limiting inductors between the pins and the line itself and a thyristor or zener protection network at the line. In many applications, especially in PBXs, the amount of protection circuitry can be reduced. The capacitors between LA, LB and ground, allow noise from the regulator to be decoupled.

The capacitor C_{HP} between HPA and HPB (pins 22 and 23) is used to filter out the AC component of the signal on the line. The voltage difference between the two pins should be effectively DC. Application Note AN82 contains a further discussion on this component.

The resistor, R_{TH}, between RD (pin 24) and V_{EE} (pin 20) programs the threshold current for the loop detector. A capacitor in parallel can be added to reduce the effect of the AC component of the line current, but this can cause instability in standby operation with highly inductive lines if it is too large.

The value of R_{TH} sets the current I_{DET} according to the relationship:

$$I_{DET} = 350 \div R_{TH}$$

The CHS pin (pin 9) is connected to BGND through a capacitor and to V_{REG} by a capacitor and resistor in series. This stabilises the regulator control loop. Operation of the regulator has been described earlier in the Functional Description section (pins 2,6 & 7).

It is recommended that the substrate (SUB) pin be decoupled to AGND. However, BGND may be used if this is sufficiently quiet, otherwise some degradation in noise performance may be experienced.

DC current flows between the RDC (pin 17) and RSN (pin 19). This is used to set the line feed current. Any minor AC fluctuations are reduced by dividing the resistance RDC equally such that $R_{DC1} = R_{DC2} = {}^1/_2 R_{DC}$ and connecting a capacitor from the junction of R_{DC1} and R_{DC2} to AGND.

The network (Z_{TX}) between V_{TX} and RSN controls the 2 wire terminating impedance (Z_T) This can also be a complex impedance. The value of Z_{TX} can be calculated from the relationship :-

$$Z_{TX} = (\text{Required } Z_T) \times (\text{Receive Current Gain}) \times {}^1/_2$$

The Receive Gain is set by the network (Z_{GR}) which controls the receive current flowing into RSN. This can be a complex impedance network to allow for complex impedance terminations. Note that Meter Pulse Injection is achieved in the same way as for receive gain, but set by the network value Z_{GM} and taking into account an additional factor of 0.66. More details of these gain settings are given in AN82.

Control and status pins are TTL compatible. They are designed to give a simple interface to digital circuits and are directly compatible with the MV3010-1 SLAC.

RING TRIP

Ring Trip detection operates by comparing the voltages on DA and DB and providing the output on $\overline{DET}$ when this function is enabled by the status input pins of the Digital Interface. A resistance bridge (R_{B1} to R_{B4}) must be connected to the line and the ringing voltage source to cause the differential voltage between DA and DB to change sign when the line resistance falls below the level associated with Ring Trip. Note that it is simplified by use of $R_{B1} = R_{B2}$ and $R_{B3} = R_{B4}$ (see discussion in AN82).

Ringing voltage is normally applied to the line through the Ring Relay which is activated by RING + and RING- (see Ring Relay Driver). The ringing voltage sources, including line feed, are connected to the line via Ringing-feed resistors, R_{FEED1} and R_{FEED2}. The resistance bridge operates by allowing the DC voltage dropped across the Ringing-feed resistors in the Off-Hook condition to reverse the polarity of the voltage on DA and DB (DA < DB). Since the AC ringing voltage is greater than the DC feed, the capacitor C_B (Fig. 12) will filter this out at the comparator inputs. The connection shown is suitable for

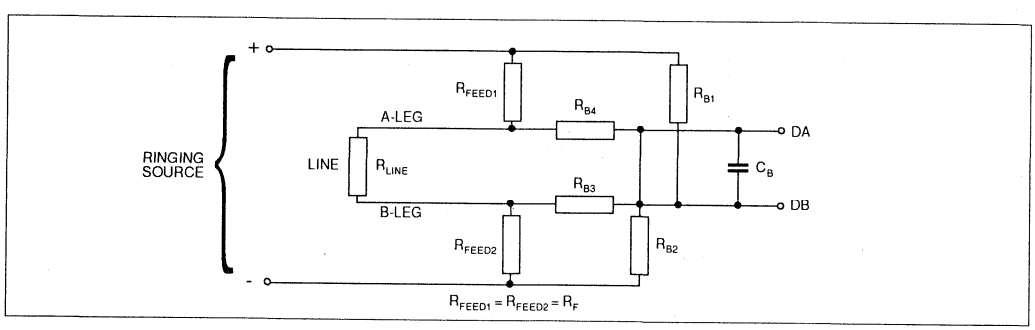


Figure 12: Ring trip circuit (balanced ringing)

balanced ringing only. For unbalanced ringing, separate capacitors from DA (C_{B1}) and DB (C_{B2}) to ground will be required to achieve the same result.

Fig. 12 shows how the resistance bridge is connected when used with balanced ringing. The circuit can operate correctly provided there is a DC feed in addition to the AC ringing voltage.

If R_{LTH} is the line resistance corresponding to the Ring Trip threshold (DA= DB), this can be determined frorn the values of RF ($R_{FEED1} = R_{FEED2} = R_F$). R_{B1} and R_{B4} ($R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$) as:-

$$R_{LTH} = \frac{RB_4(2R_F)}{(R_{B1} - R_{B4})}$$

R_{B1} and R_{B4} should be a few hundred kΩ.

The amplitude of the AC ringing voltage at DA (DB by the same amount) is reduced by a factor of $[1 + (2\pi f_r t_r)^2]^{-1/2}$ where f_r is the ringing AC frequency and t_r is set by:-

$$t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$$

for balanced ringing. For f_r = 20Hz, t_r should be = 50ms. For unbalanced ringing C_B will become $C_{B1}C_{B2} \div (C_{B1} + C_{B2})$ in the above equation. More detail on Balanced and Unbalanced ringing is given in AN82.

RING RELAY DRIVER

It is possible to drive the Ring Relay from the SL376 in one of two ways, as shown in Figs. 13a and 13b. Note that RING- is clamped from going below the substrate, and that V+ may be +30V (max.) if V_{BAT} = -50V. (Absolute Maximum Voltage, RING+ to V_{BAT} = 80V).

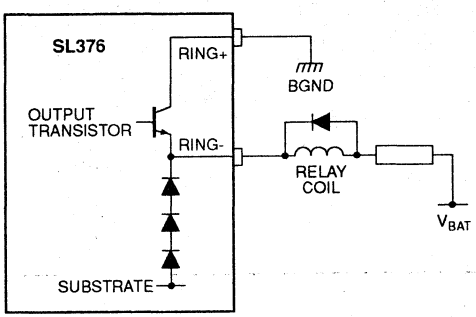


Figure 13a: Negative supply

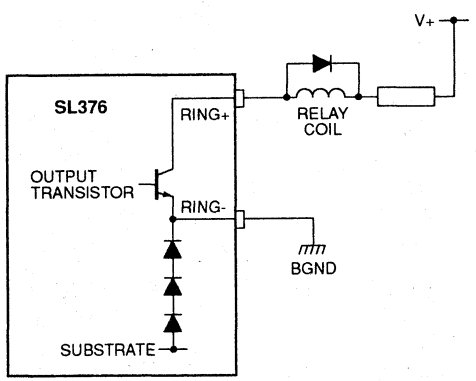


Figure 13b: Positive supply

Figure 13: Alternative relay drive configurations

PIN DESCRIPTIONS

Symbol	Pin no	Pin name and description
BGND	1	**Battery Ground (Power Input).** 0 Volts.
V_{REG}	2	**Regulated Voltage (Negative Power Input).** The voltage at this pin is compared to that required for line feed, and the result is used to control the voltage regulator.
V_{CC}	3	**Positive Supply (Power Input).** + 5 Volts.
RING-	4	**Ring Relay Driver Output, Transistor Emitter.** This output is designed to drive a relay, when used together with the RING+
RING+	5	**Ring Relay Driver Output, Transistor Collector**. This output is designed to drive a ring relay, when used together with RING-.
+CH	6	**Switching Regulator (Chopper) Output (Negative Power Output).** Chopper switch transistor collector. An internal regulator controls the mark/space ratio of the switching waveform to maintain V_{REG} (pin 2) at the required voltage.
V_{BB}	7	**Battery Voltage (Negative Power Input).** This is the battery supply pin which connects to the V_{BAT} supply via an external diode, to the chopper switch emitter, and via an on-chip resistor to SUB.
SUB	8	**Substrate (Decoupling Node).** An external decoupling capacitor (0.33µF) should be connected between this pin and AGND.
CHS	9	**Line Feed Regulator (Chopper) Stabilising Network.** This is the input to the voltage comparator which is used to control the switching regulator.
CHCLK	10	**Line Feed Regulator (Chopper) Clock (Digtal Input).** This is the positive edge triggered, 256kHz clock input for the voltage regulator, which will free run in the absence of an input signal.
E1	11	**Detector Select (Digital Input).** Selects the line status detector (Loop or Ground Key).
E0	12	**Detector Data output Enable (Digital Input).** Enables the Detector data output ($\overline{DET}$).
$\overline{DET}$	13	**Detector Data output (Digital Output).** This pin outputs the status of the detector which has been selected by D0 - D2 and E1. It is enabled by the E0 pin.
C2 C3 C1	14 15 16	**Control Input (Digital Input).** **Control Input (Digital Input).** **Control Input (Digital Input).**	These inputs determine the MSLIC operating mode, and control the ring relay, selection of ringing and non-ringing Modes, line polarity, line status and line detector.
R_{DC}	17	**DC Reference Voltage (Voltage Output).** A reference voltage of ± (50-$\|V_{LA}$-$V_{LA}\|$) ÷20 Volts depending on line polarity), is output at this pin, excepting Saturation Guard operation.
AGND	18	**Analog Ground (Analog Reference Node).** This is the ground reference pin for the analog signals. It also provides a ground reference for the Digital Interface. Signal reference and decoupling connections should be separately run to this pin.
RSN	19	**Receive Summing Node (Current Input).** The current which is input on this pin is used to control the transverse current at LA and LB.

V_{EE}	20	**Negative Supply (Power Input).** - 5 Volts.
V_{TX}	21	**Transmit Voltage (Voltage Output).** The voltage output at this pin is equal to the difference between the voltage (V_{LA}-V_{LB}) and the differential DC voltage (V_{HPA}-V_{HPB}), multiplied by the 2 to 4-wire voltage gain.
HPA HPB	22 23	**High Pass A, High Pass B - AC/DC separation (Voltage Inputs).** These inputs sense the DC feed voltages on the LA and LB pins respectively. Under normal operation they are connected to LA and LB respectively by internal resistors and should be connected as shown in Fig. 11.
RD	24	**Loop Detection Control (Current Output / Voltage Input).** This pin outputs a current which equals the transverse loop current through LA and LB divided by 280. Off-Hook is indicated via the DET pin when the voltage at this pin is 2 (V_{EE} + 1.25) Volts.
DA DB	25 26	**Ring Trip Detector A, Ring Trip Detector B (Voltage Inputs).** These are the A and B inputs to the internal ring trip comparator. The output of the comparator controls the ring trip output on $\overline{DET}$.
LA LB	27 28	**A Line Transceiver, B Line Transceiver (Current Outputs / Voltage Inputs).** These two pins form the 2-wire port connecting to the subscriber loop.

ELECTRICAL CHARACTERISTICS

Operating Range

V_{CC} = + 5.0V ± 5%, V_{EE} =-5.0V ± 5%, V_{BAT} =-40.5V to 64.0V (typical -50V). V_{BGND} = -0.1V to +0.1V, V_{IH} = 2.0V, V_{IL} = 0.7V, Z_L = ∞Ω. Voltages measured with respect to analog ground (V_{AGND}). Temperature T_{amb} = 0°C to +70°C.

Test Levels

1. Tested over full operating range.
2. Tested at 25°C but guaranteed over the full operating range.
3. Not tested, but guaranteed by characterisation.

Supply Characteristics

Characteristic	Symbol	Value			Units	Conditions	Test Level
		Min.	Typ.	Max.			
Positive supply (V_{CC}) current, Disconnect mode	I_{CC1}			4	mA		2
Positive supply (V_{CC}) current, Disable mode	I_{CC2}			10	mA	On / Off-Hook, I_L = 0	2
Positive supply (V_{CC}) current. Active mode	I_{CC3}			10	mA	On / Off-Hook, I_L = 0	2
Negative supply (V_{EE}) current, Disconnect mode	I_{EE1}			2	mA		2
Negative supply (V_{EE}) current Disable mode	I_{EE2}			3	mA	On / Off-Hook, I_L = 0	2
Negative supply (V_{EE}) current Active mode	I_{EE3}			3	mA	On / Off-Hook, I_L = 0	2
Battery supply (V_{BB}) current Disconnect mode	I_{BB1}			1	mA		2
Battery supply (V_{BB}) current Disable mode	I_{BB2}			5	mA	On-Hook, I_L = 0	2
Battery supply (V_{BB}) current Active mode	I_{BB3}			6	mA	On-Hook, I_L = 0	2

Supply Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions	Test Level
		Min.	Typ.	Max.			
Positive supply (V_{CC}) rejection ratio (supply to 2-wire transverse)	P_{SRT}	20			dB	50mV on V_{CC} supply, 300-3400Hz, R_L = 600Ω	2 Note 3
Positive supply (V_{CC}) rejection ratio (supply to 2-wire longitudinal)	P_{SRL}	17			dB	50mV on V_{CC} supply, 300-3400Hz, R_L = 600Ω	2 Note 3
Negative supply (V_{EE}) rejection ratio (supply to 2-wire transverse)	N_{SRT}	20			dB	50mV on V_{EE} supply, 300-3400Hz, R_L = 600Ω	2 Note 3
Negative supply (V_{EE}) rejection ratio (supply to 2-wire longitudinal)	N_{SRH}	20			dB	50mV on V_{EE} supply, 300-3400Hz, R_L = 600Ω	2 Note 3
Battery supply (V_{BB}) rejection ratio (supply to 2-wire transverse)	B_{SRT}	20			dB	50mV on V_{BAT} supply. 300-3400Hz, R_L = 600Ω	2 Note 3
Battery supply (V_{BB}) rejection ratio (supply to 2-wire longitudinal)	B_{SRL}	25			dB	50mV on V_{BAT} supply. 300-3400Hz, R_L = 600Ω	2 Note 3
Power dissipation, Active state	P_{WA1}			1.1	W	Z_L = 600Ω	2
Power dissipation, Active state	P_{WA2}			1.5	W	Z_L = 0- ∞Ω	2
Power dissipation, Disable state on hook	P_{WD1}			0.3	W		2
Power dissipation, Disable state off hook	P_{WD2}			1.5	W	See note 1	2

NOTE
1. Because the regulator is inhibited, only short term operation is envisaged in Disable mode, off-hook.
2. Battery voltage V_{BAT} is generally defined. The corresponding V_{BB} voltage is assumed to be 0.7V more positive than V_{BAT} allowing for the diode drop in D2, Fig. 7.
3. Tested at 1KHz.

ANALOG CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions	Test Level
		Min.	Typ.	Max.			
2-wire port, low freq overload level	V_{OAB}	- 6.0		+ 6.0	Volts (pk)	See Fig 14, note 4: E_R = 1000Hz, E_L = 0V,	3
2-wire port, longitudinal impedance, off hook	Z_{LL1}			35	Ω/wire	See Fig 15: f<100Hz Z_L = 600Ω	2
2-wire port, longitudinal impedance, on hook	Z_{LL2}			35	Ω/wire	See Fig 16: f < 100Hz Z_L = 600Ω	2
Longitudinal current limit, Active state	ILL_A	17.5			mA/wire (rms)	See Fig 17, note 5: E_R=- 10dBm 700-1100Hz	3
Longitudinal current limit, Disable state	ILL_S	8.0			mA/wire (rms)	See Fig 17, note 5: E_R=- 10dBm 700-1100Hz	3
4-wire transmit port, overload level	V_{OT}	- 3.1		+ 3.1	V (pk)	See Fig 14, note 4: f = 1000Hz 4-Wire Load ≥25kΩ, E_R=0V,	2
4-wire transmit port, offset voltage	V_{TOFF}	- 15		+ 15	mV	See Fig 14: E_R =0	2

ANALOG CHARACTERISTICS (continued)

Characteristic	Symbol	Value			Units	Conditions	Test Level
		Min.	Typ.	Max.			
4-wire transmit port,output impedance	Z_T			10	Ω	See Fig 14: E_R= 0	3
Transmit (2 to 4-wire) voltage gain	G_T	- 6.03		-5.73	dB	See Fig 14: E_R = 0, E_L = 0dBu Note 4, 1kHz	2
4-wire receive port, low impedance virtual earth input	Z_{RI}			20	Ω	Note 6	3
4-wire receive port, low frequency voltage gain	G_{RL4}	-0.15		+0.15	dB	See Fig 18: E_R=2.6dBu 1kHz	2
4-wire receive port, high freq voltage gain (open loop)	G_{RH4}	G_{RH} -0.6		G_{RH} +0.6	dB	See Fig 18, note 7: ER = 2.6dBu 15000Hz	2
4-wire receive port, current gain	G_{RI4}	59.8	60.0	60.2	dB	See Fig 14:	3
4 to 4-wire voltage gain	G_R x G_T	-6.08		-5.68	dB		2
2-wire to 4-wire frequency response	F_{24}	- 0.1		+ 0.1	dB	See Fig 14, note 8: E_R = 0, E_L = 0dBu 200-3400 Hz,	2
4-wire to 2-wire frequency response	F_{42}	- 0.1		+0.1	dB	See Fig 14, note 8: E_L=0, E_R=0dBu 200-3400 Hz,	2
4 to 4-wire frequency response	F_{44} = F_{24} x F_{42}	- 0.1		+ 0.1	dB	Note 8	2
Gain linearity, 2-wire to 4-wire	G_{L24}	-0.05		+0.05	dB	See Fig 14, note 9: E_R = 0V, E_L = +7 to -59dBu 1 kHz	3
Gain linearity, 4-wire to 2-wire	G_{L42}	- 0.05		+0.05	dB	See Fig 14, note 9: E_L = 0, E_R = + 3dBu to -64dBu 1 kHz	3
4-wire idle channel noise (psophometric weighted)	N_{P4}			-80.0	dBup	See Fig. 14: V_{BAT} = -48V, E_L = V_R = 0V	2
2-wire idle channel noise (psophometric weighted)	N_{P2}			-75.0	dBup	See Fig. 14: V_{BAT} = -48V, E_L = V_R = 0V	2

NOTES
4. Overload occurs when distortion is 1% of total signal in the range 300-3400Hz.
5. E_{LL} = 50Hz. Amplitude is increased until signal-to-distortion ratio at $V_T \leq$ 20dB.
6. dBu is defined thus: 0dBu is equivalent to the voltage at 0dBm when loaded with 600Ω (= 0.775V_{RMS}).
7. Very dependent on board layout. $G_{RH} \approx$ -3.6dBu.
8. Response is measured with respect to 1 kHz.
9. Linearity is measured with respect to gain at 0dBu.

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions	Test Level
		Min.	Typ.	Max.			
2-wire differential noise (wide band)	N_{D2}		Fig. 20			See Fig. 19	3
2-wire longitudinal noise (wide band)	N_{L2}		Fig. 21			See Fig. 19	3
Regulator noise, 4-wire transmit, single frequency	N_{R4}		- 55.0		dBu	See Fig. 19	3
Regulator noise, 2-wire transverse, single frequency	N_{RT}		- 50.0		dBu	See Fig. 19	3
Regulator noise, 2-wire longitudinal, single frequency	N_{RL}		- 50.0		dBu	See Fig. 19	3
Longitudinal balance, longitudinal to transverse	B_{L-T}	50			dB	See Fig. 15, Z_L = 600Ω, E_R = 0. E_{LL} = + 2dBu 40-4000 Hz	2
Longitudinal balance, trans-long + long-trans	B_{T-L} + B_{L-T}	98			dB	See Fig 15 & Fig 22: Z_L = 600Ω E_R = 0, E_{LL} = +2dBu 300 - 800Hz	2
Longitudinal signal rejection, longitudinal to 4-wire	RJ_{L-4}	50	60		dB	See Fig. 15: Z_L = 600Ω, E_R = 0. E_{LL} = + 2dBu 40-4000 Hz	2
Longitudinal signal generation, 4-wire to longitudinal	GN_{4-L}	40			dB	See Fig. 23: Z_L = 600Ω or 1.6kΩ E_R = 2.6dBu f = 300-800 Hz	2
Harmonic distortion, 4 to 2-wire	T_{HD1}			- 50.0	dB	E_R = 0dBu See Fig.14, note 10: 1 kHz	2
High frequency harmonic distortion, 4 to 2 wire, on-hook	T_{HD2}			- 35.0	dB	See Fig.24, note 11: V_{A-B} = 2.2Vrms, 16kHz	3
Intermodulation distortion	ID_{A-B1}			- 40.0	dB	See Fig . 14, note 12: $E_R = f_1 + f_2$, $f_1 = f_2$ = - 4 to - 21 dBu,	3
50Hz intermodulation distortion	ID_{A-B2}			- 49.0	dB	Note 6	3
Loop current, Active state,	I_{ACT1}	32.7		38.7	mA	See note 13: Z_L= 600Ω, See Fig. 27	2
Loop current, Active state	I_{ACT2}	14.5		19.7	mA	See note 13: Z_L = 1.84kΩ, See Fig. 27	2
2-wire current, Disconnected state	I_{DCT}			1.0	mA	LA to LB or ground, or both LA and LB to ground	2
Loop current, Disable state, normal (+) or reverse (-)	I_{LIM}	10.0		12.8	(±) mA	See note 14; Z_L = 600Ω See Fig. 27	2
Loop detector, current threshold	I_{TH}	I_{TH} - 20%	I_{TH}	I_{TH} + 20%	A	See Fig 27: $I_{TH} = 350 \div R_{TH}$	2

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions	Test Level
		Min.	Typ.	Max.			
Ring trip detector offset voltage	V_{RTO}	-50		+50.0	mV	See Fig. 25: $V_{BB} < V_{CMM} < -2V$	2
Ring trip detector bias current	I_{RTB}			1.0	µA	See Fig 25: $I_{RTB} = {}^1/_2(I_{RTDA} + I_{RTDB})$	2
Ground key Active state	R_{G1}	900		10	kΩ	See Fig. 26, notes 15 and 16: SW1 closed, RW = 300Ω	2
Ground key Active state	R_{G2}	1.7		10	kΩ	See Fig. 26, notes 15 and 16: SW1 open, RW = 0Ω	2
Earth call Disconnect A Disable B	R_{G3}	1.7		10	kΩ	See Fig. 26, note 16: SW1 open, RW=0Ω	2
Relay driver, saturation voltage (active)	V_{SAT}			1.8	V	I = 60mA drawn from external positive supply	2
Relay driver, leakage current (non-active)	I_{LK}			0.1	mA	RING- = 0V, RING+ = +6V	2
Relay driver, clamp voltage	V_{CL-}	V_{BAT} -3 0			V	I = 25mA from RING-	2

NOTES
10. Distortion measured in the bandwidth 300-3400 Hz.
11. Distortion measured in the bandwidth 20Hz-100kHz.
12. f_1 & f_2 in the range 300-3400Hz, $f_1 \div f_2$= Non-integer. Measure $(2f_1 - f_2)$ relative to f_1 or f_2 level.
13. Feed resistance is (40K ÷ 50)Ω ie R_{DC} = 40kΩ. Nominal apparent battery = -50V.
14. Constant current in Disable mode is approximately $(600 \div R_{TH})$mA.
15. For polarity reversed state, connections to LA and LB are reversed.
16. 'Must detect' and 'Must not detect' are indicated in the Min. and Max. columns respectively.

Digital Characteristics

Characteristic	Symbol	Value			Units	Conditions	Test Level
		Min.	Typ.	Max.			
Input low voltage (C1 - C3, E0, E1, CHCLK)	V_{IL}			0.8	V		2
Input high voltage (C1 - C3, E0, E1, CHCLK)	V_{IH}	2.0			V		2
Input low current (C1 - C3, E0, E1, CHCLK)	I_{IL}			- 0.25	mA	V_{IL} - 0.4V	2
Input high current (C1 - C3, E0, E1, CHCLK)	II_H			0.04	mA	V_{IH} = 2.4V	2
$\overline{DET}$ output low voltage	V_{OL}			0.4	V	I_{OL} = 0.8mA	2
$\overline{DET}$ output high voltage	V_{OH}	2.4			V	I_{OH} = 0.1mA	2
$\overline{DET}$ output, internal pull-up	R_{OUT}	10		20	kΩ		2
Propagation delay, E1 to $\overline{DET}$	t_{PD}			4	µs	$\overline{DET}$ 6.2kΩ to V_{CC} 15pF to BGND	2
Loop detector make response time	t_{LM}			3	ms	Z_L = 2kΩ	2
Loop Detector break response time	t_{LB}			3	ms	Z_L = 2kΩ	2
CHCLK input frequency	F_{CLK}		256		kHz		2
CHCLK min. pulse width	T_{CLK}		500		ns		2

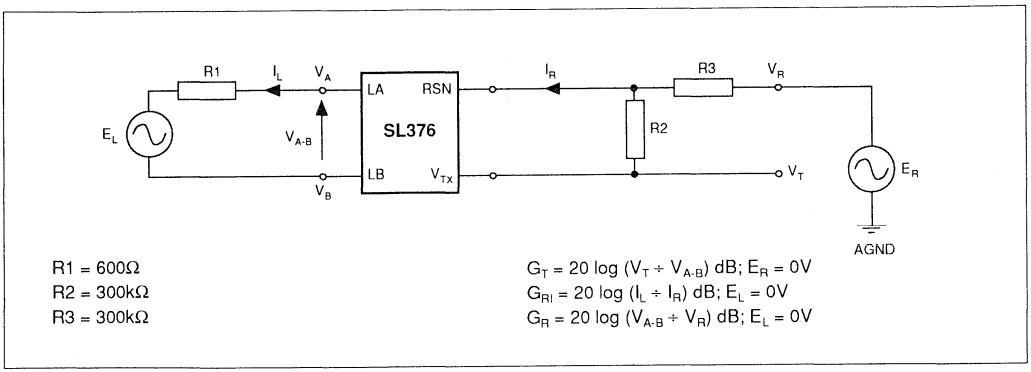


Figure 14: Test configuration (Note the SL376 block = Fig 27)

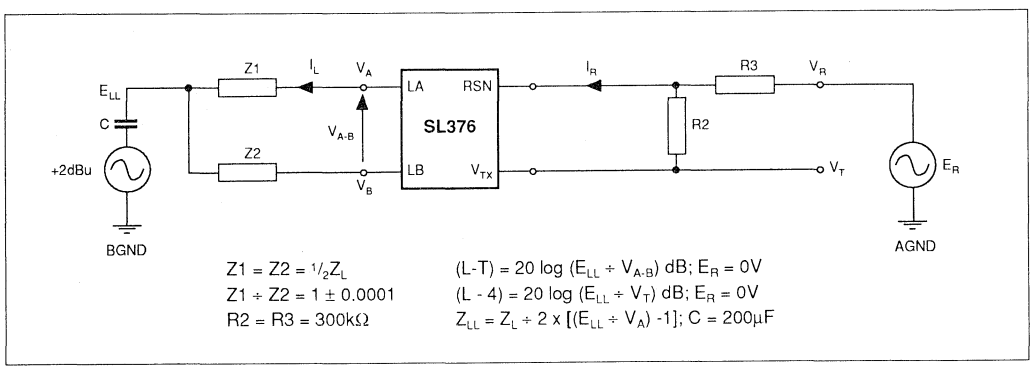


Figure 15: Test configuration (Note the SL376 block = Fig 27)

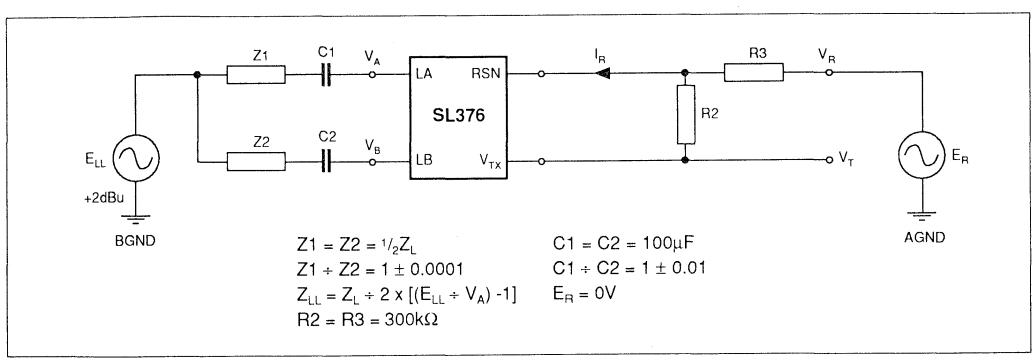


Figure 16: Test configuration (Note the SL376 block = Fig 27)

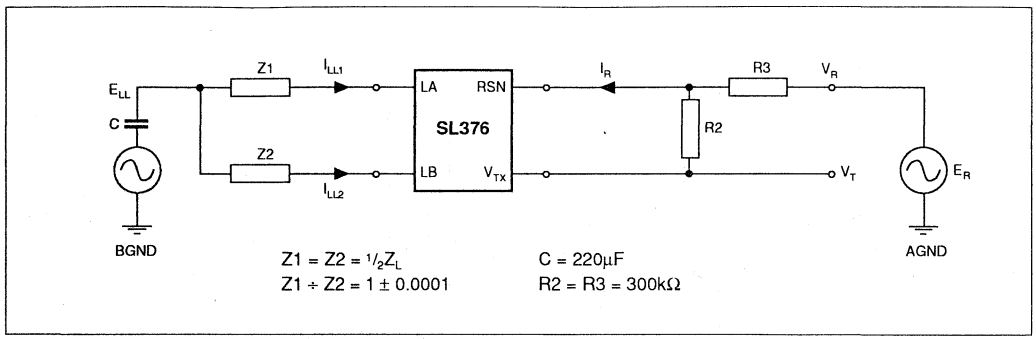


Figure 17: Test configuration (Note the SL376 block = Fig 27)

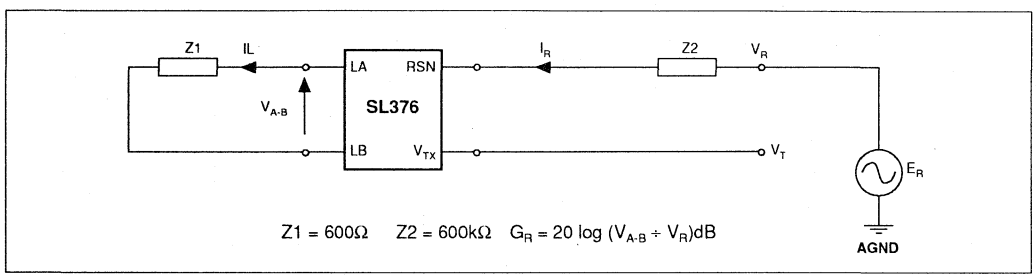


Figure 18: Test configuration (Note the SL376 block = Fig 27)

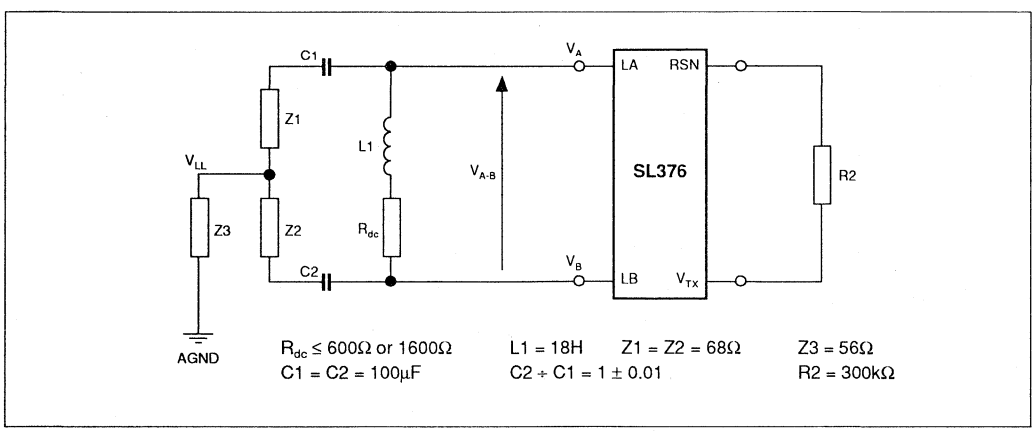
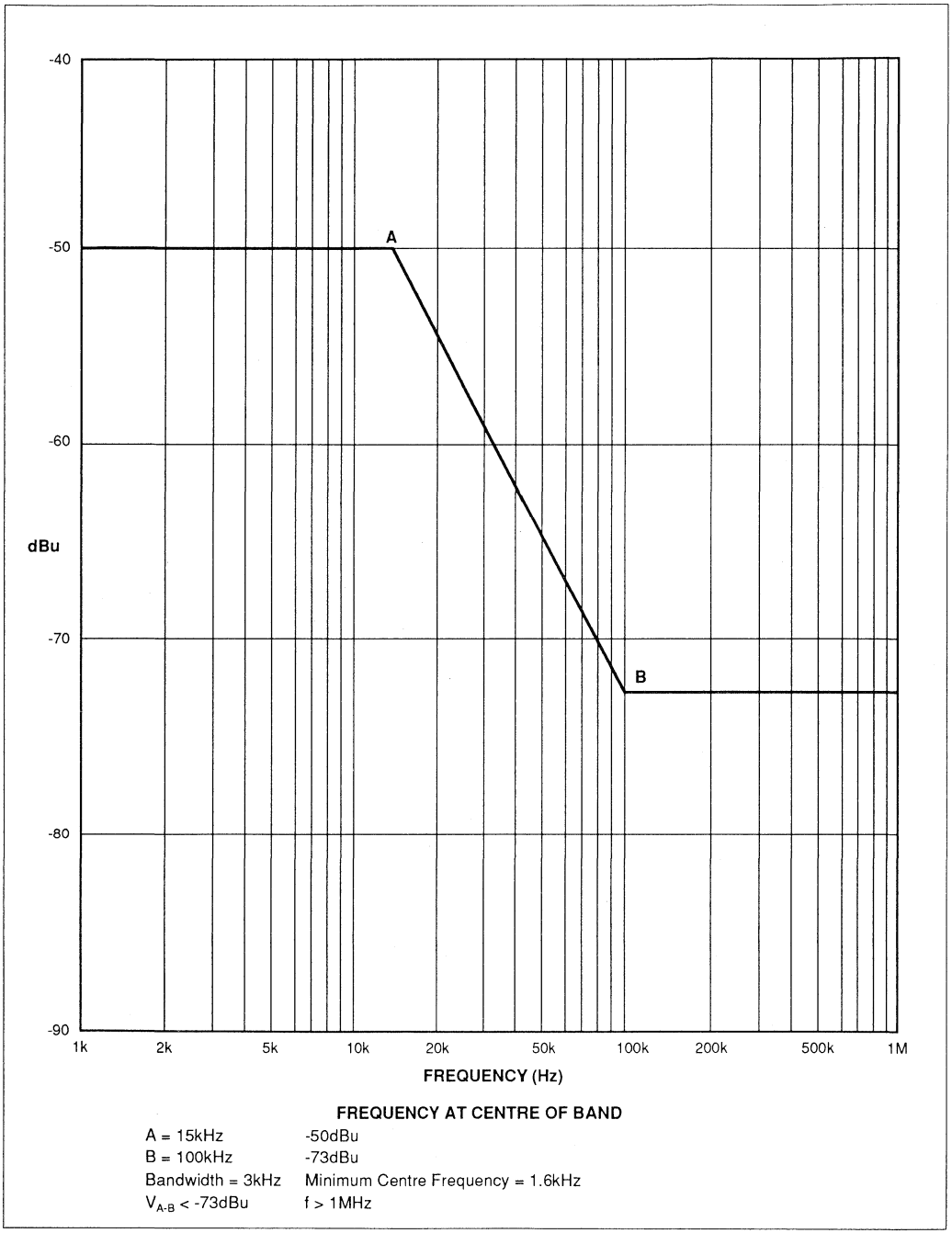


Figure 19: Test configuration (Note the SL376 block = Fig 27)



FREQUENCY AT CENTRE OF BAND

A = 15kHz	-50dBu
B = 100kHz	-73dBu
Bandwidth = 3kHz	Minimum Centre Frequency = 1.6kHz
V_{A-B} < -73dBu	f > 1MHz

Figure 20: 2-Wire differential noise

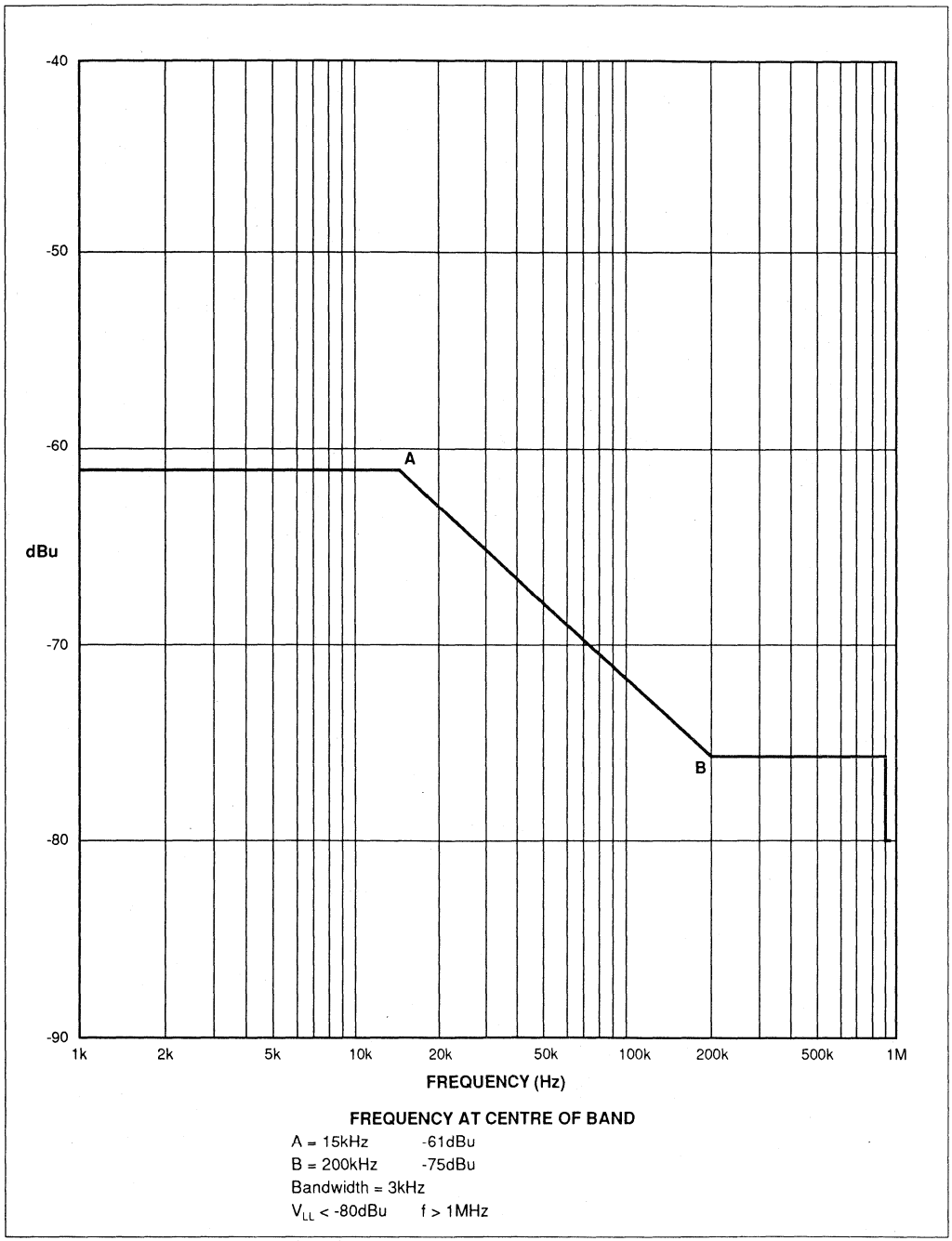


Figure 21: 2-Wire longitudinal noise

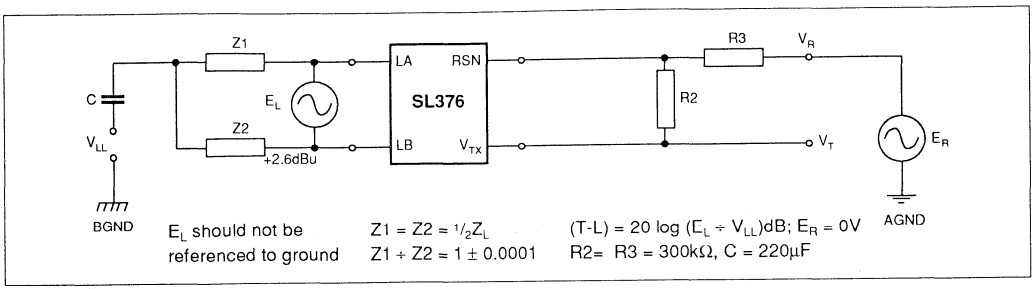


Figure 22: Test configuration (Note the SL376 block = Fig 27)

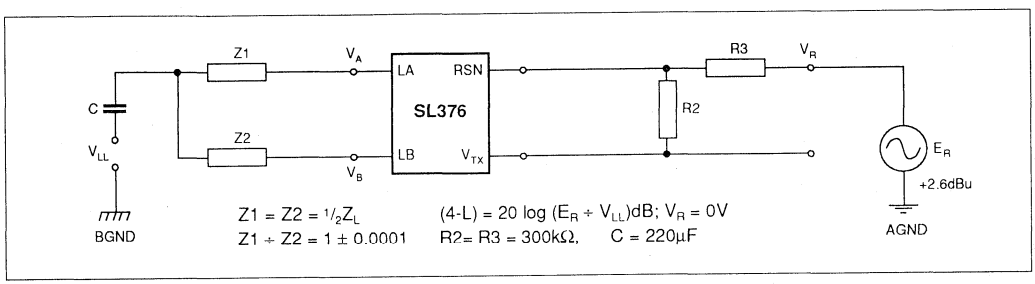


Figure 23: Test configuration (Note the SL376 block = Fig 27)

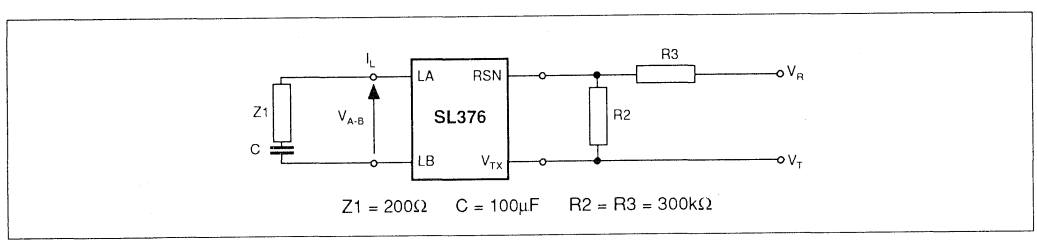


Figure 24: Test configuration (Note the SL376 block = Fig 27)

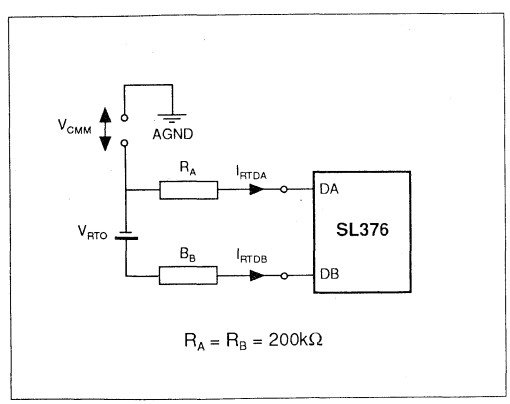


Figure 25: Test configuration (Note the SL376 block = Fig 27)

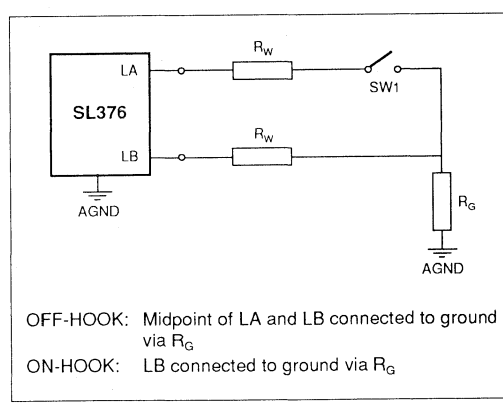
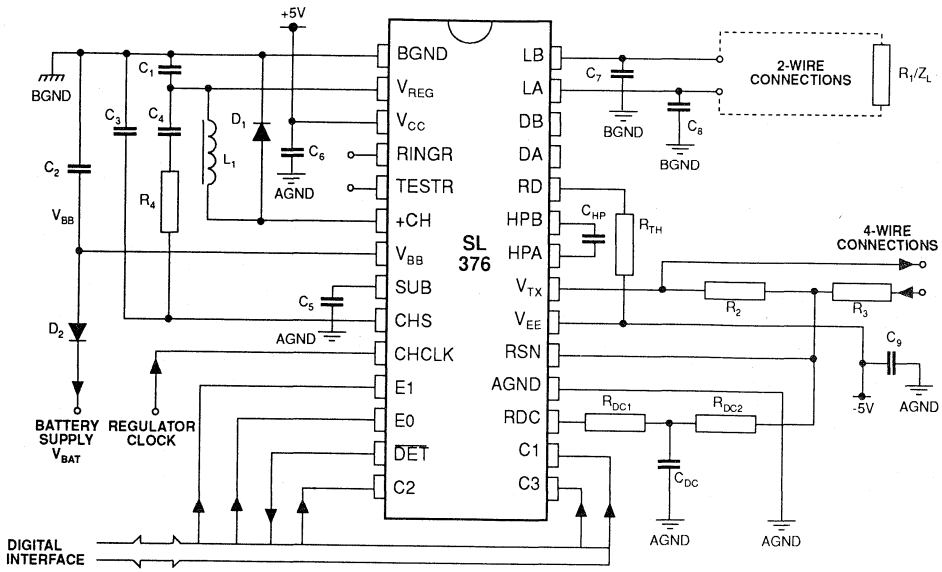


Figure 26: Test configuration (Note the SL376 block = Fig 27)



C_1 = 470n	C_6 = 100n	C_{DC} = 100n	R_{TH} = 56kΩ
C_2 = 470n	C_7 = 2.2n	D_1 = 100V, 100mA	$R_{DC1} = R_{DC2} = {}^1/_2R_{DC}$ = 20kΩ
C_3 = 560p	C_8 = 2.2n	D_2 = 100V, 100mA	R_2 as Test Configuration
C_4 = 8.2n	C_9 = 100n	L_1 = 1mH	R_3 as Test Configuration
C_5 = 330n	C_{HP} = 330n	R_4 = 2.4kΩ	Z_L: See Electrical Characteristics

For all tests assume AGND = BGND

Figure 27: Test circuit for Figures 14 - 19 and 22 - 26

ABSOLUTE MAXIMUM RATINGS* - Voltages are with respect to analog ground (V_{AGND}).

Parameter	Symbol	Value		Units
		Min.	Max.	
Battery supply voltage	V_{BB}	- 70	+ 1.0	V
Battery voltage, rate of change	V_{BBR}	- 0.4	+ 0.4	V/µs
Continuous battery ground voltage	V_{BGNDC}	- 2.0	+ 2.0	V
Intermittent (10µs) battery ground voltage	V_{BGNDI}	-4.0	+4.0	V
Positive supply voltage	V_{CC}	- 0.4	+ 7.0	V
Negative supply voltage	V_{EE}	- 7.0	+ 0.4	V
Subscriber line voltage on LA, LB or both, continuous	V_{LC}	- 75.0	+ 1.0	V
Subscriber line voltage on LA, LB or both, 10ms duration, f = 0.1 Hz rate	V_{LR1}	-70	+ 5.0	V
Subscriber line voltage on LA, LB or both, 1µs duration, f = 0.1 Hz rate	V_{LR2}	-90	+ 10.0	V
Subscriber line voltage on LA, LB or both, 250ns duration, f = 0.1 Hz rate	V_{LR3}	-120	+ 15.0	V
Switched regulator voltage (off)	V_{CH}	V_{BB}	+ 1.0	V
Switched regulator current (on)	I_{CH}		150	mA
RING+ to RING- relay driver voltage	V_{RING}		+70	V
RING to V_{BAT}	$V_{RINGVBAT}$	V_{BAT}	+80	V
Relay source current	I_{RING}		60	mA
Ring-Trip input voltage (DA or DB)	V_{RT}	V_{BB}	0	V
Ring-Trip input current (non repetitive 10ms pulse)	I_{RT}	-2.0	+ 2.0	mA
Digital input voltage	V_{ID}	- 0.4	V_{CC}	V
Digital input current (sink)	I_{ID}		- 5.0	mA
Digital output voltage	V_{OD}	-0.3	V_{CC}	V
Digital output current (source)	I_{OD}		3	mA
Storage temperature	T_{ST}	- 65	+ 150	°C
Operating junction temperature	T_{JOP}		+ 150	°C
Package power dissipation (DG28)	P_{PDG28}		1.5	W
Package power dissipation (LC28)	P_{PLC28}		1.2	W

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

SL377

SUBSCRIBER LINE INTERFACE CIRCUIT

The SL377 is a Subscriber Line Interface Circuit (SLIC) for use at the telephone exchange or PABX end of a telephone line.

It provides power feed, transmits and receives voice signals, controls ringing and detects Ground Key or Off-Hook conditions. These functions can be programmed to provide the flexibility required for different telephone networks.

The SL377 is fabricated using bipolar technology.

FEATURES

- Low Power Line Feed via Regulator
- Programmable Constant Current Feed Independent of Battery, to Line
- Programmable AC Termination Impedance
- Good Longitudinal Balance
- Ground Key and Ring Trip Detection
- Programmable Off-Hook Detection
- Disconnect and Low Power Disable Modes
- A-Leg Disconnect, B-Leg Disable Mode
- Normal or Reversed Line Polarity Operation
- Ring and Test Relay Drivers
- Thermal Shut-Down Protection

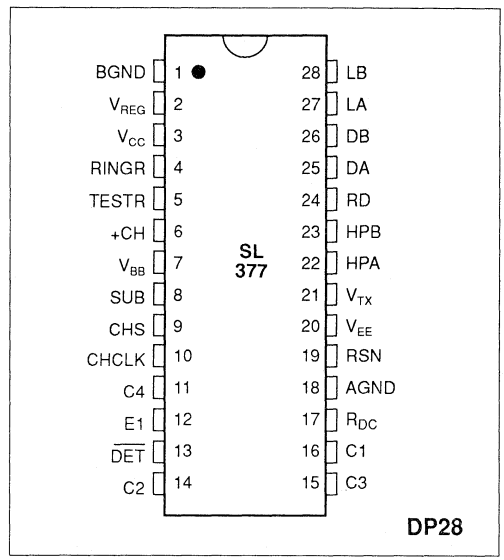


Figure 1: Pin connections - top view

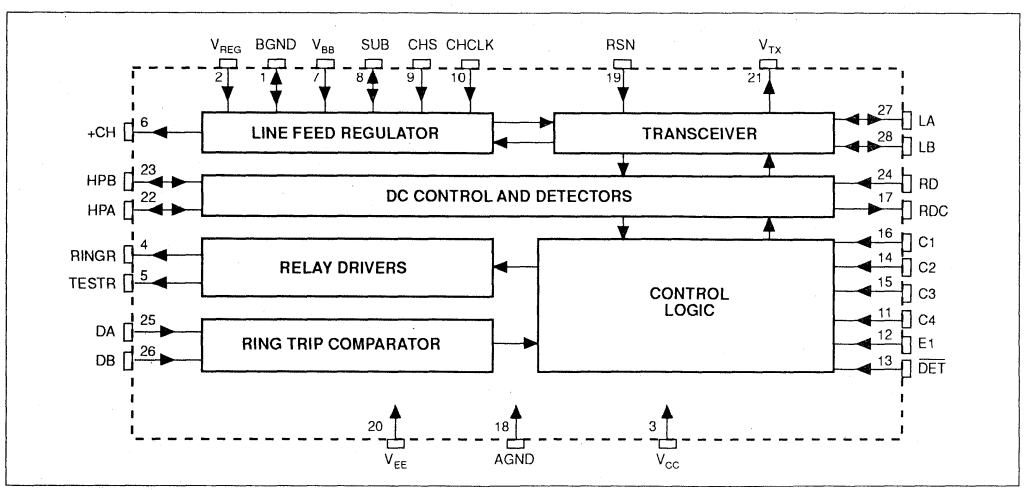


Figure 2: Functional block diagram

FUNCTIONAL OVERVIEW

The SL377 Subscriber Line Interface Circuit (SLIC), together with some external components, provides most of the line interface functions for ordinary or PABX line connections in a telephone network. It performs the interface between the two wire line and an ALAP (Analogue Line Audio Processor)/ COMBO, such as the GEC Plessey Semiconductors MV3010-1 SLAC (Subscriber Line Audio Circuit) DSP device.

The SLIC circuit contains several functional blocks to achieve the design aims (Fig.2). Firstly, the Transceiver consists of the two wire port, pins LA and LB. These pins are fed from the 4 wire input (RSN) controlling AC conditions, and from the Line Feed Regulator and DC Control blocks, controlling DC conditions. The 2 wire transverse AC signal is fed onto the 4 wire transmit output, VTX.

Power dissipation is minimised, under varying line conditions, by the Line Feed Regulator which adjusts the internal high voltage supply to that required for line feed. It consists of a switching regulator which can be synchronised to a 256kHz clock.

DC line conditions at the 2 wire interface are determined by the DC Control block. These DC conditions (modes of operation) are set by the Control Logic, which also monitors line status (On/Off-Hook) via the DC Control block detectors (Loop/Ground Key/Ring Trip comparator). The control logic also controls the Ring Relay Driver for Ringing mode of operation and an undedicated Test relay driver.

A brief outline of the device functionality is given below, before a more detailed discussion of the SLIC circuitry in the Functional Description section.

LINE FEED

Line loop (pins LA &LB) feeding is obtained from the battery supply (pin 7) by means of an internal power circuit, which can be set to different modes of operation (refer to table 2). These modes are as follows:

Disable Mode

Disable mode is the SLIC's low power mode in which the battery feed circuit limits the DC loop current to a level just sufficient to enable the SLIC to detect current above the On/ Off-Hook threshold. Both the Loop and Ground Key detectors work in this mode.

Disconnect A and B Leg

This mode programs the SLIC such that the A and B leg output amplifiers are turned off, preventing current flow to the line.

Disconnect A, Disable B Leg

This is the SLIC Standby mode with the A Leg amplifier turned off, so that current can only flow in the B Leg. In this state it is only possible to detect the application of a ground to the B Leg.

Active Mode

This is the normal operating mode with a call in progress. The SLIC is used as a constant current feed device, with the feed current being set by external resistors.

Polarity Reversal

The polarity of the feeding voltage at the SLIC can be reversed on command, in Active and Disable modes.

All Active and Disable conditions apply equally to the respective reverse conditions. In these conditions the polarity of any DC parameter is reversed.

Ringing

This mode enables the Ring Relay output and selects the Ring Trip comparator. It does not provide DC line feed or AC ringing voltage which must be supplied externally (via the ring relay).

Test Mode

Testing of the line is not performed by the SLIC. This mode enables external access to the telephone line by directly driving the test relay.

SUPERVISION

The SLIC provides an Off-Hook (or loop) Detector (OHD), Ring Trip Detector (RTD) and a Ground Key Detector (GKD). These are described below, in addition to the SLIC on-chip thermal protection.

Off-Hook Detector

The Off-Hook Detector recognises the loop status by means of a threshold circuit. The OHD operates in Disable and Active modes (with or without polarity reversal), and in the presence of longitudinal currents. The detector threshold is nominally the same in Disable and Active modes, the actual level being externally programmable.

Ring Trip Detector

This detects when a subscriber goes off-hook during the application of a ringing signal (normally 25Hz) within a maximum delay of 150ms (determined by external components - see Applications section). The detector is active when the Ring Relay Driver is activated.

Ground Key Detector

The GKD circuit detects a current path from the A or B Leg to ground. It can be used in Disable, Active and Disconnect A Disable B modes.

Thermal Protection

In conditions which cause the chip junction temperature to rise above a critical level (around 150°C), the thermal protection will operate. This switches off the line current and therefore reduces the power dissipation.

TRANSMISSION

The signal transmission functions include 2 to 4-wire and 4 to 2- wire conversions.

The 2-wire termination impedance of the SLIC is programmed by external components. Transmit and Receive Gain are fixed and are nominally both unity (0dB), with the 2-wire port terminated in a matched load.

All the transmission parameters apply when the SLIC is operating in the presence of longitudinal currents, as specified in the Electrical Characteristics.

CONTROL

The SLIC is provided with a digital interface for controlling the 2-wire line status and passing line status information to the line card/system hardware. The operating characteristics can be selected by hardware with external components (see Digital Interface).

METERING

Injection of high amplitude high frequency meter pulses is not supported by the SL377. If this function is required, then the GPS SL376 Metering SLIC can be used instead (refer to separate Data Sheet).

RINGING

The application of the ringing voltage to the subscriber line can be via a relay or suitable high voltage crosspoint, external to the SLIC. This component is driven by the on-chip Ring Relay Driver. The relay is connected between RINGR and V_{BAT}.

When the SLIC is set to RING mode, the Ring Relay Driver output will be activated to energise the ring relay. The relay should be connected so as to cause the line to be disconnected from the SLIC and connected to a suitable ringing supply (continuous) voltage. Ring cadence can then be obtained by de-energising and re-energising the relay as required.

OVERVOLTAGE PROTECTION

Overvoltage protection is required to protect the SLIC from such line phenomena as lightning strikes, and induced AC signals from, or direct contact with, power lines. This protection can be realised with components external to the SLIC (refer to SLIC Application Note AN82).

INTERFACES

The SLIC has three main interfaces to external circuitry. These are the 2-wire, 4-wire and Digital interfaces which are described below.

Subscriber Line Interface (2-wire port)

Pins LA and LB form the Subscriber Line Interface providing line feed, signalling supervision and voice transmission between the subscriber's apparatus and exchange. It exhibits very good balance about ground to minimise the crosstalk between adjacent pairs in the local cable and noise from longitudinal interference. The termination impedance is set externally by Z_{TX} (see Fig. 3 and Functional Description).

The 2-wire port is designed to offer a low impedance to any longitudinal signals that appear on the subscriber line and the resulting signal level at the 4-wire output port is minimised.

It is able to handle longitudinal currents on the subscriber line in all modes of operation, except Disconnect mode, Ringing and Disconnect A Disable B when the SLIC 2-wire port is no longer connected to the line.

Analog 4-wire interface

Two pins of the SLIC (V_{TX} and RSN), together with associated grounds, provide the 4 wire interface to an ALAP or COMBO device. Both the transmit (V_{TX}) and receive (RSN) signals are unbalanced and have fixed gain settings. The V_{TX} pin has a low output impedance, whilst the RSN pin is a low impedance virtual earth input. The input current is normally a combination of the receive voice signal from the ALAP, line feed current programmed by the RDC pin (see Applications section) and termination of the V_{TX} pin.

Hybrid Balancing is not provided on the SLIC. This can be done by an ALAP such as the MV3010-1 SLAC which uses DSP techniques, including an Adaptive Echo Cancellation feature.

Digital Interface

This is a parallel interface providing control of all the SLIC operating modes and indication of line status information. It consists of the 6 pins as listed in Table 1, the functions of which are described in Table 2.

Pin designation	Pin description
C1	Data Input
C2	Data Input
C3	Data Input
C4	Test Select Input
E1	Detector Select Input
$\overline{DET}$	Detector Data Output

Table 1: Digital interface pin designation

Mode	C4	C3	C2	C1	DET output status (Note 2)		Test relay
					E1 = 0	E1 = 1	
Disconnect A & B Legs	X	0	0	0	(Invalid)	(Invalid)	-
Ringing	X	0	0	1	Ring Trip (Note 3)	-	-
Active (non-ringing)	X	0	1	0	Loop Detect	Ground Key	-
Disable	X	0	1	1	Loop Detect	Ground Key	-
Disconnect A, disable B	X	1	0	0	(Invalid)	Ground Key	-
Reserved	X	1	0	1	-	-	-
Active, polarity reversed	X	1	1	0	Loop Detect	Ground Key	-
Disable, polarity reversed	X	1	1	1	Loop Detect	Ground Key	-
Line test (note 1)	0	X	X	X	-	-	Enabled
	1	X	X	X	-	-	Disabled

NOTES

1. C3, C2, C1 still change SLIC status even though Line outputs will be disconnected from line.
2. $\overline{DET}$ = 1 for On-Hook (high line impedance), $\overline{DET}$ = 0 for Off-Hook (low line impedance).
3. $\overline{DET}$ = 1 for Voltage DA > DB, $\overline{DET}$ = 0 for Voltage DA < DB.

Table 2: Digital interface functional description

FUNCTIONAL DESCRIPTION

VOICE TRANSMISSION AND RECEPTION

It is conventional to assign the signal directions from the point of view of the served telephone set. The receive direction is towards the served telephone and the transmit direction is from it.

The basic voice circuit for the device is shown in Fig.3. The current which flows on the line, into LA and out of LB is 1000 times the current which flows into RSN and through the device to AGND.

The AC voice current flowing into RSN is composed of the current from VRX through ZGR, which controls the signal received at the remote telephone and a current from V_{TX} through Z_{TX} which controls the termination impedance. There is also a DC current at RSN which is analysed later in the discussion on DC line feed.

The 2-wire termination impedance is $Z_{AB} = (Z_{TX} \div \alpha)$ where a ($\approx$1000) is the current gain between RSN and I_L (see Fig.3). This can be checked by setting V_{RX} to zero.

The Receive Gain, for normal voice signals (at V_{RX}). is inversely proportional to Z_{GR}. The actual value, which is negative, can be obtained by setting $(V_L)_{ac}$ equal to zero in Fig.3. This gives:-

AC voltage between LA and LB $(V_{LA}-V_{LB})_{ac}$

$= (V_{LA}-V_{LB})-(V_{HPA}-V_{HPB})$

$= (I_L)_{ac} \times \{Z_{AB}||Z_L\}$

$$= -\left(\frac{Z_L \times \frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right)\frac{V_{RX}}{\frac{V_{GR}}{\alpha}}$$

i.e. minus the ratio of the line and terminating impedances (Z_L and $Z_{TX} \div a$) in parallel, to the receive impedance divided by the current gain ($Z_{GR} \div a$). This expression simplifies to :-

$$= \frac{-V_{RX}\alpha Z_L Z_{TX}}{(\alpha Z_L + Z_{TX})Z_{GR}}$$

In the transmit direction, the voltage at V_{TX} is the superposition of the voltage from the line, with the voltage produced on the line from V_{RX}, i.e:-

$$V_{TX} = \left[\left(\frac{\frac{Z_{TX}}{\alpha}}{Z_L \div \frac{Z_{TX}}{\alpha}}\right)V_L - \left(\frac{Z_L \times \frac{Z_{TX}}{\alpha}}{Z_L + \frac{Z_{TX}}{\alpha}}\right)\frac{V_{RX}}{\frac{Z_{GR}}{\alpha}}\right]$$

This expression simplifies to :-

$$V_{TX} = \frac{[Z_{GR}(V_L)_{ac} - \alpha Z_L V_{RX}]Z_{TX}}{(\alpha Z_L + Z_{TX})Z_{GR}}$$

This equation can be used to determine the transmit gain, from $(V_L)_{ac}$ to V_{TX}, by setting $V_{RX} = 0$ which gives $+Z_{TX} \div (\alpha Z_L + Z_{TX})$. The 4 wire-4 wire gain, V_{RX} to V_{TX}, is also given by this equation when setting $(V_L)_{ac} = 0$, which gives us the alternative result $-\alpha Z_L Z_{TX}[(\alpha Z_L + Z_{TX})Z_{GR}]$. If fuse resistors are included in the 2 wire loop, then Z_L is modified to become $(Z_L + 2R_{FUSE})$ in the above equations.

The transmission circuitry also contains a longitudinal feedback circuit, such that the SLIC appears as typically 25Ω resistors from LA and LB to a bias voltage (see DC Line feed section). This bias voltage comes from the DC feed circuitry. The feedback circuit attenuates longitudinal signals from the transmit path, and has no effect on transverse signals.

DC LINE FEED (ACTIVE MODE)

DC line feed (loop) current $I_L = {}^1/_2(|I_A - I_B|)$ is provided by the device when it is in non-ringing modes. In RING mode, DC line feed and AC ringing voltage are normally applied through the Ring relay which is controlled by the device. The line feed current is reduced during standby operation.

In Active mode, Power feed is controlled by the resistance R_{DC} (= R_{DC1} + R_{DC2}) between the R_{DC} pin and the RSN pin (Fig.4). Again, the current in the 2 wire loop will be 1000 times the current into RSN. Operation of the DC feed circuitry is described with reference to Fig.4, which shows a conceptual model.

For the normal line feed region, a voltage V_{DC}, of magnitude 2.5V is produced at the R_{DC} pin. The sign of V_{DC} determines normal or reverse polarity operation. If negative, normal polarity is established and if positive, reverse polarity will occur (polarity is set by control logic see Table 2). This normal line feed region exists when $|V_{BAT}|-|V_{DCT}| \geq V_{SG}$ (V_{SG} = 15V nominally, $V_{DCT} = |V_{LA} - V_{LB}|$), else the Saturation Guard circuit is active (described later).

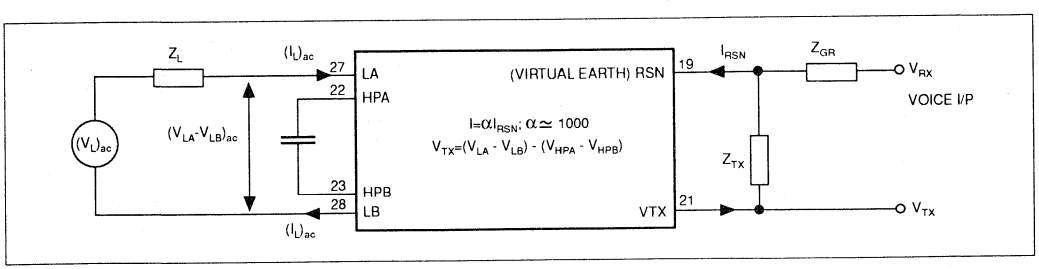


Figure 3: Voice circuit

Note that the internal resistors, R_{HP}, and external capacitor, C_{HP}, form a low pass filter network (see discussion on C_{HP} in SLIC Application Note AN82 Applications General Considerations Section). During the action of reversing polarity, the resistors R_{HP} are momentarily short-circuited to reduce the time taken for the DC voltage on C_{HP} to change sign.

The x1000 virtual earth input amplifier means that the feed current is determined by R_{DC}, i.e:-

$$I_{FEED} = 2500 \div R_{DC} \text{ (Saturation Guard inactive)}$$

If fuse resistors are included in the 2-wire loop, the feed current will not be affected. However, the fuse resistors will affect the line current in the saturation guard region (described later).

As an example, to set I_{FEED} = 40mA, then:-

$$R_{DC} = (R_{DC1} + R_{DC2}) = 2500 \div I_{FEED} = 62.5k\Omega$$

The values Of R_{DC1} and R_{DC2} should be kept nearly equal, forming a low pass filter network with C_{DC} to reduce chopper noise from the R_{DC} pin (see also discussion in AN82 Applications General Considerations Section). The time constant of this network (C_{DC} and $R_{DC1}||R_{DC2}$) also affects the time taken for a polarity reversal, and it is normally ≈ 1.5ms.

The remaining circuitry models the action of the saturation guard circuit. This operates to reduce the voltage at the R_{DC} pin when:- $|V_{BAT}|-|V_{DCT}|<V_{SG}$. V_{SG} is a notional threshold voltage which is the headroom between the value of V_{DCT} and the battery voltage at the point where saturation guard becomes active (this includes the diode drop in series with the V_{BAT} supply, D_2 figure 7). Thus, when the comparator determines this condition, the magnitude of the difference is used to reduce the voltage at R_{DC}.

The total line feed characteristic is shown graphically in Figs. 6a and 6b. The nearly constant voltage region is due to the action of the saturation guard circuit, and is affected by the value of R_{FUSE} as shown in Fig. 6a. Fig. 6b plots the loop current value as a function of line resistance R_L. The example shown is that of a 40mA (R_{DC} = 62.5kΩ) feed current, the graphs being obtained by using the simple models of Figs. 5a and 5b (on fuse resistors). Figs. 6a and 6b also show the action of V_{BB} on the line characteristics.

With the Saturation Guard inactive, normal line feed conditions apply such that the feed current and line/loop resistance determine VL by the following relationship:-

$$V_L = I_L \times R_L$$

This gives the characteristic shown in Fig. 6a, which is the vertical line section of the graph.

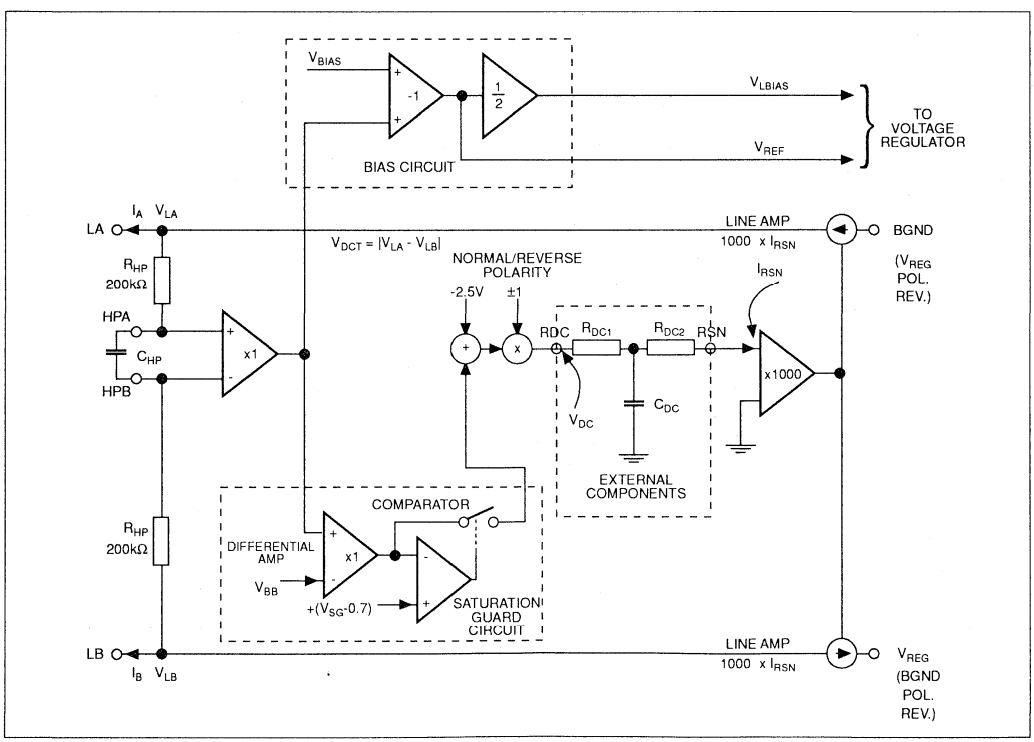


Figure 4: DC power feed circuit model

When the saturation guard is active, then the line voltage is effectively held constant due to the reduction of the voltage at the RDC pin. Thus, line conditions are set by the following:

$$I_L = [(|V_{BAT}|-V_{SG}) \div (R_L + 2R_{FUSE})]$$

To determine the line resistance (R_{LSG}) and Line voltage (V_{LSG}) at which the saturation guard becomes active, these parameters are obtained by equating the two expressions for normal and saturation guard regions. Thus,

$$R_{LSG} = [(|V_{BAT}|-V_{SG}) \times (R_{DC} \div 2500)]-2R_{FUSE}$$
$$V_{LSG} = |V_{BAT}|-V_{SG}-[2R_{FUSE} \times (2500 \div R_{DC})]$$

The resultant line voltage (V_{LSG}) that occurs depends on the ohmic relationship of I_{LSG} and R_{LSG} (see Fig. 6a) which will equal $|V_{BAT}|-V_{SG}$ when $2R_{FUSE}=\infty\Omega$. The open circuit voltage, $V_{LOC} \approx |V_{BAT}|-V_{SG}$ at $R_L = 0\Omega$. will always be greater than V_{LSG}. even when $2R_{FUSE} = 0\Omega$. This change in voltage between V_{LSG} and V_{LOC} will be greater at lower battery voltages. Fig. 6a shows the nominal effect.

DC LINE FEED (DISABLE MODE)

During normal and reverse Disable Mode an internal reference is used to feed the d.c. line current at a nominal 20mA into 600Ω. This condition will support Loop detection and speech Transmission.

LINE POLARITY

Normal line polarity (Active/Disable) consists of the LA pin voltage near to BGND and the LB pin voltage near to V_{BAT}. Under these conditions $I_L = +{}^1/_2|I_A - I_B|$ and the voltage at the R_{DC} pin will be negative. Reverse polarity will give LA voltage near V_{BAT}. LB voltage near BGND, $I_L = -{}^1/_2|I_A - I_B|$ and the R_{DC} pin is positive.

BIAS CIRCUIT

The Bias circuit (Fig. 4) produces two reference voltages, both referred to ground. These are V_{REF}, being related to the 2-wire transverse DC voltage and V_{LBIAS} approximately half V_{REF}.

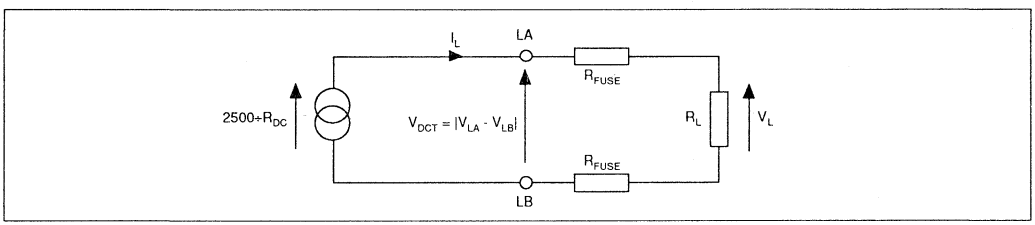


Figure 5a: Simple power feed model (normal line feed)

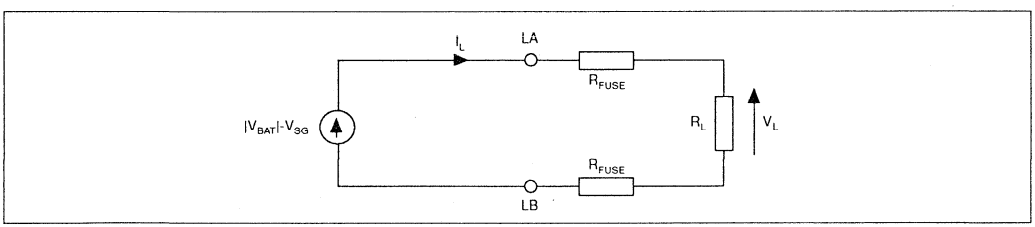


Figure 5b: Simple power feed model (saturation guard active)

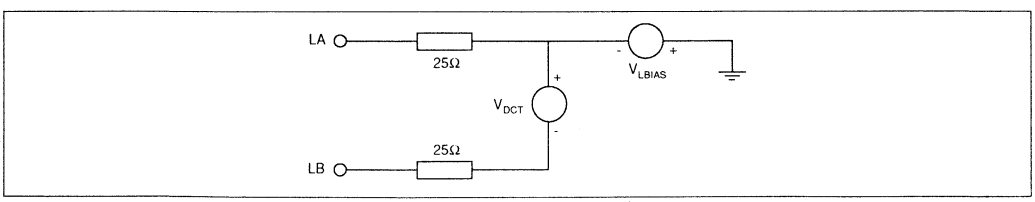
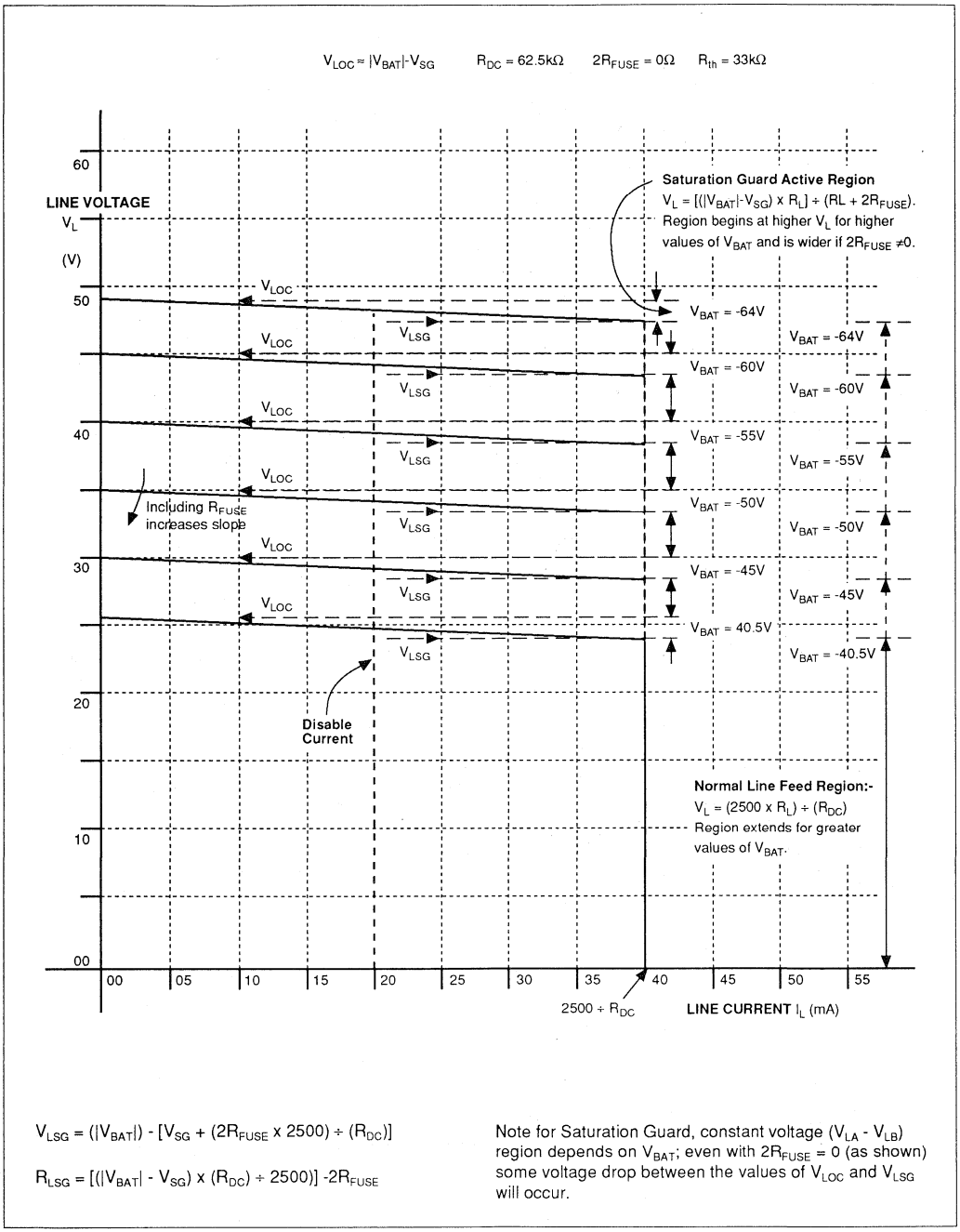


Figure 5c: Longitudinal bias circuit



$V_{LSG} = (|V_{BAT}|) - [V_{SG} + (2R_{FUSE} \times 2500) \div (R_{DC})]$

$R_{LSG} = [(|V_{BAT}| - V_{SG}) \times (R_{DC} \div 2500)] - 2R_{FUSE}$

Note for Saturation Guard, constant voltage (V_{LA} - V_{LB}) region depends on V_{BAT}; even with $2R_{FUSE} = 0$ (as shown) some voltage drop between the values of V_{LOC} and V_{LSG} will occur.

Figure 6a: Line feed characteristic, V_L vs I_L

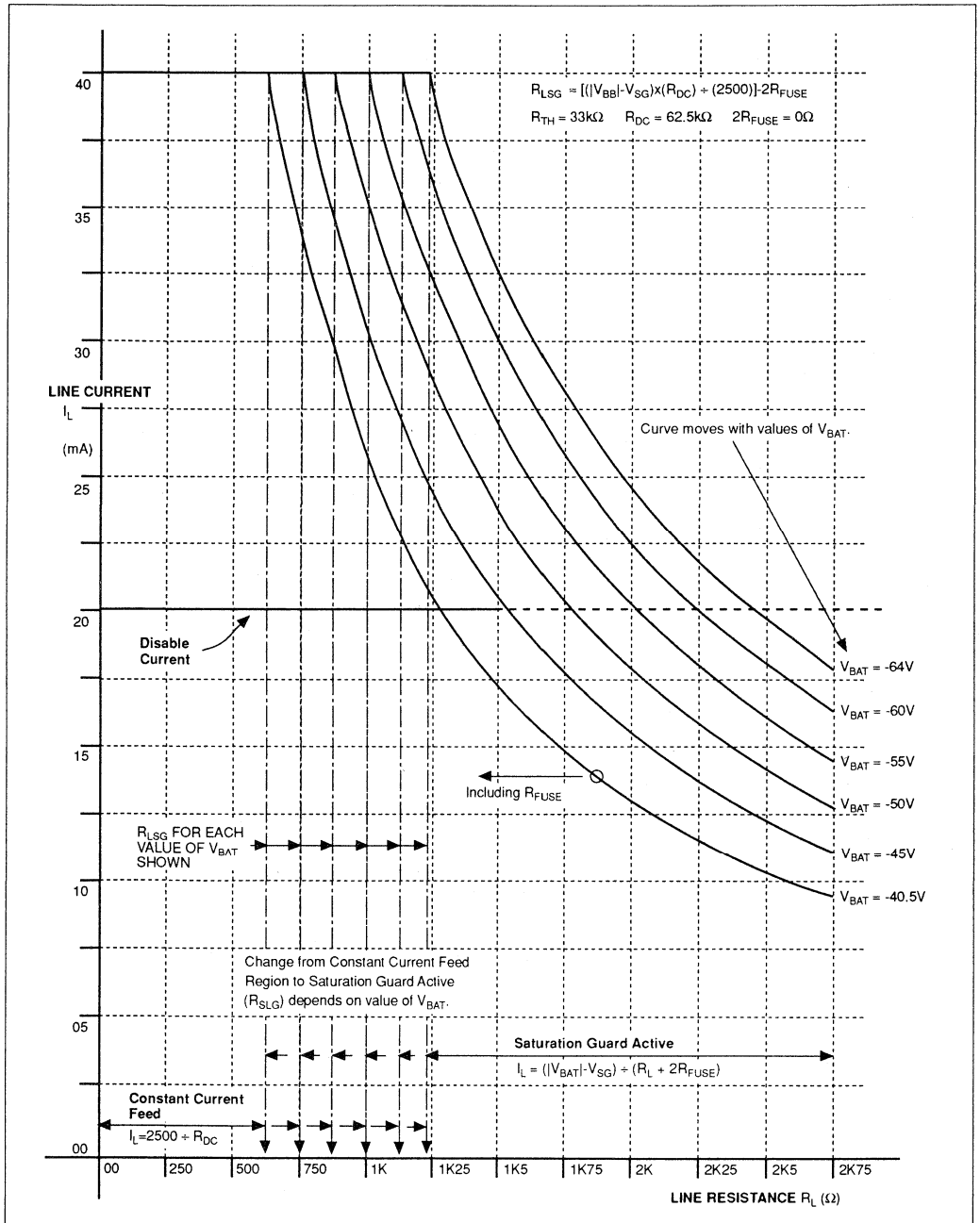


Figure 6b: Line Feed Characteristic, I_L vs R_L

V_{REF} controls the line feed regulator and V_{LBIAS} sets the 2-wire feed balance voltage (centre point voltage of the lines). The longitudinal control loop achieves an input impedance of approximately 25Ω per line for longitudinal signals, as shown in Fig. 5c.

LINE FEED REGULATOR

The DC voltage between LA and LB will vary with the DC loop resistance. Unless the voltage supplied to the chip can be varied to match that on the line there will be a voltage drop across the chip along the path taken by the feed current. This could cause significant power dissipation. The purpose of the line feed regulator is to minimise this power dissipation by regulating the voltage supplied to the line amplifiers.

Regulated voltage is supplied to the line amplifiers on V_{REG} and unregulated voltage is supplied on V_{BB}. The chip switches V_{BB} onto +CH when more power is required at the V_{REG} pin. V_{REG} is the voltage used by the device to power the 2-wire interface, and it is adjusted to follow a reference voltage V_{REF} (from Power Feed). This reference voltage is determined as follows:

$$V_{REF} = -\{ | V_{DCT} | + V_{BIAS} \}$$

and is such to set V_{REG} to the minimum required to power the line interface, thus minimising power dissipation. The voltage V_{BIAS} is needed to keep the amplifier response linear when audio signals are transmitted.

Fig. 7 shows the external components associated with the power supply aspect of the voltage regulator. + CH is the positive terminal of the regulator switch that connects to V_{BB}.

When the switch is turned on, current in L_1 and C_1 increases, thus increasing stored energy. When the switch turns off, this stored energy sustains L1 current which flows in D_1. The voltage at +CH is thus a square wave of up to 50V p-p making this node sensitive to PCB layout. Note that the inductor should be capable of taking twice the line current without saturating. The regulator will work with a wide range of inductor resistance, although if this is too large, long line drive capability and regulator efficiency will be reduced. Since there are large current fluctuations from V_{BB} through the switch, C_2 provides filtering of the V_{BB} pin, whilst D2 isolates the V_{BAT} supply should the LA/LB pins be taken negative of the V_{BAT} supply.

The chip senses the voltage at V_{REG}, compares it to its requirements and switches power from V_{BB} to +CH, using the variable mark/space method, to give appropriate matching. The rate of switching can be governed by CHCLK (pin 10) or allowed to free run, its stability ensured by the network on CHS (pin 9), i.e. C_3, R_1, C_5. Since noise is produced by the switching, a decoupling node is provided at SUB (pin 8).

CONTROL AND SIGNALLING

The mode of operation of the SL377 is determined by the digital interface pins, as described in Tables 1 and 2. These pins enable ringing or non-ringing modes of operation, controlling line status, line polarity, relay driver and selection of line detector.

The line status is selected by use of the C3..C1 pins, Table 2, to determine the modes as listed. The function of these modes has already been described in the 'Overview' and 'DC Line Feed' sections; more detail of the device detectors is given on the following page (refer to Fig. 8).

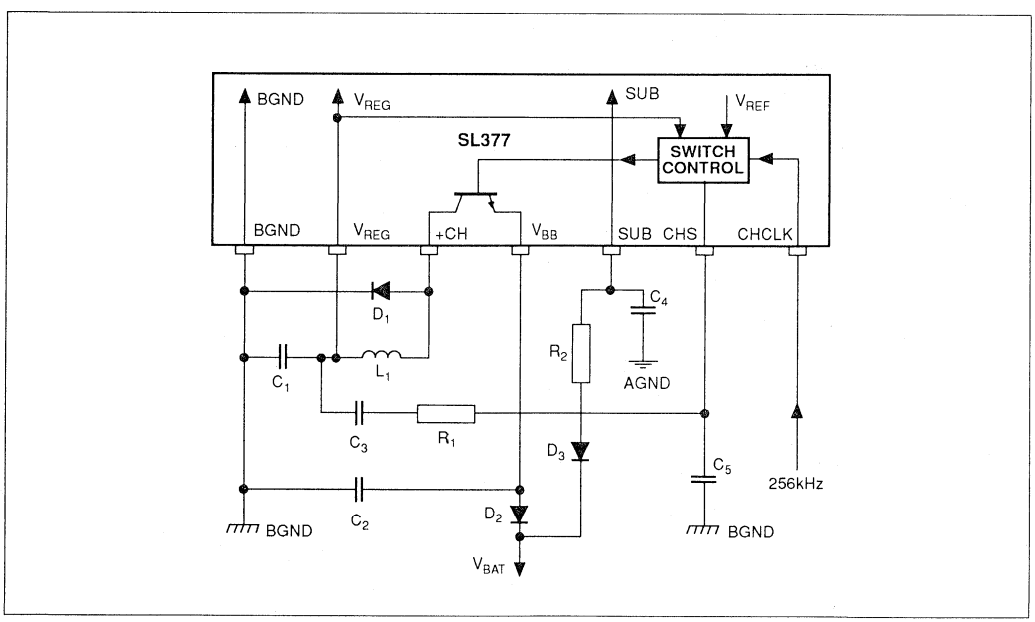


Figure 7: Voltage regulator power supply circuit

Loop Detect

This detector is used in Active and Disable modes (with/without polarity reversal). The loop current at which the detector indicates the Off-Hook condition, is set by the comparator at pins 24 (RD) and 20 (V_{EE}). Normally a resistor, R_{TH}, is connected between these pins, such that Off-Hook line current threshold (I_{DET})is set by:

$$I_{DET}=350 \div R_{TH}$$

This is due to the fact that the current out of the RD pin is equal to the loop current IL=(1/2|I_A-I_B) divided by ~280. This will create a voltage across R_{TH} at the RD pin. Off-Hook is given by a logic low at the $\overline{DET}$ output pin (when detector is selected) when this voltage rises above the internal 1.25V reference.

Ground Key Detector

This detector is selected by the E1 pin of the Digital Interface. It can be used in Active and Disable modes (with/without polarity reversal), as well as Disconnect A Disable B mode.

Operation of the detector is via an internal threshold and the longitudinal current I_{LL}= I_A+I_B of the 2-wire loop. Ground Key detection is indicated when either the midpoint of the A and B legs is connected to ground, or the B leg (A leg, polarity reversed) is connected to ground. The resistance values for which Ground Key detection is valid are given in the Electrical Characteristics section.

Ring Trip Detector

This consists of a comparator connected to the DA and DB pins, and indicates Ring Trip when the voltage at DA < DB. Selection of Ringing mode operates the Ring Relay and enables the Ring Trip Detector. The external ringing supply must consist of DC line feed in addition to the AC ringing voltage. In order that the Ring Trip Detector senses Ring Trip in ringing mode, a resistance bridge network is used in association with pins DA, DB, line and ring source. This network is described in the Applications section of this data sheet.

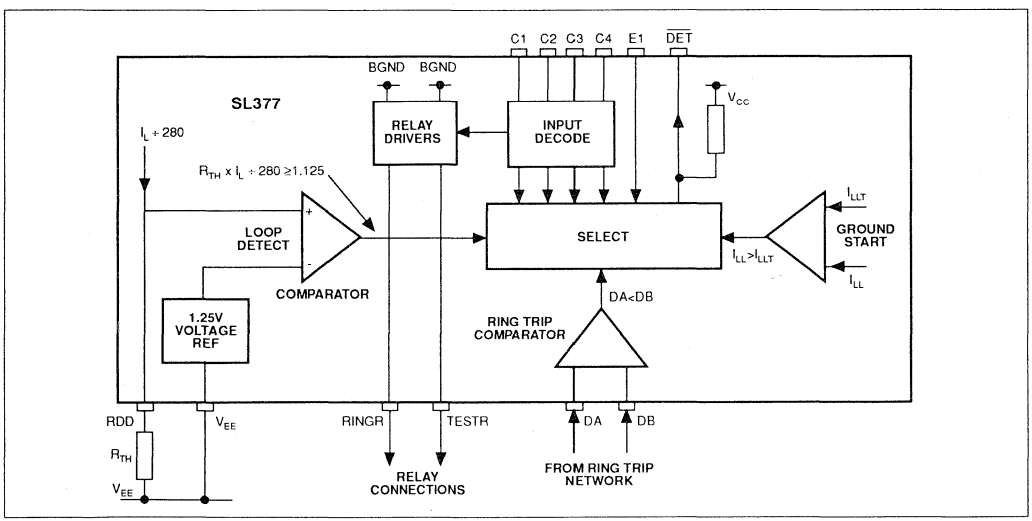


Figure 8: Detector circuits

FUNCTIONAL PARAMETER SUMMARY

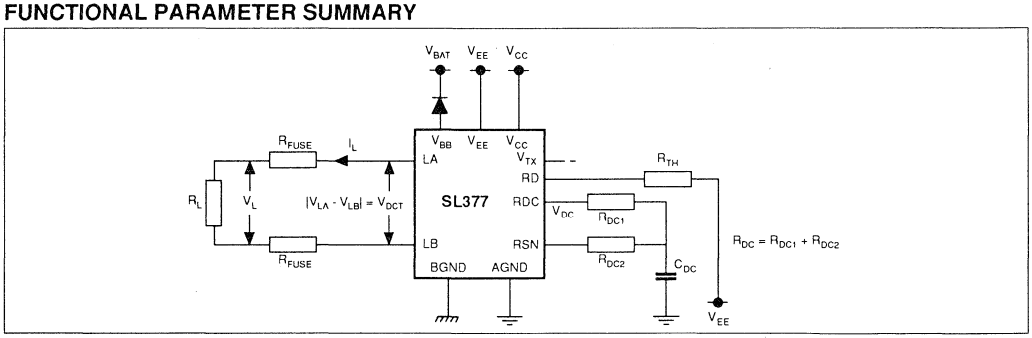


Figure 9: DC parameters and components for the SL377

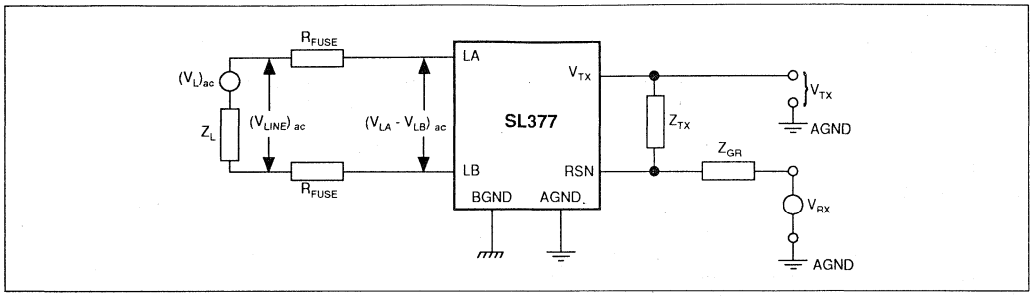


Figure 10: AC parameters and components for the SL377

LIST OF DEFINITIONS

1. Loop Current is defined as :- $I_L = \pm{}^1/_2|I_A - I_B|$

   I_A = current out of LA pin, I_B = current out of LB pin, + ⇒ normal line polarity and − ⇒ reverse line polarity.

2. Longitudinal Current is defined as :- $ILL = (I_A + I_B)$

   I_A = current out of LA pin, I_B = current out of LB pin.

3. Normal Line Feed Region when $|V_{BAT}|-|V_{DCT}| > V_{SG}$ with $I_L = I_{FEED} = (2500 \div R_{DC})$

4. Saturation Guard Threshold when $|V_{BAT}|-|V_{DCT}| = V_{SG} = 15.0V$ such that :-

   $V_L = V_{LSG} = |V_{BAT}|-V_{SG}\{2R_{FUSE} \times (2500 \div R_{DC})]$ which will equal $|V_{BAT}|-V_{SG}$ with $2R_{FUSE} = 0$ and
   $R_{LSG} = [(|V_{BAT}|-V_{SG}) \times (R_{DC} \div 2500)]-[2R_{FUSE}]$

5. Saturation Guard feed Region when $|V_{BAT}|-V_{DCT} < V_{SG}$ with $I_L = [|V_{BAT}|-V_{SG}] \div [R_L \div 2R_{FUSE}]$

6. Note that V_{LSG} is referred to as the value of the line voltage, V_L, at the point where Saturation Guard becomes active. This will differ from the value of $|V_{LA}-V_{LB}|$ (i.e. V_{DCT}) if $2R_{FUSE} \neq 0$. V_{SG} is used as a notional threshold voltage which is the internal headroom between the $|V_{LA}-V_{LB}|$ voltage and the battery supply, at this same point.

7. Open Circuit Line Voltage V_{LOC} at $R_L = \infty\Omega$ such that :- $V_L = V_{LOC} \approx [|V_{BAT}|-V_{SG}]$

   V_{LOC} will be $\geq V_{LSG}$ even with $2R_{FUSE}=0$. The voltage drop from V_{LOC} to the defined V_{LSG} point will be greater at lower values of V_{BAT}

8. 2 Wire Termination Impedance $Z_{AB} = (Z_{TX} \div \alpha) = (Z_{TX} \div 1000)$

   Note that Z_{TX} is normally set to $[\alpha(Z_L \div 2R_{FUSE})]$ where Z_L is the desired termination impedance.

9. Receive Gain from V_{RX} to $(V_{LA}-V_{LB})_{ac}$ or $(V_{LINE})_{ac}$ is set by Z_{GR} after setting Z_{TX}. Thus, with $(V_L)_{ac} = 0$:-

$$\frac{(V_{LA} - V_{LB})_{ac}}{V_{RX}} = \frac{-\alpha Z_L Z_{TX}}{[\alpha(Z_L) + Z_{TX}]Z_{GR}} \quad \text{with } 2R_{FUSE} = 0; \qquad \frac{(V_{LINE})_{ac}}{V_{RX}} = \frac{-\alpha Z_L Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]Z_{GR}} \quad \text{with } 2R_{FUSE} \neq 0$$

10. Resultant Transmit Gain is then :-

$$\frac{V_{RX}}{(V_L)_{ac}} = \frac{Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}} \quad \text{with } V_{RX} = 0$$

11. Resultant 4 Wire-4 Wire Gain is then :-

$$\frac{V_{TX}}{V_{RX}} = \frac{-\alpha(Z_L + 2R_{FUSE}) + Z_{TX}}{[\alpha(Z_L + 2R_{FUSE}) + Z_{TX}]Z_{GR}} \quad \text{with } (V_L)_{ac} = 0$$

12. Off-Hook Threshold is set by R_{TH} at :- $I_L = I_{DET} = 350 \div R_{TH}$.

13. Ring Trip Threshold is set by the bridge associated with pins 25 .. 28 and the 2 Wire Line, thus :-

$R_L = R_{LTH} = R_{B4}(2R_F) \div (R_{B4}\text{-}R_{B1})$ assuming $R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$ and $R_{FEED1} = R_{FEED2}$ for the bridge components (balanced ringing). R_{B1}.....$R_{B4} \approx$ a few 100KΩ and $R_{FEED1} \approx$ a few 100Ω .

14. AC ringing voltage at DA (DB by the same amount) is reduced by a factor of :- $[1 + (2\pi f_r t_r)^2]^{1}/_{2}$

f_r is the ringing frequency and t_r is determined by the bridge components including C_B, thus :- for balanced ringing. $t_r = \dfrac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$

APPLICATIONS

The requirements for the subscriber line interface vary considerably from one telephone administration to another The SL377 is designed to have the flexibility to meet these varying requirements. For simplicity, only a single example is given to illustrate how the device is connected. Fig. 11 shows the circuit which can be used to evaluate the device.

Further Applications information is given in SLIC Applications Note AN82.

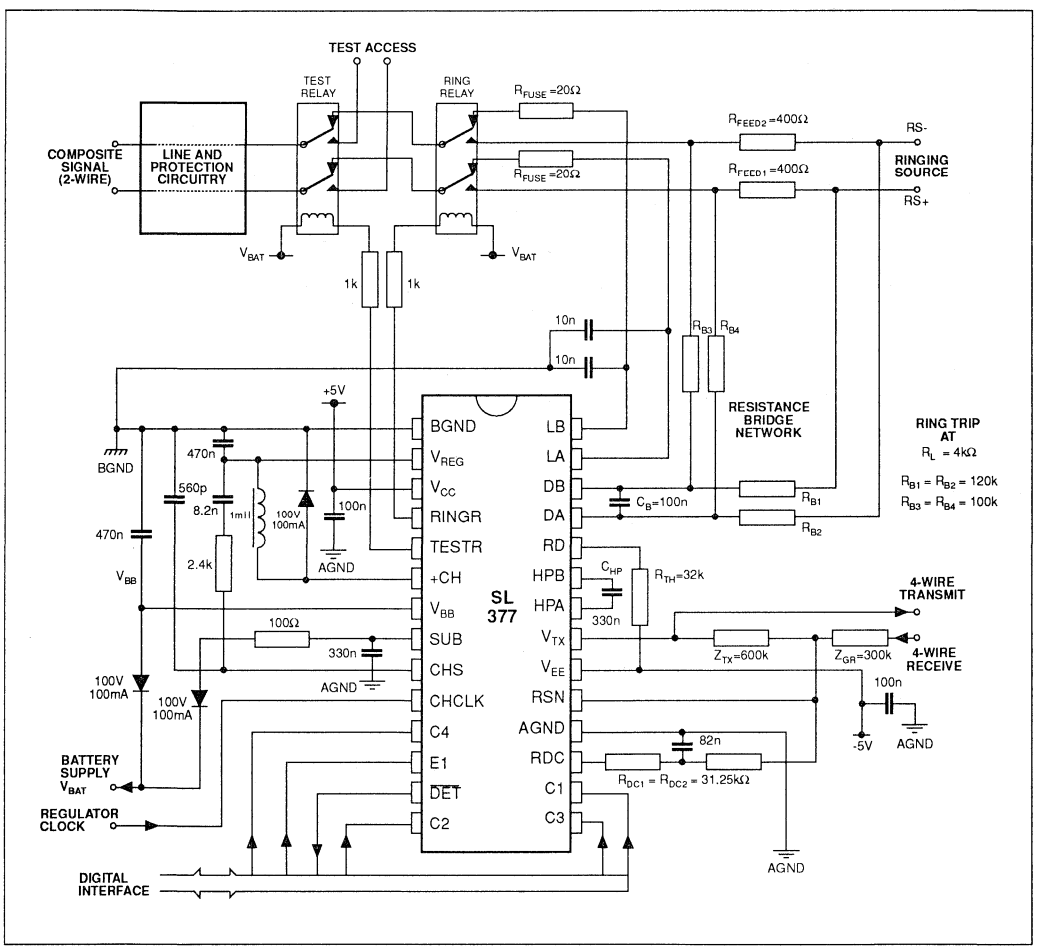


Figure 11: Application circuit

The DA and DB pins are connected to a resistance bridge network (R_{B1} to R_{B4}). This allows the change in line resistance to be sensed when the remote telephone goes off-hook during ringing (ring trip). The details of this network (and C_B) are given later (see Ring Trip section). The resistors R_{FEED1} and R_{FEED2} provide feeding of the ringing source onto the line during ringing mode. The Ring Relay coil is connected through current limiting resistors.

Connections to the LA and LB pins are shown, and include the resistors R_{FUSE} in addition to the ring relay. These resistors have a value around 20 to 30 ohms, depending on the application, and provide current line protection.

Overvoltage and protection circuitry may consist of slew-limiting inductors between the pins and the line itself and a thyristor or Zener protection network at the line. In many applications, especially in PBXs, the amount of protection circuitry can be reduced. The capacitors between LA, LB and ground, allow noise from the regulator to be decoupled.

The capacitor C_{HP} between HPA and HPB is used to filter out the AC component of the signal on the line. The voltage difference between the two pins should be effectively DC. The SLIC Application Note AN82 contains a further discussion on this component.

The resistor, R_{TH}, between RD (pin 24) and V_{EE} (pin 20) programs the threshold current for the loop detector. A capacitor in parallel can be added to reduce the effect of the AC component of the line current, but this can cause instability on standby operation with highly inductive lines if it is too large. The value of R_{TH} sets the current I_{DET} according to the relationship:-

$$I_{DET} = 350 \div R_{TH}$$

The CHS pin (pin 9) is connected to BGND through a capacitor and to V_{REG} by a capacitor and resistor in series. This stabilises the regulator control loop (pins 2, 6 and 7).

It is recommended that the substrate (SUB) pin is decoupled to AGND. However, BGND may be used if this is sufficiently quiet, otherwise some degradation in noise performance may be experienced.

DC current flows between RDC (pin 17) and RSN (pin 19). This is used to set the line feed current. Any minor AC fluctuations are reduced by dividing the resistance equally such that $R_{DC1} = R_{DC2} = {}^1/_2R_{DC}$ and connecting a capacitor from the junction of R_{DC1} and R_{DC2} to AGND.

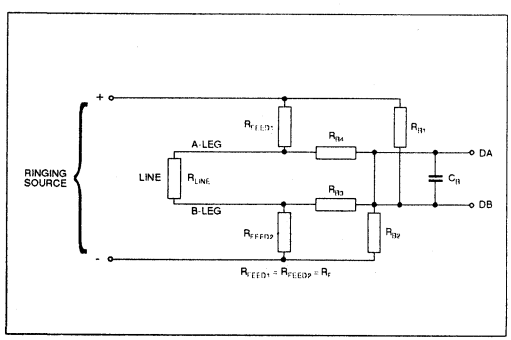


Figure 12: Ring trip circuit (balanced ringing)

The network (Z_{TX}) between V_{TX} and RSN controls the AC terminating impedance. This can also be a complex impedance. The value of Z_{TX} can be calculated from the relationship :-

Z_{TX} = (Required Z_T) x (Receive current gain)

Connections for both Ring and Test relays are also shown in Fig 11. Note that the 1kΩ resistors provide current limit through the relay coils when the driver outputs are on.

Control and status pins are compatible. They are designed to give a simple interface to digital circuits and are directly compatible with the MV3010 SLAC.

RING TRIP

Ring Trip detection operates by comparing the voltages on DA and DB and providing the output on $\overline{DET}$ when this function is enabled using the status input pins of the Digital Interface. A resistance bridge (R_{B1} to R_{B4}) must be connected to the line and to the ringing voltage sources to cause the differential voltage between DA and DB to change sign when the line resistance falls below the level associated with Ring Trip. Note that it is simplified by use of $R_{B1} = R_{B2}$ and $R_{B3} = R_{B4}$ (see discussion in AN82).

Ringing voltage is normally applied to the line through the Ring Relay which is activated by RINGR. The ringing voltage sources, including line feed, are connected to the line via ringing feed resistors, R_{FEED1} and R_{FEED}. The resistance bridge operates by allowing the DC voltage dropped across the ringing feed resistors (RF) in the OffHook condition to reverse the polarity of the voltage on DA and DB (DA< DB). Since the AC ringing voltage is greater than the DC feed, the capacitor CB (Fig. 12) will filter this out at the comparator inputs. The connection shown is suitable for balanced ringing only. For unbalanced ringing, separate capacitors from DA (CBI) and DB (CBZ) to ground will be required to achieve the same result.

Fig. 12 shows how the resistance bridge is connected when used with balanced ringing. The circuit can operate correctly provided there is a DC feed in addition to the AC ringing voltage.

If R_{LTH} is the line resistance correspondlng to the Ring Trip threshold (DA =DB), this can be determined from the values of RF ($R_{FEED1} = R_{FEED2} = RF$), R_{B1} and R_{B4} ($R_{B1} = R_{B2}$, $R_{B3} = R_{B4}$ as:-

$$R_{LTH} = \frac{R_{B4}(2\ R_F)}{(R_{B1}\text{-}R_{B4})}$$

R_{B1} and R_{B4} should be a few hundred kΩ.

The amplitude of the AC ringing voltage at DA (DB is by the same amount) is reduced by a factor of $[1 + (2\pi f_r t_r)^2]^{-1/2}$ where f_r is the ringing AC frequency and t_r is set by:-

$$t_r = \frac{2R_{B1}R_{B4}C_B}{(R_{B1} + R_{B4})}$$

for balanced ringing. For $f_r \approx 20$Hz, t_r should be ≈ 50ms. For unbalanced ringing C_B will become $C_{B1}C_{B2} \div (C_{B1} + C_{B2})$ in the above equation. More detail on Balanced and Unbalanced Ringing is given in AN82

PIN DESCRIPTIONS

Symbol	Pin no	Pin name and description
BGND	1	**Battery Ground (Power Input).** 0 Volts.
V_{REG}	2	**Regulated Voltage (Negative Power Input).** The voltage at this pin is compared to that required for line feed, and the result is used to control the voltage regulator.
V_{CC}	3	**Positive Supply (Power Input).** + 5 Volts.
RINGR		**Ring Relay Driver Output, Transistor Emitter.** This output is designed to drive a relay, when used together with the V_{BAT} supply.
TESTR	5	**Test Relay Driver Output (Pull-up Output)** This output is designed to drive a relay, when used together with the V_{BAT} supply.
+CH	6	**Switching Regulator (Chopper) Output (Negative Power Output).** Chopper switch transistor collector. An internal regulator controls the mark/space ratio of the switching waveform to maintain V_{REG} (pin 2) at the required voltage.
V_{BB}	7	**Battery Voltage (Negative Power Input).** This is the -50 Volt battery supply pin which connects to the V_{BAT} supply via an external diode. It is connected to the chopper switch emitter.
SUB	8	**Substrate (Decoupling Node).** An external decoupling capacitor (0.33µF) should be connected between this pin and AGND.
CHS	9	**Line Feed Regulator (Chopper) Stabilising Network.** This is the input to the voltage comparator which is used to control the switching regulator.
CHCLK	10	**Line Feed Regulator (Chopper) Clock (Digital Input).** This is the positive edge triggered, 256kHz clock input for the voltage regulator, which will free run in the absence of an input signal.
C4	11	**Control Input (Digital Input).** Enables the Test relay driver output pin.
E1	12	**Control Input (Digital Input).** Selects the line status detector (Loop or Ground Key).
$\overline{DET}$	13	**Detector Data output (Digital Output).** This pin outputs the status of the detector which has been selected by D0 - D3.
C2 C3 C1	14 15 16	**Control Input (Digital Input).** **Control Input (Digital Input).** **Control Input (Digital Input).** These inputs determine the SLIC operating mode, and control the ring relay, selection of ringing and non-ringing Modes, line polarity, line status and line detector.
R_{DC}	17	**DC Reference Voltage (Voltage Output).** A reference voltage of ± 2.5Volts (± depending on line polarity), is output at this pin, excepting Saturation Guard operation.
AGND	18	**Analog Ground (Analog Reference Node).** This is the ground reference pin for the analog signals. It also provides a ground reference for the Digital Interface. Signal reference and decoupling connections should be separately run to this pin.
RSN	19	**Receive Summing Node (Current Input).** The current which is input on this pin is used to control the transverse current at LA and LB.

V_{EE}	20	**Negative Supply (Power Input).** - 5 Volts.
V_{TX}	21	**Transmit Voltage (Voltage Output).** The voltage output at this pin is equal to the difference between the voltage (V_{LA}-V_{LB}) and the differential DC voltage (V_{HPA}-V_{HPB}), multiplied by the 2 to 4-wire voltage gain.
HPA HPB	22 23	**High Pass A, High Pass B - AC/DC separation (Voltage Inputs).** These inputs sense the DC feed voltages on the LA and LB pins respectively . Under normal operation they are connected to LA and LB respectively by internal resistors and should be connected as shown in Fig. 11.
RD	24	**Loop Detection Control (Current Output / Voltage Input).** This pin outputs a current which equals the transverse loop current through LA and LB divided by 280. Off-Hook is indicated via the $\overline{DET}$ pin when the voltage at this pin is $\geq$ (V_{EE} + 1.25) Volts.
DA DB	25 26	**Ring Trip Detector A, Ring Trip Detector B (Voltage Inputs).** These are the A and B inputs to the internal ring trip comparator. The output of the comparator controls the ring trip output on $\overline{DET}$.
LA LB	27 28	**A Line Transceiver, B Line Transceiver (Current Outputs / Voltage Inputs).** These two pins form the 2-wire port connecting to the subscriber loop.

ELECTRICAL CHARACTERISTICS

Operating Range

V_{CC} = +5.0V ± 5%, V_{EE} = -5.0V ± 5%, V_{BAT} = -40.5V to -64.0V (typical -48V), V_{BGND} = -0.1V to +0.1V, V_{IH} = 2.0V, V_{IL} = 0.7V, Z_L = ∞Ω. Voltages are measured with respect to analog ground (V_{AGND}).

Temperature T_{amb} = 0°C to +70°C.

Test Levels

1. Tested over full operating range.
2. Tested at 25°C but guaranteed over the full operating range.
3. Not tested, but guaranteed by characterisation.

Supply Characteristics

Characteristic	Symbol	Value			Units	Conditions	Test level
		Min.	Typ.	Max.			
Positive supply (V_{CC}) current, disconnect mode	I_{CC1}			4	mA		2
Positive supply (V_{CC}) current, disable mode	I_{CC2}			10	mA	On / Off-Hook, I_L = 0	2
Positive supply (V_{CC}) current. active mode	I_{CC3}			10	mA	On / Off-Hook, I_L = 0	2
Negative supply (V_{EE}) current, disconnect mode	I_{EE1}			2	mA		2
Negative supply (V_{EE}) current disable mode	I_{EE2}			4	mA	On / Off-Hook, I_L = 0	2
Negative supply (V_{EE}) current active mode	I_{EE3}			4	mA	On / Off-Hook, I_L = 0	2
Battery supply (V_{BB}) current disconnect mode	I_{BB1}			1.5	mA		2
Battery supply (V_{BB}) current disable mode	I_{BB2}			5	mA	On-Hook, I_L = 0	2
Battery supply (V_{BB}) current active mode	I_{BB3}			6	mA	On-Hook, I_L = 0	2

Supply Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions	Test level
		Min.	Typ.	Max.			
Positive supply (V_{CC}) rejection ratio, supply to 2-wire transverse	P_{SRT}		17		dB	See note 2; 50mV on supply, 300-3400Hz, Z_L = 600Ω	2
Positive supply (V_{CC}) rejection ratio, supply to 2-wire longitudinal	P_{SRL}		17		dB	See note 2; 50mV on supply, 300-3400Hz, Z_L = 600Ω	2
Negative supply (V_{EE}) rejection ratio, supply to 2-wire transverse	N_{SRT}		17		dB	See note 2; 50mV on supply, 300-3400Hz, Z_L = 600Ω	2
Negative supply (V_{EE}) rejection ratio, supply to 2-wire longitudinal	N_{SRL}		17		dB	See note 2; 50mV on supply, 300-3400Hz, Z_L = 600Ω	2
Battery supply (V_{BB}) rejection ratio, supply to 2-wire transverse	B_{SRT}		27		dB	See note 2; 50mV on supply, 300-3400Hz, Z_L = 600Ω	2
Battery supply (V_{BB}) rejection ratio, supply to 2-wire longitudinal	B_{SRL}		27		dB	See note 2; 50mV on supply, 300-3400Hz, Z_L = 600Ω	2
Power dissipation, active state	P_{WA}			1.00	W	Z_L = 600Ω	2
Power dissipation, active state standby state, on hook	P_{WD1}			0.35	W	I_L = 0	2

ANALOG CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions	Test level
		Min.	Typ.	Max.			
2-wire port, low freq overload level	V_{OAB}	- 3.1		+ 3.1	V	See Fig 13, note 4: V_R = (pk) 1000Hz, E_L = 0V,	3
2-wire port, longitudinal impedance	Z_{LL}			35	Ω/wire	See Fig 14: f<100Hz Z_L = 600Ω	2
Longitudinal current limit, active state	ILL_A	17.5			mA/wire (rms)	See Fig 15, note 5: E_R= -10dBm 700-1100Hz Z_L = 600Ω	3
Longitudinal current limit, disable state	ILL_S	3.6			mA/wire (rms)	See Fig 15, note 5: E_R= -10dBm 700-1100Hz Z_L=600Ω	3
Longitudinal current limit, active state, B leg	ILL_B	63			mA	I_{LLB} is Current in B leg with B leg = 0V and A leg O/C	2

ANALOG CHARACTERISTICS (continued)

Characteristic	Symbol	Value			Units	Conditions	Test level
		Min.	Typ.	Max.			
4-wire transmit port, overload level	V_{OT}	- 3.1		+ 3.1	V (pk)	See Fig 13, note 4: f = 1000 kHz, V_R=0V 4-Wire load ≥25kΩ	3
4-wire transmit port, offset voltage	V_{TOFF}	- 30		+ 30	mV	See Fig 13: V_R =0V,	2
4-wire transmit port,output impedance	Z_T			20	Ω	See Fig 13: E_L=0V,	2
Transmit (2 to 4-wire) voltage gain	G_T	- 0.1		+ 0.1	dB	See Fig 13: , E_L = 0dBu (see note 6) 1kHz , V_R = 0	2
4-wire receive port, low frequency voltage gain	G_{RL}	-0.2		+0.2	dB	See Fig 16: V_R=2.6dBu 1kHz	2
4-wire receive port, current galn	G_{RI}	59.8	60.0	60.2	dB	See Fig 13:	3
4 to 4-wire voltage gain	G_R x G_T	- 0.2		+ 0.2	dB	See Fig 16, R3 = 600kΩ V_R = 2.6dBu, 1000Hz	2
2-wire to 4-wire frequency response	F_{24}	- 0.1		+ 0.1	dB	See Fig 13, note 7: V_R = 0, E_L = 0dBu 200-3400 Hz,	2
4-wire to 2-wire frequency response	F_{42}	- 0.1		+0.1	dB	See Fig 13, note 7: E_L=0 V_R=0dBu 200-3400 Hz,	2
4 to 4-wire frequency response	F_{44} = F_{24} x F_{42}	- 0.1		+ 0.1	dB	See Fig 13, note 7: E_L=0 V_R=0dBu 200-3400 Hz,	2
Gain linearity, 2-wire to 4-wire	G_{L24-1}	-0.1		+0.1	dB	See Fig 13, note 8: V_R = 0, E_L = +7 to -30 dBu 1 kHz	3
Gain linearity, 2-wire to 4-wire	G_{L24-2}	- 0.1		+0.1	dB	See Fig 13, V_R = 0, E_L = -30 to -59 dBu, 1 kHz	3
Gain linearity, 4-wire to 2-wire	G_{L42-1}	- 0.1		+ 0.1	dB	See Fig 13, note 8: E_L = 0, V_R = +3 to -30dBu, 1 kHz	3
Gain linearity, 4-wire to 2-wire	G_{L42-2}	- 0.1		+ 0.1	dB	See Fig 13, E_L = 0, V_R = -30 to -64dBu, 1 kHz	3

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions	Test level
		Min.	Typ.	Max.			
4-wire idle channel noise (psophometric weighted)	N_{P4}			- 78.0	dBup	See Fig. 13, $E_L = V_R = 0V$	2
2-wire idle channel noise (psophometric weighted)	N_{P2}			- 78.0	dBup	See Fig. 13, $E_L = V_R = 0V$	2
2-wire differential noise (wide band)	N_{D2}		Fig. 19			See Fig. 13; $E_L = V_R = 0V$	3
2-wire longitudinal noise (wide band)	N_{L2}		Fig. 20			See Fig. 18; $E_R = 0V$	3
Regulator noise, 4-wire transmit, single frequency	N_{R4}			- 55.0	dBu	See Fig. 21,	3
Regulator noise, 2-wire transverse, single frequency	N_{RT}			- 50.0	dBu	See Fig. 21, measure V_{A-B}	3
Regulator noise, 2-wire longitudinal, single frequency	N_{RL}			- 50.0	dBu	See Fig. 21, measure V_{LL}	3
Longitudinal balance, longitudinal to transverse	B_{L-T1}	50	60		dB	See Fig. 14, note 11: $Z_L = 600\Omega$, $V_R = 0$. $E_{LL} = +$ 2dBu 40-4000 Hz	2
Longitudinal balance, longitudinal to transverse	B_{L-T2}	33.5 40.0 45.0	40.0 45.0 50.0		dB dB dB	See Fig. 14, $V_R = 0$, $Z_L = 1.6k\Omega$ $E_{LL} = +$ 2dBu 40-400 Hz $E_{LL} = +$ 2dBu 400-1000 Hz $E_{LL} = +$ 2dBu 1000-4000 Hz	2
Longitudinal balance, transverse to longitudinal + longitudinal to transverse	B_{T-L+} B_{L-T1}	98			dB	See Fig. 14 & Fig 17: $Z_L=600\Omega$, $V_R=0$, $E_{LL} = +$ 2dBu 300-800 Hz	2
Longitudinal balance, transverse to longitudinal + longitudinal to transverse	B_{T-L+} B_{L-T2}	90			dB	See Fig. 14 & Fig 17: $Z_L=1600\Omega$, $V_R=0$, $E_{LL} = +$ 2dBu 300-800 Hz	2
Longitudinal signal rejection, longitudinal to 4-wire	RJ_{L-4A}	50	60		dB	See Fig. 14: $Z_L = 600\Omega$, $V_R = 0$. $E_{LL} = +$ 2dBu 40-4000 Hz	2
Longitudinal signal rejection, longitudinal to 4-wire	RJ_{L-4BL} RJ_{L-4BH}	35 45	40 50		dB dB	See Fig. 14: $Z_L = 1600\Omega$, $V_R = 0$. $E_{LL} = +$ 2dBu 40-300 Hz $E_{LL} = +$ 2dBu 300-4000 Hz	2
Longitudinal signal generation, 4-wire to longitudinal	GN_{4-L}	40			dB	See Fig. 18: $Z_L = 600$ or $1.6k\Omega$ $E_R = 2.6$dBu f = 300-800 Hz	2
Harmonic distortion, 4 to 2-wire	T_{HD1}			- 50	dB	See Fig. 13, note 9: $V_R = 0$dBu, 100Hz	2
Intermodulation distortion	ID_{A-B1}			- 40.0	d B	See Fig . 13, note 10: $V_R = f_1 + f_2$, $f_1 = f_2 =$ - 4 to - 21 dBu,	3
50Hz intermodulation distortion	ID_{A-B2}			- 49.0	dB	See Fig 13: $V_R = f_1 +$ f2, f1 =- 9dBu 300-3400 Hz, f2 = - 23dBu 50 Hz.	3

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions	Test level
		Min.	Typ.	Max.			
Loop current, active state constant current region	I_{ACT1}	38	40	42	mA	Refer Fig. 24, note 12: Z_L = 600Ω, R_{DC} = 62.5kΩ	2
Loop current, active state	I_{ACT2}	23			mA	Refer Fig. 24, note 12: Z_L = 2kΩ, R_{DC} = 62.5kΩ	2
Loop current limit conversion factor K_{LIM} (see DC line feed section)	K_{LIM}	1.25		2.6	-	Standby mode	2
2-wire current, disconnected state	I_{DCT}			1.0	mA	LA to LB or Ground, or both LA and LB to Ground	2
2-wire current, disconnect A disable B mode	I_{DASB}			1.0	mA	Z_L = 600Ω	2
Loop current, disable state, normal (+) or reverse (-)	I_{LIM}	18.0	20.0	22.0	(±)mA	Z_L = 600Ω	2
Regulator voltage, pin 2	V_{REG1}	-31.1 -38.3		 -32.2 -39.1	V V V V	V_{LA}-V_{LB} = 18.9 V_{LA}-V_{LB} = 22.5 V_{LA}-V_{LB} = 26.9 V_{LA}-V_{LB} = 30.5	Refer to Fig. 13; V_{BAT} = -63V 2
Loop detector, current threshold	I_{TH}	I_{TH}-15%	I_{TH}	I_{TH} + 15%	A	Refer Fig. 24: I_{TH} = 350 ÷ R_{TH}	2
Ring trip detector offset voltage	V_{RTO}	- 50		+ 50	mV	See Fig. 22: R = 200kΩ V_{BB} < V_{CMM} < -2V	2
Ring trip detector bias current	I_{RTB}	-1.0			µA	See Fig. 22: I_{RTB} = $^1/_2$(I_{RTDA} + I_{RTDB})	2
Ground key active mode $\overline{DET}$ = 0	R_{G10}			900	Ω	See Fig. 23, note 1: SW1 closed, RW = 300Ω	2
Ground key active mode $\overline{DET}$ = 1	R_{G11}	10			kΩ	See Fig. 23, note 1: SW1 closed, RW = 300Ω	2
Earthcall active mode $\overline{DET}$ = 0	R_{G20}			1.7	kΩ	See Fig. 23, note 1: SW1 open, RW = 300Ω	2
Earthcall active mode $\overline{DET}$ = 1	R_{G21}	10			kΩ	See Fig. 23, note 1: SW1 open, RW = 0Ω	2
Earthcall disconnect A disable B mode, $\overline{DET}$=0	R_{G30}			1.7	kΩ	See Fig. 23, note 1: SW1 open, RW=300Ω	2
Earthcall disconnect A disable B mode, $\overline{DET}$ = 1	R_{G31}	10			kΩ	See Fig. 23, note 1: SW1 open, RW = 0Ω	2

Analog Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions	Test level
		Min.	Typ.	Max.			
Relay drivers, saturation voltage (active)	V_{SAT}	- 2			V	I = 25mA Connected to BGND	2
Relay drivers, leakage current (non-active)	I_{LK}			0.1	mA	V_{OUT}=Voltage at pin 8	2
Relay driver, clamp voltage	V_{CLMP}	V_{BAT} -2.0			V	I = 25mA into pin 4 or 5	2

NOTES
1. For polarity reversed state, L_A and L_B are reversed.
2. Figures will degrade when saturation guard is active, i.e. when $|V_{BAT}|-|V_{DCT}| < V_{SG}$. V_{DCT} is voltage between pins LA and LB and $V_{SG} \approx 15.0V$.
3. The battery voltage V_{BAT} is generally defined. The corresponding V_{BB} voltage is assumed to be 0.7V more positive than V_{BAT} allowing for the diode drop in D_2, Fig. 24.
4. Overload occurs when distortion is 2% of total signal in the range 300-3400Hz.
5. E_{LL} = 50Hz. Amplitude of I_{LL} when signal-to-distortion ratio at $V_T \leq 30dB$.
6. dBu is defined thus: 0dBu is equivalent to the voltage at 0dBm when loaded with 600Ω (= $0.775V_{RMS}$).
7. Response is measured with respect to 1 kHz.
8. Linearity is measured with respect to gain at 0dBu.
9. Distortion measured in the bandwidth 300-3400 Hz.
10. f_1 & f_2 in the range 300-3.4kHz, $f_1 \div f_2$= Non-integer. Measure ($2f_1 - f_2$) relative to f_1 or f_2 level.
11. Parameter will degrade for some values of V_{BAT}.
12. Applied V_{BAT} = -63V.

Digital Characteristics

Characteristic	Symbol	Value			Units	Conditions	Test level
		Min.	Typ.	Max.			
Input low voltage (C1 - C4, E1, CHCLK)	V_{IL}			0.7	V		2
Input high voltage (C1 - C4, E1, CHCLK)	V_{IH}	2.0			V		2
Input low current (C1 - C4, E1, CHCLK)	I_{IL}			- 0.25	mA	V_{IL} = - 0.4V	2
Input high current (C1 - C4, E1, CHCLK)	II_H			0.04	mA	V_{IH} = 2.4V	2
$\overline{DET}$ output low voltage	V_{OL}			0.4	V	I_{OL} = 0.8mA	2
$\overline{DET}$ output high voltage	V_{OH}	2.4			V	I_{OH} = 0.1mA	2
$\overline{DET}$ output, internal pull-up	R_{OUT}	10		20	kΩ		2
Propagation delay, E1 to $\overline{DET}$	t_{PD}			4	µs	$\overline{DET}$ 6.2knΩ to V_{CC} 15pF to BGND	2
Loop detector make response time	t_{LM}			5	ms	Z_L = 2kΩ (V_{OL} < 0.45)	2
Loop Detector break response time	t_{LB}			10	ms	Z_L = 2kΩ (V_{OL} > 2.35)	2
CHCLK input frequency	F_{CLK}		256		kHz		2
CHCLK min. pulse width	T_{CLK}		500		ns		3

Recommended Operating Range

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply voltage	V_{CC}	+4.75	5.0	+5.25	V	
Negative supply voltage	V_{EE}	- 4.75	- 5.0	- 5.25	V	
Battery supply voltage	V_{BAT}	- 40.5	-48	- 64	V	
Battery ground voltage	V_{BGND}	-0.1		+0.1	V	
Ambient temperature	T_{AMB}	0		+70	°C	

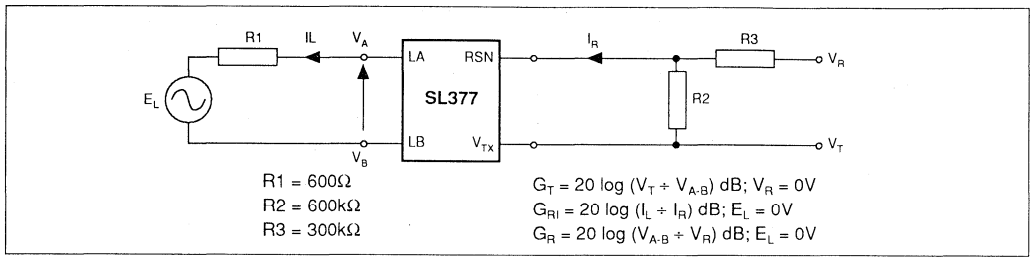


Figure 13: Test configuration (Note the SL377 block = Fig 24)

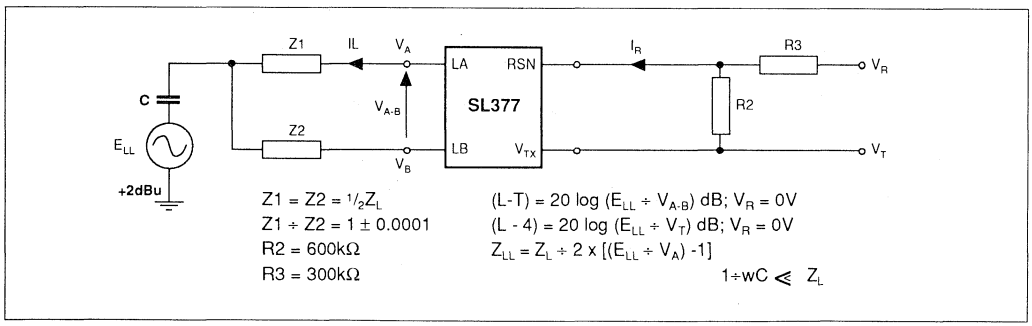


Figure 14: Test configuration (Note the SL377 block = Fig 24)

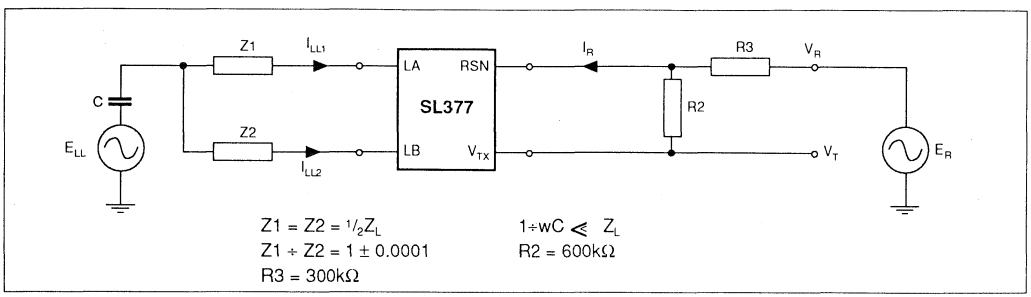
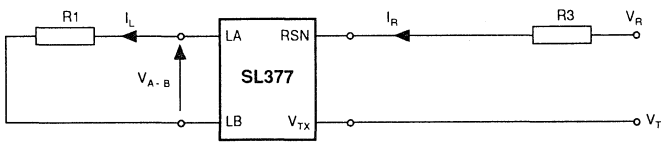
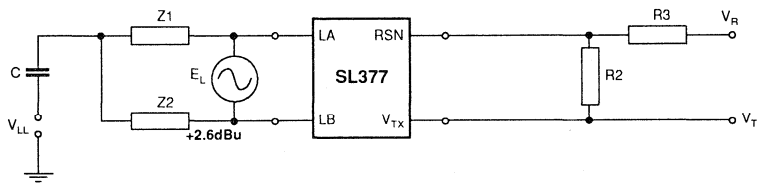


Figure 15: Test configuration (Note the SL377 block = Fig 24)



R1 = 600Ω R3 = 600kΩ $G_R = 20 \log (V_{A-B} \div V_R)$dB

Figure 16: Test configuration (Note the SL377 block = Fig 24)



EL should not be referenced to ground

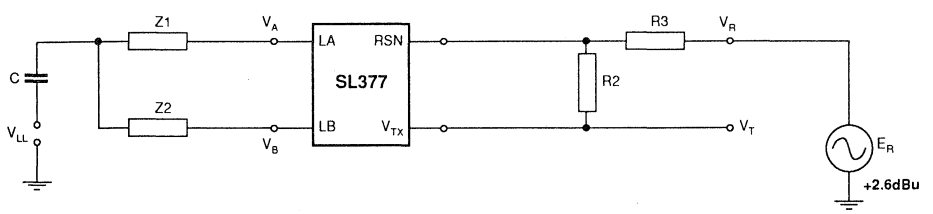
$Z1 = Z2 = {}^1/_2 Z_L$

$Z1 \div Z2 = 1 \pm 0.0001$

$(T\text{-}L) = 20 \log (E_L \div V_{LL})$dB; $V_R = 0V$

R2 = 600kΩ R3 = 300kΩ $1 \div wC \ll Z_L$

Figure 17: Test configuration (Note the SL377 block = Fig 24)



$Z1 = Z2 = {}^1/_2 Z_L$

$Z1 \div Z2 = 1 \pm 0.0001$

R3 = 300kΩ

$(4\text{-}L) = 20 \log (E_R \div V_{LL})$ dB; $V_R = 0V$

R2 = 600kΩ

$1 \div wC \ll Z_L$

Figure 18: Test configuration (Note the SL377 block = Fig 24)

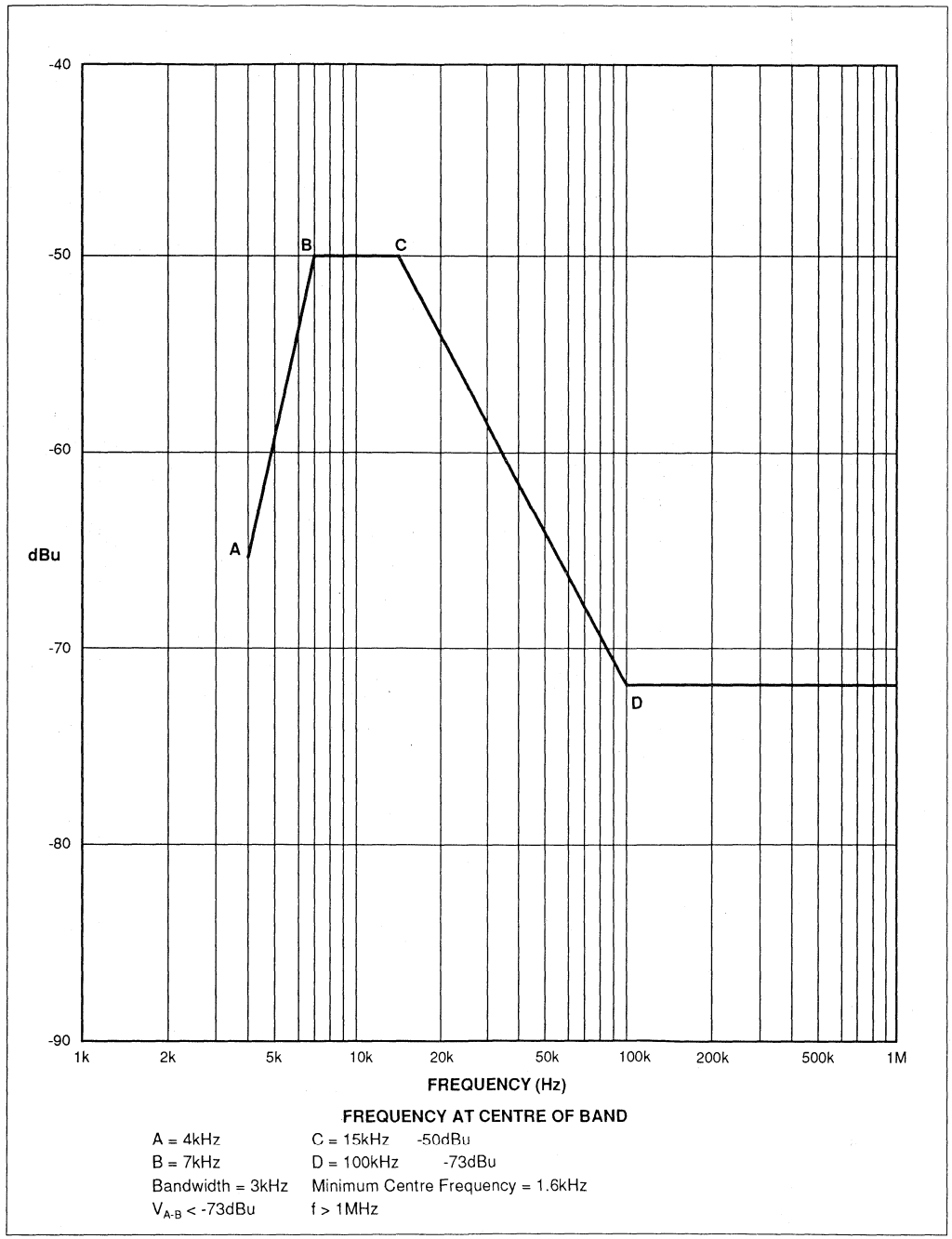
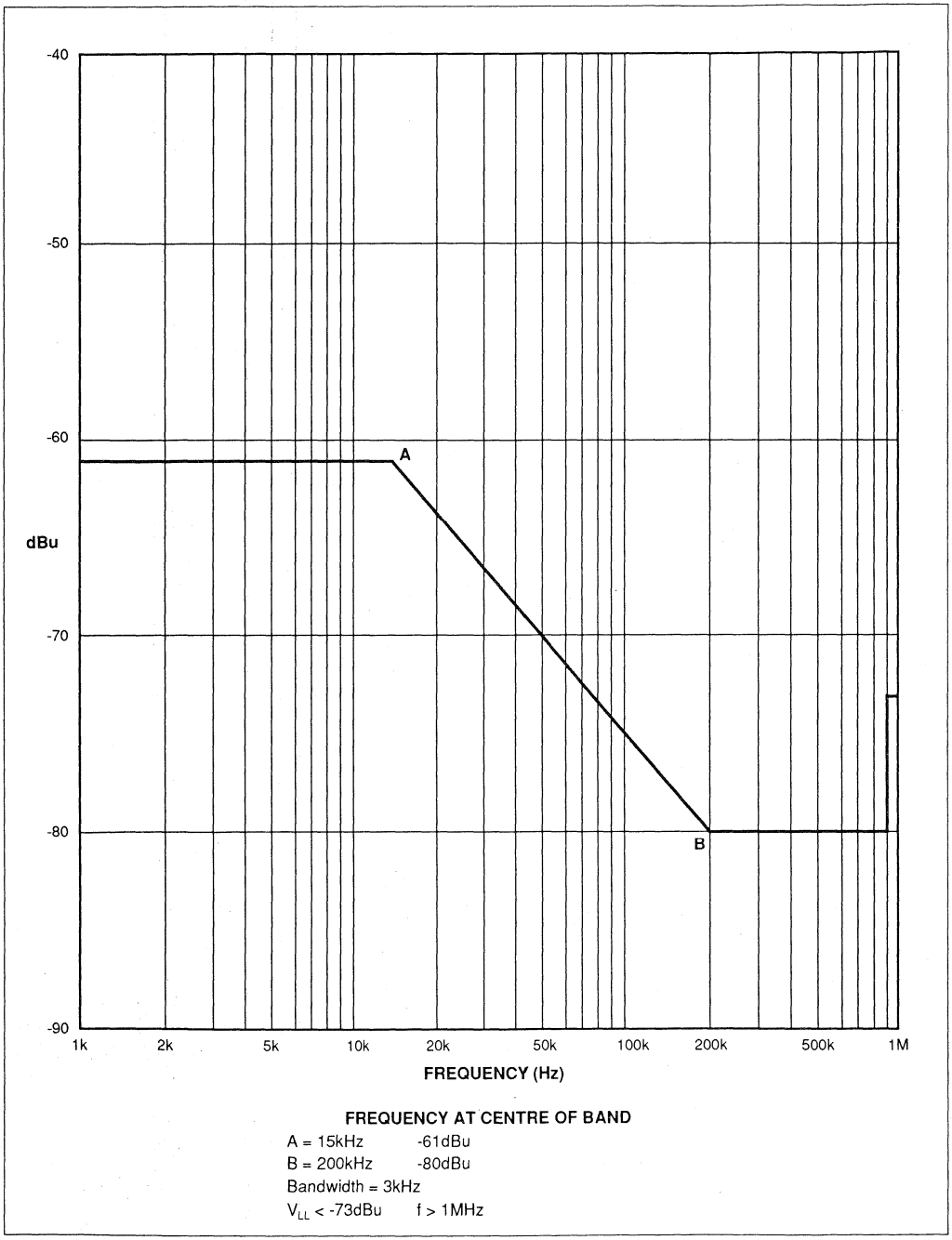


Figure 19: 2-Wire differential noise



FREQUENCY AT CENTRE OF BAND

A = 15kHz -61dBu
B = 200kHz -80dBu
Bandwidth = 3kHz
V_{LL} < -73dBu f > 1MHz

Figure 21: 2-Wire longitudinal noise

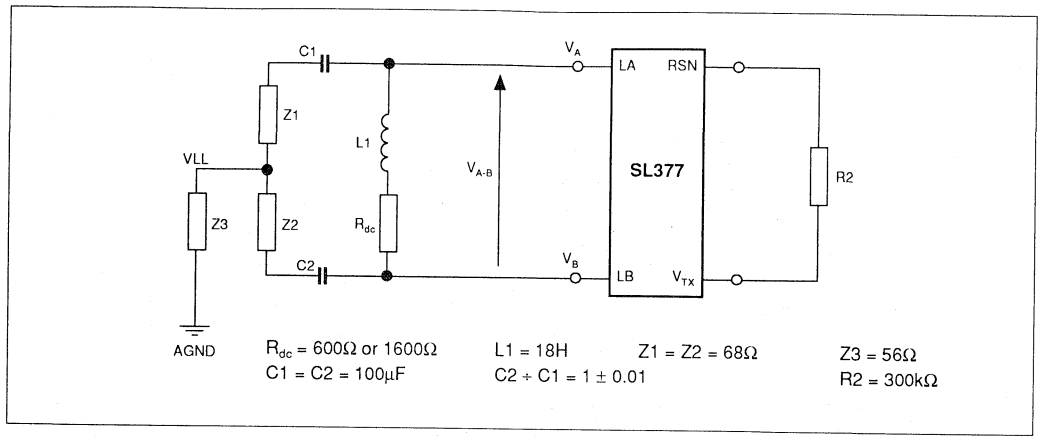


Figure 21: Test configuration (Note the SL377 block = Fig 24)

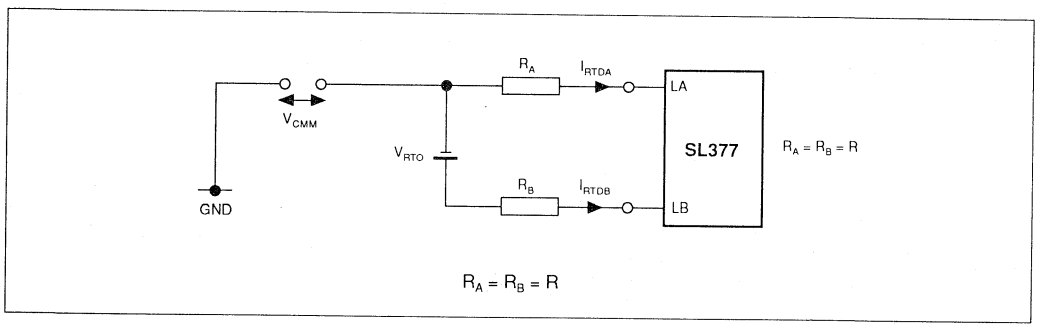


Figure 22: Test configuration (Note the SL377 block = Fig 24)

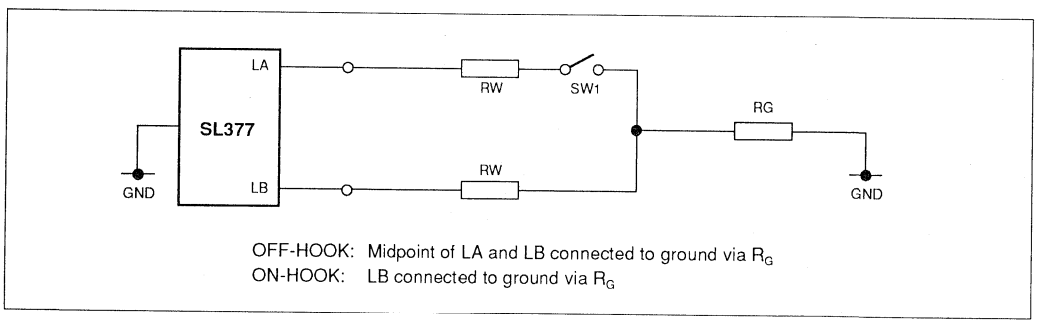
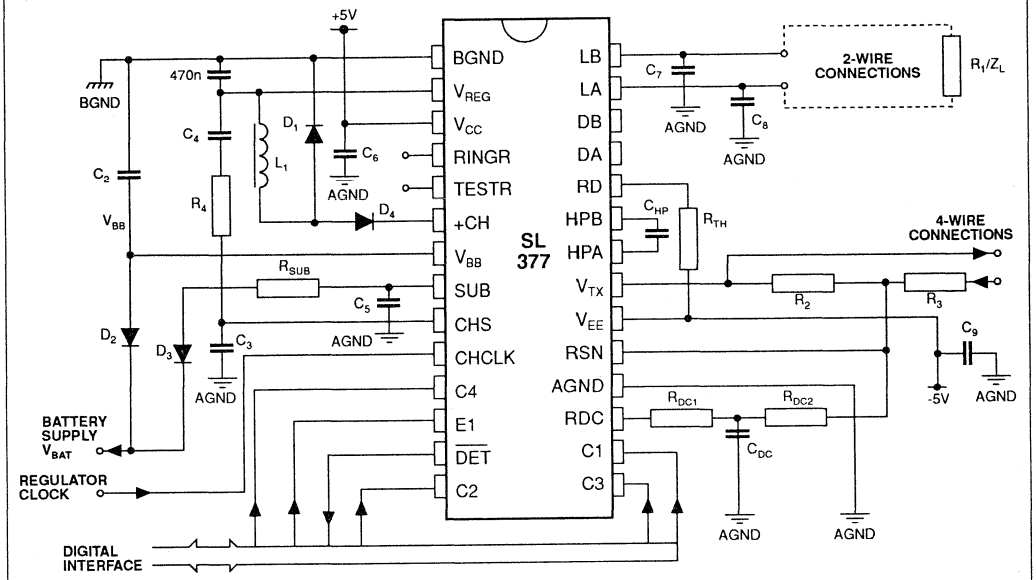


Figure 23: Test configuration (Note the SL377 block = Fig 24)



C_1 = 470n	C_6 = 100n	C_{DC} = 82n	L_1 = 1mH	R1 sa Test Configuration
C_2 = 470n	C_7 = 10n	D_1 = 100V, 100mA	R_{SUB} = 100Ω	R2 as Test Configuration
C_3 = 560p	C_8 = 10n	D_2 = 100V, 100mA	R_{TH} =32kΩ	R3 as Test Configuration
C_4 = 8.2n	C_9 = 100n	D_3 = 100V, 100mA	R_{DC1} = R_{DC2} = 31.25kΩ (See Elec. Char.)	R4 = 2.4kΩ
C_5 = 330n	C_{HP} = 330n	D_4 = 100V, 100mA	Z_L= See Electrical Characteristics	

For all tests assume AGND = BGND

Figure 24: Test circuit for Figures 13 - 18 and 21 - 23

ABSOLUTE MAXIMUM RATINGS* - Voltages are with respect to analog ground (V_{AGND}).

Parameter	Symbol	Value		Units
		Min.	Max.	
Battery supply voltage	V_{BB}	- 70	+ 1.0	V
Continuous battery ground voltage	V_{BGNDC}	- 0.3	+ 0.3	V
Intermittent (10µs) battery ground voltage	V_{BGNDI}	-4.0	+4.0	V
Positive supply voltage	V_{CC}	- 0.4	+ 7.0	V
Negative supply voltage	V_{EE}	- 7.0	+ 0.4	V
Subscriber line voltage on LA, LB or both, continuous	V_{LC}	- 70.0	+ 0.4	V
Differential DC line current	I_{LDC}		150	mA
Switched regulator voltage (off)	V_{CH}	V_{BB}	+ 1.0	V
Switched regulator current (on)	I_{CH}		150	mA
Relay drivers output voltage	V_{RLY}	V_{BAT}		V
Relay Drivers output source current	I_{RLY}		30	mA
Ring-Trip input voltage (DA or DB)	V_{RT}	V_{BB}	0	V
Ring-Trip input current (non-repetitive 10ms pulse)	I_{RT}	-10.0	+ 10.0	mA
Digital input voltage	V_{ID}	- 0.4	V_{CC}	V
Digital input current (sink)	I_{ID}		5.0	mA
Digital output voltage	V_{OD}	-0.3	V_{CC}	V
Digital output current (source)	I_{OD}		3	mA
Storage temperature	T_{ST}	- 55	+ 125	°C
Operating junction temperature †	T_{JOP}		+ 150	°C
Package power dissipation (DG28)	P_{PDG28}		1.5	W

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
† Circuit includes thermal protection such that T_{PROT} (Min) = 150°C.

SL379

SUBSCRIBER LINE INTERFACE CIRCUIT

(Replaces SL7953 Datasheet (DS2448-1.0))

The SL379 is a Subscriber Line Interface Circuit (SLIC) for use at the telephone exchange or PABX end of a telephone line.

It provides power feed, transmits and receives voice signals, controls ringing and detects Ground Key or Off-Hook conditions. These functions can be programmed to provide the flexibility required for different telephone networks.

The SL379 is fabricated using bipolar technology.

FEATURES

- Optimised for 48V battery
- Low Power Line Feed via Regulator
- Programmable Constant Current Feed Independent of Battery, to Line
- Programmable AC Termination Impedance
- Good Longitudinal Balance
- Ground Key and Ring Trip Detection
- Programmable Off-Hook Detection
- Disconnect and Low Power disable Modes
- A-Leg Disconnect, B-Leg disable Mode
- Normal or Reversed Line Polarity Operation
- Test/Ring Relay Drivers
- Thermal Shut-Down Protection
- Industry Standard pin-out
- ESD protection†

† ESD precautions must be observed

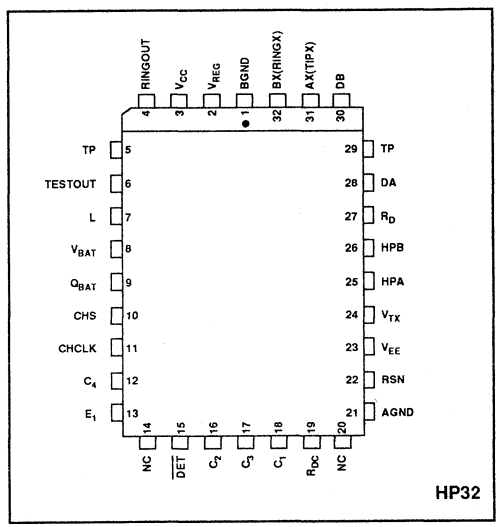


Fig.1 Pin connections - top view
(Note1: Pin 1 is marked for orientation)

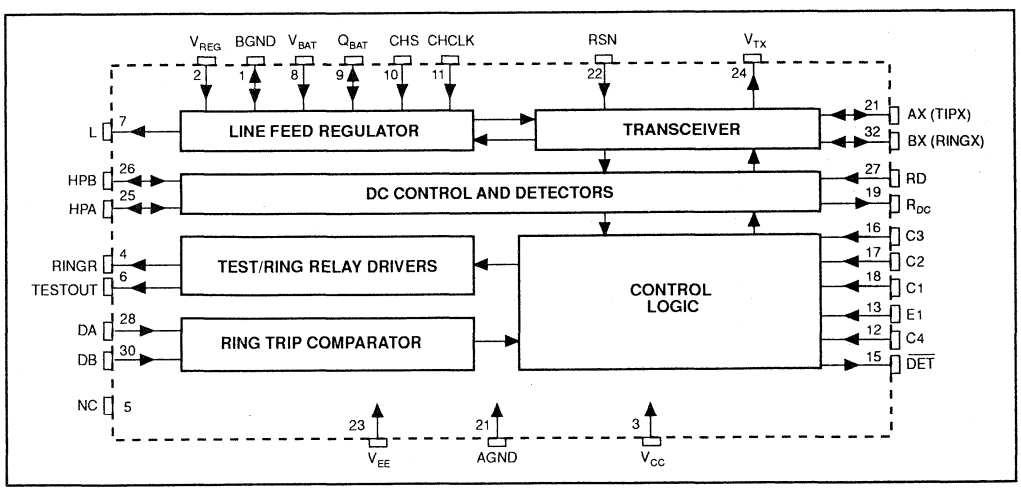


Fig.2 Functional block diagram

Pin Name	Pin Function	Pin Description
AGND	Ground	Analog (Quiet) ground.
AX(TIPX)	(Output)	Output of a A(TIP) power amplifier.
BGND/DGND	Ground	Battery (power) ground / digital ground.
BX(RINGX)	(Output)	Output of B(RING) power amplifier.
C3 - C1 Decoder	(Inputs)	TTL compatible. C3 is MSB and C1 is LSB.
C4	Test Relay Driver Command	TTL compatible. A logic low enables the driver.
CHCLK	Chopper Clock (Input)	Input to switching regulator (TTL compatible). Frequency = 256kHz (Nominal).
CHS	Chopper Stabilization (Input)	Connection for external stabilization components.
DA	Ring Trip Negative (Input)	Negative input to ring trip comparator.
DB	Ring Trip Positive (Input)	Positive input to ring trip comparator.
$\overline{\text{DET}}$	Detector (Output)	When enabled, a logic low indicates that the selected detector is tripped. The detector is selected by the logic inputs (C3 - C1, E1). The output is open-collector with a built-in 15K pull-up resistor.
E1	Ground Key Enable (Input)	E1 = high connects the ground-key detector to DET, and E1 = low connects the off-hook or ring trip detector to DET.
HPA		A(TIP) side of high-pass filter capacitor.
HPB		B(RING) side of high-pass filter capacitor.
L	Switching Regulator Power Transistor (Output)	Connection point for filter inductor and anode of catch diode. This pin will have up to 60V of pulse waveform on it and must be isolated from sensitive circuits. Extreme care must be taken to keep the diode connections short because of the high currents and high di/dt.
Q_{BAT}	Quiet Battery	Filtered battery supply for the signal processing circuits.
R_D		Threshold modification and filter point for the off-hook detector.
R_{DC}		Connection point for the DC feed current programming network connects to the Receiver Summing Node (RSN). The sign of V_{RDC} is minus for normal polarity and plus for reverse polarity.
RINGOUT	Ring Relay Driver (Output)	Sourcing from BGND.
TESTOUT	Test Relay Driver (Output)	Sourcing from BGND.
TP		Thermal conduction pin. Tied to substrate. Leave isolated or connect to Q_{BAT}.
RSN	Receive Summing Node (Input)	The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 1000 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node. This node is extremely sensitive. Care should be taken to route the 256kHz chopper clock and switch lines away from the RSN node.
V_{BAT}		Connected to Office battery supply through an external protection diode.
V_{CC}		+5V power supply.
V_{EE}		-5V power supply.
V_{REG}	Regulated Voltage (Input)	Provides negative power supply for power amplifiers and connection point for inductor, filter capacitor and chopper stabilization.
V_{TX}	(Transmit Audio (Output)	This output is a unity gain version of the AX(TIPX) and BX(RINGX) metallic voltage. The other end of the two-wire input impedance programming networks connects here.

ELECTRICAL CHARACTERISTICS

DESCRIPTION	TEST CONDITIONS	Test Level (Note 8)	PRELIMINARY			Units	Comments
			Min	Typ	Max		
Analog (V_{TX}) Output Impedance		3		3.0	20	Ohm	
Analog (V_{TX}) output Offset		1	-30		+30	mV	
Longitudinal Impedance at AX or BX	300Hz to 3.4kHz	3			35	Ohm	
Overload level, 2 wire = 600 to 900Ω	four-wire two-wire	1	-3.1		+3.1	Vpk	See Note 2
Longitudinal Balance (two-wire and four-wire, see Test Circuit (c)							
RL = 600Ω, Longitudinal to Metallic L-T, L-4	300Hz to 3400Hz	1	50			dB	
Longitudinal signal generation 4-L	300Hz to 800Hz	1	40			dB	
Longitudinal current capability per wire (RMS)	Active State	1	17.5			mA	
	Disable State	1	3.6				
Active B Leg only DC (RMS)		1	63			mA	See Note 4
Insertion Loss (two-wire to four-wire and four-wire to two-wire, see Test Circuits A and B)							
Gain Accuracy 4 - 2	0dBm, 1kHz	1	-0.15		+0.15	dB	
2 - 4		1	-0.1		+0.1	dB	
Gain Tracking	0 to -55dBm	3	-0.15		+0.15	dB	See Note 5
Variation with Frequency	300Hz to 3400Hz to 1kHz	1	-0.1		+0.1	dB	See Note 3
Balance Return Signal (four-wire to four-wire, see Test Circuit B)							
Gain Accuracy	0dBm, 1kHz	1	-0.2		+0.2	dB	See Note 3
Variation with Frequency	300Hz to 3400Hz to 1kHz	1	-0.1		+0.1	dB	See Note 3
Total Harmonic Distortion (two-wire to four-wire or four-wire to two-wire, see Test Circuits A and B)							
Total Harmonic Distortion	0dBm, 300Hz-3.4kHz	1			-50	dB	
Idle Channel Noise							
Psophometric Weighted Noise	Two-wire	1			-78	dBu	See Note 6
	Four-wire	1			-78	dBu	
DC Feed Currents - Battery = -48V							
Active Mode Loop Current Accuracy	ILOOP (nominal) = 40mA	1	-7.5		+7.5	%	
Disable Mode	R_L = 600Ω	1	18	20	22	mA	
Disconnect A, Disable B Mode	R_L = 600Ω	1			1.0	mA	
Disconnect Mode	R_L = 0Ω	1			1.0	mA	
Power Dissipation - Battery = -48V, Normal Polarity							
On-Hook Disable Mode		1			350	mW	
Off-Hook Active Mode	R_L = 600Ω	1			1000	mW	

DESCRIPTION	TEST CONDITIONS	Test Level (Note 8)	PRELIMINARY			Units	Comments
			Min	Typ	Max		
Supply Currents							
V_{CC} On-Hook Supply Current	Disconnect Mode	1			4.5	mA	
	Disable Mode	1			10	mA	
	Active Mode	1			12	mA	
V_{EE} On-Hook Supply Current	Disconnect Mode	1			2.3	mA	
	Disable Mode	1			3.5	mA	
	Active Mode	1			4	mA	
V_{BAT} On-Hook Supply Current	Disconnect Mode	1			1	mA	
	Disable Mode	1			5	mA	
	Active Mode	1			6	mA	
Power Supply Rejection Ratio (Vripple = 50mV RMS)							
V_{CC}	1kHz	1		49	30	dB	See Note 6
V_{EE}	1kHz	1		49	30	dB	See Note 6
V_{BAT}	1kHz	1		42	30	dB	See Note 6
Off-Hook Detector							
Current Threshold Accuracy	$I_{DET} = 365/R_D$ Nominal	1	-20		+20	%	
Ground-Key Detector Thresholds, Active Mode (See Test Circuit F)							
Ground-Key Resistance Threshold	B(RING) to GND	1	2	5.0	10	kohm	
Ring Trip Detector Input							
Bias Current		1	-1			µA	
Offset Voltage		1	-50	0	+50	mV	
Logic Inputs (C1, C2, C3, C4, E1 and CHCLK)							
Input High Voltage		1	2.0			V	
Input Low Voltage		1			0.7	V	
Input High Current		1			4.0	µA	
Input Low Current		1	-0.4			mA	
Logic Output (DET)							
Output Low Voltage	IOUT = 0.8mA	1			0.4	V	
Output High Voltage	IOUT = -0.1mA	1	2.4			V	
Switch Hook Detect Mode RL = 600 Ohms (See Test Circuit G)							
E1 Low to DET Low		1			4	µS	
E1 Low to DET High		1			4	µS	

SLIC DECODING

STATE	C3	C2	C1	TWO-WIRE STATUS	DET OUTPUT E1 = 0	DET OUTPUT E1 = 1
0	0	0	0	Disconnect		
1	0	0	1	Ringing	Ring Trip	Ring Trip
2	0	1	0	Active	Loop DET	Ground Key
3	0	1	1	Disable	Loop DET	Ground Key
4	1	0	0	Disconnect A, Disable B	Loop DET	
5	1	0	1	Reserved		
6	1	1	0	Active Polarity Reversal	Loop DET	Ground Key
7	1	1	1	Disable Polarity Reversal	Loop DET	Ground Key

DESCRIPTION	TEST CONDITIONS		PRELIMINARY Min	PRELIMINARY Typ	PRELIMINARY Max	Units	Comments
Relay Driver Outputs (RINGOUT, TESTOUT)							
On Voltage	30mA Source		BGND -2	BGND -0.95		V	
Off Leakage				0.5	100	µA	
Clamp Voltage	30mA Sink		Q_{BAT} -2.5			V	

NOTES:

1. Unless otherwise noted, test conditions are: Battery = -48V, V_{CC} = 5V, V_{EE} = -5V, R_L = 600 Ohms, C_{HP} = 0.22µF, R_{DC1} = R_{DC2} = 31.25k, C_{DC} = 0.1µF, R_S = 51.1k, no fuse resistors, two-wire AC output impedance, programming impedance (Z_T) = 600k resistive, receive input summing impedance (Z_{RX}) = 300k resistive. Parameters are measured at nominal 20°C but are guaranteed by characterisation between 0 and 70°C.
2. Overload level is defined when THD = 1%.
3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This spec. assumes that the two-wire AC load impedance matches the impedance programmed by Z_T.
4. Current from B leg to ground through 600 Ohm resistor with A leg open circuit.
5. Not tested in production. This parameter is guaranteed by characterisation or correlation to other tests.
6. When the SLIC is in the Anti-Sat 2 operating region, this parameter will be degraded. The exact degradation will depend on system design. The Anti-Sat 2 region occurs at high loop resistances when [V_{BAT}]-[V_{AX}-V_{BX}] is less than approximately 15V.
7. ESD withstand > 1.5kV all pins.
8. Test Levels
   - Level 1 - 100% production tested at 25°C.
   - Level 2 - 100% production tested over full temperature range.
   - Level 3 - Parameter guaranteed by characterisation or design.
   - Level 4 - Parameter is typical only.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-55°C to +150°C
V_{CC} with respect to AGND	-0.4V to +6.5V
V_{EE} with respect to AGND	+0.4V to -6.5V
V_{BAT} with respect to AGND	-0.4V to -70V
Maximum rate of rise (dV/dt) to V_{BAT} when a 0.33µF Q_{BAT} bypass capacitor is used	27V/µs
AGND with respect to BGND	±0.3V
AX(TIPX) or BX(RINGX) to BGND: Continous	-70V to +1.0V
Current from AX(TIPX) or BX(RINGX)	±150mA
Voltage on RINGOUT	V_{BAT} to +0.7V
Voltage on TESTOUT	V_{BAT} to +0.7V
Current through relay drivers or internal driver catch diodes	30mA
Voltage on ring trip inputs DA and DB	V_{BAT} to 0V
Current into ring trip inputs	±10mA
Peak current into regulator switch (L pin)	150mA
C1, C2, C3, C4, E1, CHCLK to AGND	-0.4V to V_{CC}
Maximum power dissipation	T_A = 70°C
In 32-pin PLCC package	1.15W

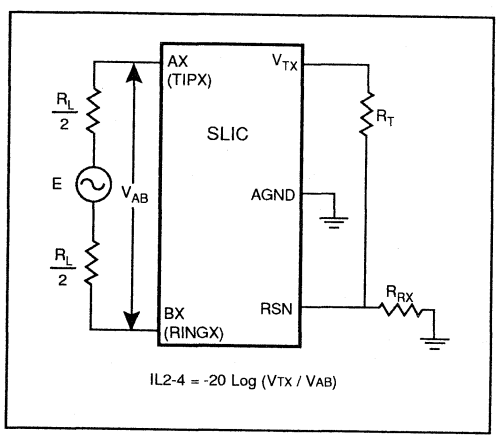
Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 150°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

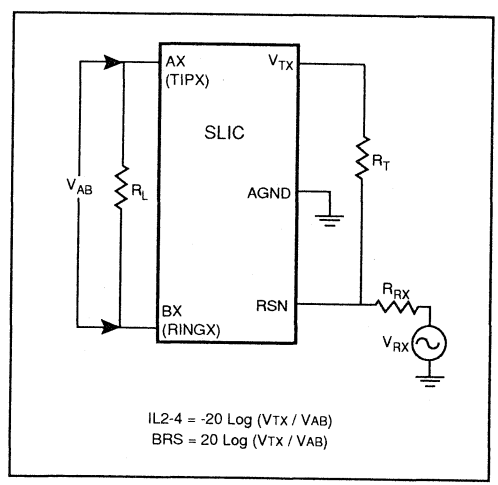
OPERATING RANGES

Ambient temperature (T_A)	0°C to +70°C
Supply Voltage (V_{CC})	4.75V to 5.25V
V_{EE}	-4.75V to -5.25V
V_{BAT}	-40.5 to -64V
AGND	0V
BGND with respect to AGND	-100mV to +100mV
Load Resistance on V_{TX} to ground	10k Ohm minimum

TEST CIRCUITS

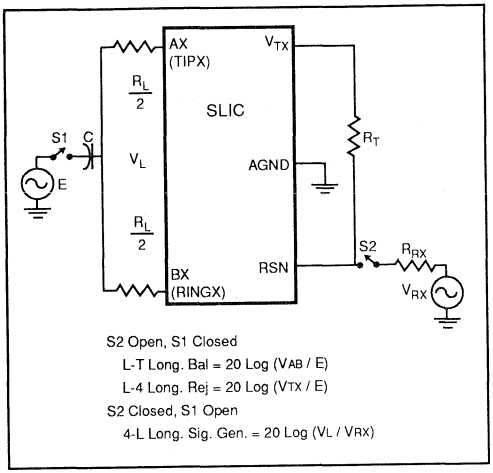


Test Circuit A: Two-to-four wire insertion loss

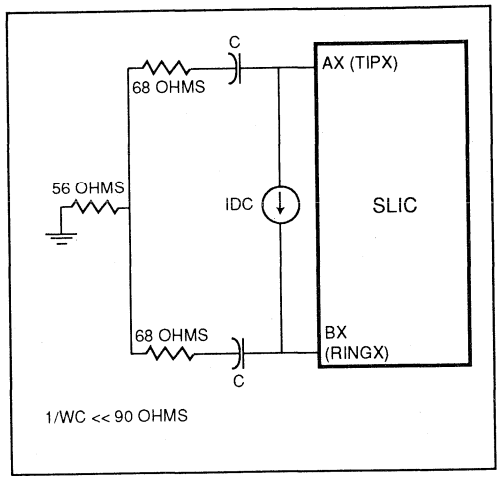


Test Circuit B: Four-to-two wire insertion loss and balance return signal

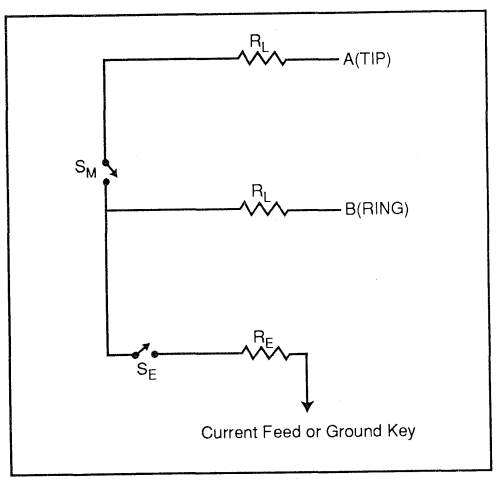
TEST CIRCUITS



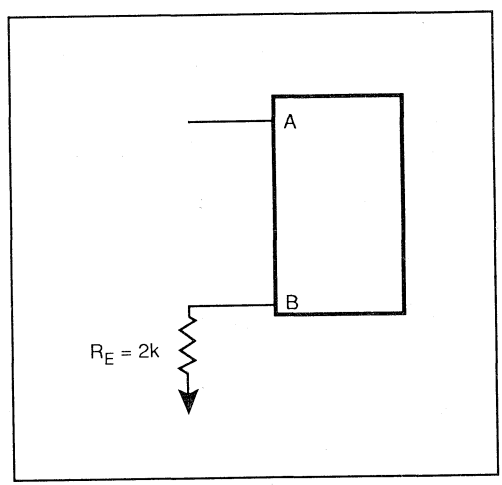
Test Circuit C: Longitudinal Balance



Test Circuit E: Single - Frequency Noise



Test Circuit F: Ground - Key Detection



Test Circuit G: Ground - Key Switching

MV3010-1

SUBSCRIBER LINE AUDIO CIRCUIT

The MV3010-1 is a Subscriber Line Audio Circuit (SLAC) for use in subscriber line cards in telephone exchanges or similar equipment.

It performs A/D and D/A conversion, adjusts the gain and frequency response for both the transmit and receive paths and performs echo suppression by automatically cancelling any content of the receive signal from the transmit path. The device also allows line card control and monitoring facilities via digital I/O pins. High performance is ensured through the use of DSP techniques implemented in CMOS technology.

The MV3010-1 meets or exceeds all CCITT G714 specifications over a range of programmable gains to 13dB.

The adaptive echo cancellation algorithm used ensures completely robust performance to a complete range of likely near and far end signal sources.

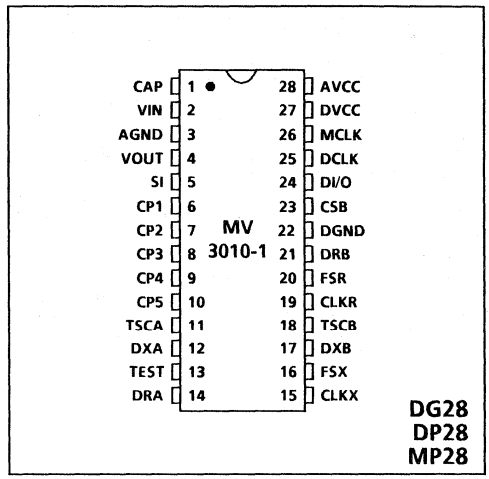


Fig.1 : MV3010-1 Pin Connections - top view.

FEATURES

- Adaptive Echo Cancellation (Hybrid Balance).
- Programmable Filters and Gain Control.
- Selectable for μ-Law, A-Law or Linear Codes.
- Programmable Line Control Interface.
- Programmable Time Slot and Clock Offset Assignments.
- Power Down Mode - Low Standby Power.
- On-chip Reference Voltage.
- Meets/exceeds CCITT and AT&T Specifications
- 2048kHz and 1544kHz PCM operation.

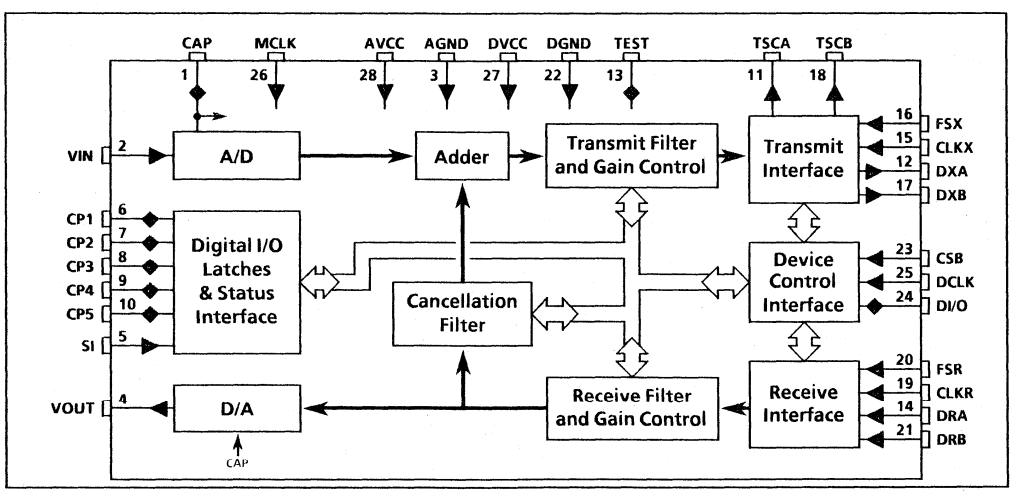


Fig. 2 : Functional Block Diagram.

FUNCTIONAL DESCRIPTION

OVERVIEW

The MV3010-1 Subscriber Line Audio Circuit performs the coding, decoding, filtering, echo cancellation and line supervision functions which are required for the subscriber line interface in a digital PABX or Central Office. It can be easily interfaced with any of the SL37X or SL79XX Subscriber Line Interface Circuits (SLIC) to provide a complete subscriber line interface/line card, supporting all of the BORSCHT functions.

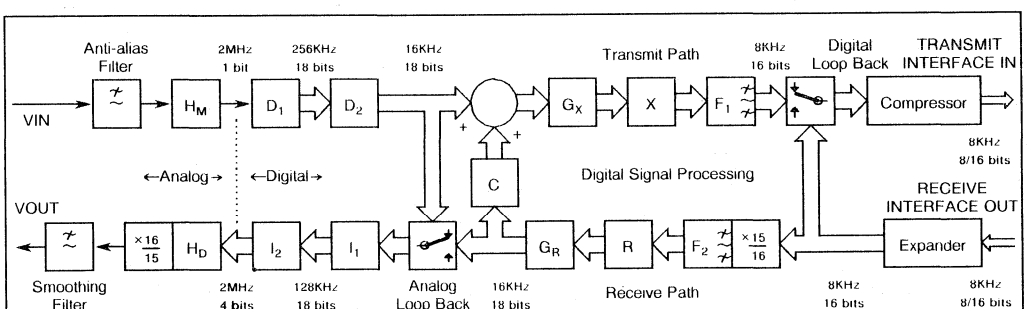
The MV3010-1 (Fig 2) samples the signal at VIN, pin 2, and provides companded or linear coded PCM samples, depending on programming (see Control and Monitoring section), at the DXA or DXB output pins. This is referred to as the Transmit direction. The Receive direction performs the opposite conversion, taking companded or linear PCM samples from the DRA or DRB pin and providing an analog signal at VOUT, pin 4. For both of the Transmit and Receive directions, the overall gain, frequency response, clock rate and PCM time slot assignment can be dynamically adjusted by virtue of the DSP structure of the MV3010-1. Also included is an automatically adaptive/static Trans-Hybrid filter (C Filter) for cancellation of any VOUT signal present at the VIN pin.

The serial Device Control Interface provides complete control and monitoring for all the MV3010-1 operating modes and functions, which are now described in more detail in the following sections.

RECEIVE PATH

PCM encoded signals are received on either the DRA pin or the DRB pin, depending on programming (see Control and Monitoring section). Bit and frame synchronisation are established by the CLKR clock and FSR pulse as described in the PCM Interface section, but will always consist of PCM samples at a basic 8KHz rate. Thus the PCM interface passes 16 bit, 8KHz samples into the receive path of the MV3010-1 DSP, as shown in figure 3. PCM samples are first expanded from A-Law or μ-Law, if necessary, before being passed through CCITT/AT&T filters, F_2. At this point samples may be switched into the transmit path to provide digital loop back (see Control and Monitoring section). Data is now interpolated from 16 to 18 bit samples running at 16KHz for the internal DSP, which now introduces an optional programmable Receive Filter, R. A 15/16 gain factor compensates for the D/A gain to restore a nominal receive gain of 0dB.

The Receive Filter is a 4 tap FIR type structure (16KHz taps) and can be used to modify the frequency response of the receive path. This might be used to adjust the overall frequency response, that may be affected by components of the external analog circuitry (e.g. 2 to 4 wire conversion) associated with VOUT. Dynamic programming and enable/disable of the filter can be achieved via the Control Interface. Note that disabling of the filter does not alter the programmed coefficients, which may be entered when the filter is in either state. This filter is described more fully in the Transmit and Receive Filters section.



FUNCTION	NAME	DESCRIPTION
A/D Conversion	H_M	A/D Conversion to 2MHz 1 bit
Decimation Filters	D_1	Triangularly Weighted FIR 2MHz→256KHz
Decimation Filters	D_2	'Imperial college' 256KHz→16KHz
Transmit Gain adjust	G_X	One Tap FIR, -∞ to +15.6dB, user programmable
Transmit Filter	X	Four Tap FIR, user programmable
CCITT/AT&T Filters	F_1	'Imperial college' - Decimation 16KHz→8KHz, 4KHz low pass, 50/60Hz Notch and DC reject Filters
CCITT/AT&T Filters	F_2	'Imperial college' - Interpolation 8KHz→16KHz, 4KHz low pass Filter and DC reject Filter
Receive Filter	R	Four Tap FIR, user programmable
Receive Gain adjust	G_R	One Tap FIR, -∞ to +6dB, user programmable
Cancellation Filter	C	9 Tap FIR + 10th TAP IIR - Adaptive, user programmable
Interpolation Filters	I_1	'Imperial college' 16KHz→128KHz
Interpolation Filters	I_2	Sample/Hold 128KHz→2MHz
D/A Conversion	H_D	D/A Conversion and multiply by 16/15

Fig. 3 : MV3010-1 Signal Processing Flow.

Following the Receive Filter is a gain stage (G_R) which can be used to adjust the overall Receive Gain of the receive path. Note that it does not have any other effect on the receive signal (frequency response or phase) other than an absolute adjustment of gain. G_R is set to 0dB (×1.0) at first application of power to the device, and can be dynamically programmed via the Control Interface. Coefficient values to adjust the Receive Gain in steps of 0.5dB are given in Table 1, and described further for other increments in Table 9.

At this point, the samples are fed in two separate directions. Firstly, they are passed to the C Filter for echo cancellation (Trans-Hybrid balance) in the Transmit Path, and secondly to the Interpolation Filters I_1 and I_2.

The C Filter is a 9 Tap FIR type filter (16KHz) plus a 10th Tap recursive IIR stage, and is described more fully in the C Filter section. It can be enabled and disabled in the same way as for the Transmit/Receive Filters, via the Control Interface. Additionally it has an adaptive mode to self adjust the cancellation according to changing conditions of the 4 wire interface (see C Filter section).

The internal sample format of 18 bits, 16KHz, is interpolated to 4 bit, 2MHz, in two stages by I_1 and I_2. Alternatively, samples may be switched in from the transmit path, to I_1, providing an Analog Loop Back mode (see Control and Monitoring section). D/A conversion, H_D introduces a gain of 16/15. The smoothing filter reduces noise and signal harmonics resulting in an output at VOUT (pin 4) of up to 3V p-p (+1.5/–1.5) biased at a DC level of V_{OO} (≈2.5V). The DC level is a consequence of the single (split analog and digital rails) +5.0V supply. The output stage, shown in figure 4a, can be coupled to a SLIC or other line interface circuitry. This is discussed further in the Applications section.

TRANSMIT PATH

The Transmit path, figure 3, begins at the VIN pin (pin 2). Analog input can be up to 6Vp-p about ground (+3.0V/–3.0V) despite the single +5.0V supply. The input stage is shown in figure 4b. Note that when left open circuit, the VIN pin biases to ≈1.66V. To maintain dynamic range of the input, the driving output should therefore have a low output impedance, to restore a ground centre point (removal of any DC bias at VIN is also necessary to prevent disabling of C Filter adaption - see separate section). The signal is now digitised using an over-sampling technique running at 1 bit, 2MHz, before being passed to the decimation stages D_1 and D_2. An anti-alias filter prevents harmonics above the sample rate from being aliased back down into the pass band.

Decimation stages D_1 and D_2 produce an 18 bit, 16KHz, sample rate for internal use by the MV3010-1 DSP, as for the Receive Path. Output from D_2 can be switched into the receive path to provide an Analog Loop Back function (see Control and Monitoring section). After this stage, samples from the Receive Path are added, via the C Filter, into the Transmit path. This is because in the intended application of a high quality Line Card/COMBO device, the analog input may contain some of the analog output of the MV3010-1, due to the echo return of the 2 to 4/4 to 2 wire conversion (performed externally to the MV3010-1). Any such content of the received signal is now attenuated by this added signal. Such use of the C Filter is described in more detail in later sections.

Following this, the Transmit signal now passes through three stages that act in a similar manner to that of the Receive side. Firstly a gain stage, G_X, provides overall adjustment of the Transmit Gain. This can be carried out in 0.5dB steps, as given in Table 1, or given other values as shown in Table 9.

Secondly, the samples now pass through a 4 Tap FIR Filter section (X) which is identical in form to the R Filter of the Receive side. The X Filter can be used to correct for phase/frequency errors in the Transmit Path, is dynamically programmable and can be disabled/enabled as for the R Filter.

Lastly, the 18 bit, 16KHz, samples are now decimated further to 8KHz by the F1 stage which provides CCITT/AT&T filters, in addition to 50/60Hz and DC reject filtering, which may be disabled via the Control Interface.

Before being passed to the PCM interface for output, the signal may be compressed to 8 bit A Law or μ Law PCM coding (Tables 2 and 3) or remain 16 bit linear (Table 4), as programmed via the Control Interface. The compressor can be switched to take samples from the receive path to provide a Digital Loop Back mode (see Control and Monitoring section). The PCM Interface outputs the samples at a basic 8KHz rate as defined by FSX (pin 16). The clock rate may be from 64KHz to 4096KHz in integral steps of 64KHz, as described further in the PCM Interface section.

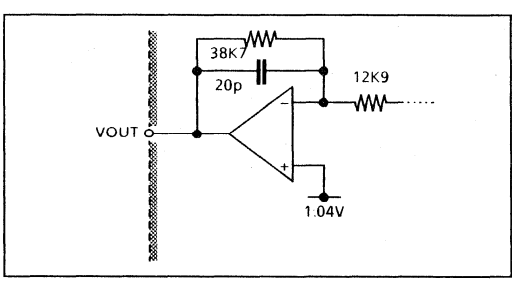


Fig. 4a : MV3010-1 VOUT circuitry.

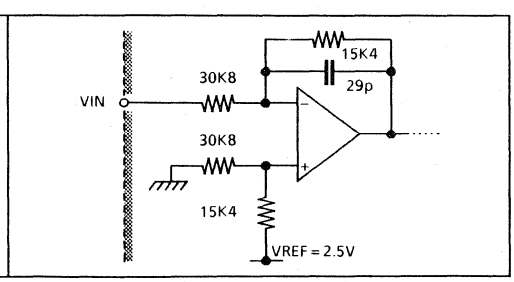


Fig. 4b : MV3010-1 VIN circuitry.

G_X (dB)	Hex Code	G_X (dB)	Hex Code	G_X (dB)	Hex Code	G_X (dB)	Hex Code
+12.0	9F-D8	+6.0	FF-F8	0.0	F0-80	–6.0	E8-84
+11.5	9C-90	+5.5	FE-90	–0.5	EF-8C	–6.5	E7-C8
+11.0	98-E4	+5.0	FC-B8	–1.0	EE-A0	–7.0	E7-94
+10.5	95-CC	+4.5	FA-F0	–1.5	ED-BC	–7.5	E6-E0
+10.0	92-CC	+4.0	F9-AC	–2.0	EC-DC	–8.0	E6-B0
+9.5	8F-E4	+3.5	F7-F8	–2.5	EC-80	–8.5	E6-80
+9.0	8D-8C	+3.0	F6-CC	–3.0	EB-A8	–9.0	E5-D8
+8.5	8A-C8	+2.5	F5-AC	–3.5	EA-D8	–9.5	E5-B0
+8.0	88-98	+2.0	F4-94	–4.0	EA-8C	–10.0	E5-88
+7.5	85-F8	+1.5	F3-84	–4.5	E9-C4	–10.5	E4-E4
+7.0	83-E8	+1.0	F1-F8	–5.0	E9-80	–11.0	E4-C0
+6.5	81-E8	+0.5	F0-F8	–5.5	E8-C0	–11.5	E4-A0
						–12.0	E4-84

Transmit Gain Coefficients. *

G_R (dB)	Hex Code	G_R (dB)	Hex Code	G_R (dB)	Hex Code
+6.0	BF-EC	0.0	A0-80	–6.0	90-84
+5.5	BC-A4	–0.5	9E-9C	–6.5	8F-94
+5.0	B8-F4	–1.0	9C-C4	–7.0	8E-A4
+4.5	B5-DC	–1.5	9A-F8	–7.5	8D-C0
+4.0	B2-DC	–2.0	99-B4	–8.0	8C-E0
+3.5	AF-F0	–2.5	98-80	–8.5	8C-84
+3.0	AD-98	–3.0	96-D4	–9.0	8B-AC
+2.5	AA-D8	–3.5	95-B0	–9.5	8A-DC
+2.0	A8-A4	–4.0	94-98	–10.0	8A-90
+1.5	A6-84	–4.5	93-88	–10.5	89-C8
+1.0	A3-F4	–5.0	92-80	–11.0	89-84
+0.5	A1-F4	–5.5	91-80	–11.5	88-C0
				–12.0	88-84

Receive Gain Coefficients . *

* Note: Smaller steps are possible - see Table 9.

Table 1 : Transmit and Receive Gain Coefficients for 0.5dB step adjustments .

PCM INTERFACE

The PCM Interface of the MV3010-1 consists of the pins DXA, DXB, CLKX, FSX, TSCA and TSCB for the Transmit output and pins DRA, DRB, CLKR and FSR for the Receive input. Figures 5 and 6 give the basic timing diagrams for Transmit and Receive directions. Note that in both cases the sample rate is set by the respective frame sync pulse (FSX/FSR) at 125µs (8KHz) intervals. This defines the length of the PCM frame which remains unchanged at all times.

For the PCM Transmit output, the FSX pulse is identified about a negative edge of CLKX, which also defines the start of the first bit (bit 1, msb) of the first 8 bit (for companded codes) or 16 bit (for linear code) sample of the frame. The MV3010-1 can be programmed to place the 8/16 bit sample in any 8 bit Time Slot of the frame. For 16 bit samples, the sample is moved by multiples of 8 bits, so that a minimum of two Time Slots are needed between any adjacent (multiplexed with other MV3010-1s) samples of the PCM frame (an offset of 8 bits is still valid). In addition, the position of all Time Slots relative to the FSX pulse can be offset by from 0 to 7 clock periods of CLKX (Clock Offset). The Time Slot and Clock Offset are dynamically programmable via the device Control Interface.

The number of Time Slots that can be in any one frame, and hence also the data rate, depends on the frequency of the data clock, CLKX. There must be at least one 8 bit Time Slot in the frame (two 8 bit Time Slots will be required for 16 bit samples), the maximum number being thirty two 8 bit Time Slots (64 for expanded mode - described later). The frequency of CLKX can therefore vary between 64KHz and 4096KHz depending on the number of Time Slots required. The number of Time Slots, N_{TS}, that are in the frame is determined by the relationship:-

$$N_{TS} = CLKX \div 64K$$

where CLKX is between 64K and 2048KHz (4096KHz expanded) in 64K steps (from 128KHz, for 16 bit linear coding).

Gating of the outputs onto a backplane or bus, can be obtained by use of the output TSCA for DXA as the programmed output pin (TSCB for DXB output). The output TSCA, or TSCB, will go low for the duration of the programmed data output time slot. Thus DXA or DXB can be gated onto a common backplane to provide security of output data. Alternatively, note that the DXA/DXB outputs are high impedance when no data is being output, so that several MV3010-1 outputs can be wire-ored.

Precise timing information for DXA, DXB, CLKX, FSX, TSCA and TSCB is given in the Electrical Characteristics section.

For the PCM input, the FSR pulse is also identified about a negative edge of the data clock i.e. CLKR. Data is also at the same basic sample rate of 125µs and has the same options of data/clock rate as for the output PCM. This means that there can be from 1 to 32 (64 expanded) 8 bit Time Slots, offset by 0 to 7 clock periods in the PCM frame. For 16 bit samples, the options of a multiple of 8 bit Time Slots as an offset, are still valid, as is the minimum of two Time Slots required between any adjacent (multiplexed) samples of the PCM frame. The above relationship for N_{TS} is also valid for the receive PCM timing.

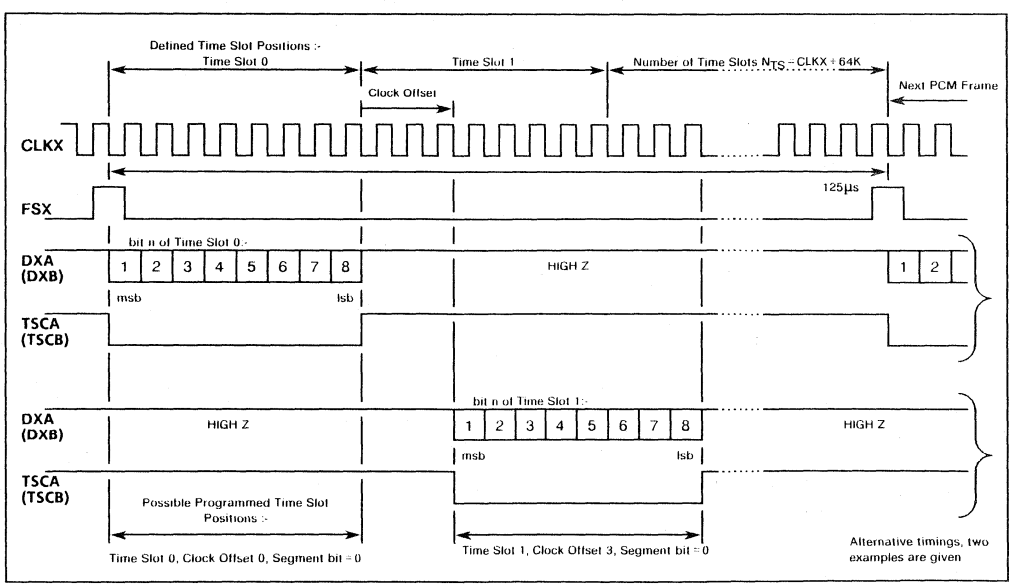


Fig. 5 : MV3010-1 Transmit PCM Timing Diagram.

Data is clocked into the device on the negative edge of CLKR. The first negative edge after FSR has occured defines the strobe time for the first bit of the first 8/16 bit sample of the frame. Positions of the 8 bit Time Slots are refered to this point. The Time Slot and Clock Offset of the frame that the MV3010-1 reads is again dynamically programmable via the Control Interface, all other bits of the frame data being ignored. Examples of the Receive PCM timing are shown in figure 6, with more precise timing information for DRA, DRB, CLKR and FSR given in the Electrical Characteristics section.

Programming of the MV3010-1 Transmit and Receive PCM timing can be such that a different format can exist between the two. However, coding of the data (companded 8 bit/linear 16 bit) is set simultaneously for both directions. Whilst FSX and FSR are both at a set 8KHz, they need not be coincident in time, provided they do not wander in phase. In the same way, CLKX, DXA/DXB can be offset from CLKR, DRA/DRB.

PCM Timing - Expanded Mode

The normal maximum number of Time Slots is 32 (for both Transmit and Receive directions) with CLKX/CLKR at 2048KHz and 256 data bits in the frame. This can be increased to 64 Time Slots by using expanded mode of operation. This creates a second set or segment of 256 bits that can be included in the frame. Thus, PCM data will be clocked out or read from either the first set of 256 bits (segment 0) or the second set of 256 bits (segment 1). Expanded mode is set via the Control Interface using the R_{SA} and X_{SA} bits (see Control and Monitoring section). The maximum number of Time Slots in expanded mode is 64 (32 for 16 bit samples), which can be set separately for Transmit and Receive directions.

2048KHz and 1544KHz PCM Formats

For 32 channel PCM, CLKX and CLKR are 2048KHz with Time Slot and Clock Offsets addressed as in Table 7 of the Control and Monitoring section. All 32 Time Slots of normal operation appear such that codes 20-6F are all valid. For 24 channel PCM, CLKX and CLKR are set to 1544KHz, with FSR and FSX still at 8KHz so that only 24 channels, plus bit 1 of Time Slot 25, appear in the frame. All other possible bits of the frame do not appear such that only codes 20-37, 40-57 and 60-6F of Table 7 are valid.

ENCODING AND DECODING

The analog input signal should be in the range ±3V with respect to analog ground. An input signal in this range is encoded according to the A-law, μ-Law or Linear algorithms. The corresponding PCM code is decoded to give an analog output signal in the range ±1.5V with respect to V_{OO} (nominally 2.5 Volts). This means that the analog output is one half of the amplitude of the analog input and has a net DC offset from ground. There are different reference milliwatt signals (0dBm0 levels) for input and output due to the difference in amplitude.

It is normal in a system to have a single coding scheme for a system, so for this reason Transmit and Receive coding are programmed simultaneously to work with the same scheme. The following sections describe each type of coding of the MV3010-1.

A-Law and μ-Law Codes (8 Bit)

These are non-linear codes in which the signal is described in terms of a sign bit plus segment and chord bits which denote the magnitude. There are 7 segments for A-Law and 8 for μ-Law. The size of the segments increase in approximately exponential steps.

Each segment is divided up linearly into chords (except the zero level in μ-Law). This means that the resolution is finer at smaller input voltages than at larger, and so gives a better match to the human ear. Table 2 shows how the A-Law code operates and Table 3 shows the μ-Law code.

In both codes positive values are represented by a sign bit of 1. The A-Law data is alternate digit inverted (ADI) and the μ-Law magnitude data is in effect inverted. These techniques are used to ensure that there are sufficient data transitions for good clock recovery (not

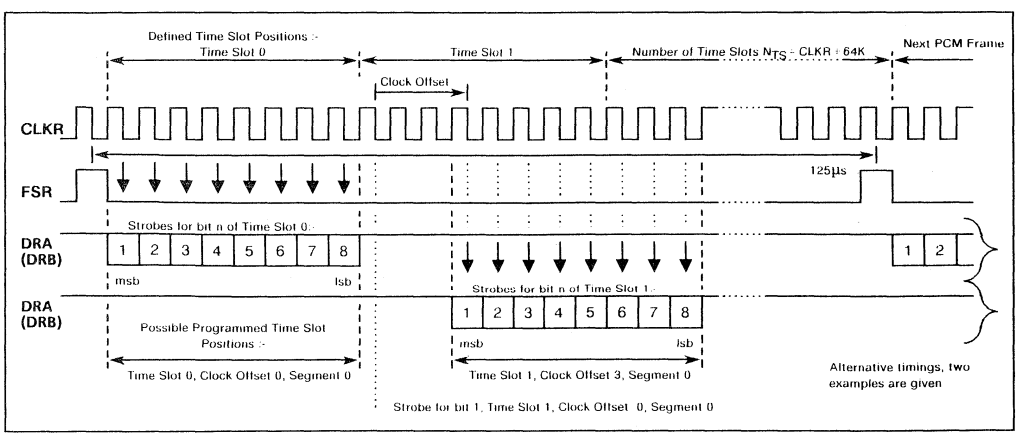


Fig 6 : MV3010-1 Receive PCM Timing Diagram.

Segment Number	Number × Size of Interval	Normalised Input Voltage = VIN × (4096 ÷ 3)	PCM DATA CHARACTER		Normalised Output Voltage (Note 2) = (V_{OUT}–V_{OO}) × (4096 ÷ 1.5)
			Without ADI msb lsb	With ADI (Note 4) msb lsb	
1	32×2	+(–) 0 to 2	1(0) 000 0000	1(0) 101 0101	+(–) 1
		+(–) 2 to 4	1(0) 000 0001	1(0) 101 0100	+(–) 3
		+(–) 4 to 6	1(0) 000 0010	1(0) 101 0111	+(–) 5
		+(–) 6 to 8	1(0) 000 0011	1(0) 101 0110	+(–) 7
		:	:	:	:
		+(–) 60 to 62	1(0) 001 1110	1(0) 100 1011	+(–) 61
		+(–) 62 to 64	1(0) 001 1111	1(0) 100 1010	+(–) 63
2	16×4	+(–) 64 to 68	1(0) 010 0000	1(0) 111 0101	+(–) 66
		+(–) 68 to 72	1(0) 010 0001	1(0) 111 0100	+(–) 70
		+(–) 72 to 76	1(0) 010 0010	1(0) 111 0111	+(–) 74
		+(–) 76 to 80	1(0) 010 0011	1(0) 111 0110	+(–) 78
		:	:	:	:
		+(–) 120 to 124	1(0) 010 1110	1(0) 111 1011	+(–) 122
		+(–) 124 to 128	1(0) 010 1111	1(0) 111 1010	+(–) 126
3	16×8	+(–) 128 to 136	1(0) 011 0000	1(0) 110 0101	+(–) 132
		+(–) 136 to 144	1(0) 011 0001	1(0) 110 0100	+(–) 140
		+(–) 144 to 152	1(0) 011 0010	1(0) 110 0111	+(–) 148
		+(–) 152 to 160	1(0) 011 0011	1(0) 110 0110	+(–) 156
		:	:	:	:
		+(–) 240 to 248	1(0) 011 1110	1(0) 110 1011	+(–) 144
		+(–) 248 to 256	1(0) 011 1111	1(0) 110 1010	+(–) 252
4	16×16	+(–) 256 to 272	1(0) 100 0000	1(0) 001 0101	+(–) 264
		+(–) 272 to 288	1(0) 100 0001	1(0) 001 0100	+(–) 280
		+(–) 288 to 304	1(0) 100 0010	1(0) 001 0111	+(–) 296
		+(–) 304 to 320	1(0) 100 0011	1(0) 001 0110	+(–) 312
		:	:	:	:
		+(–) 480 to 496	1(0) 100 1110	1(0) 001 1011	+(–) 488
		+(–) 496 to 512	1(0) 100 1111	1(0) 001 1010	+(–) 504
5	16×32	+(–) 512 to 544	1(0) 101 0000	1(0) 000 0101	+(–) 528
		+(–) 544 to 576	1(0) 101 0001	1(0) 000 0100	+(–) 560
		+(–) 576 to 608	1(0) 101 0010	1(0) 000 0111	+(–) 592
		+(–) 608 to 640	1(0) 101 0011	1(0) 000 0110	+(–) 624
		:	:	:	:
		+(–) 960 to 992	1(0) 101 1110	1(0) 000 1011	+(–) 976
		+(–) 992 to 1024	1(0) 101 1111	1(0) 000 1010	+(–) 1008
6	16×64	+(–) 1024 to 1088	1(0) 110 0000	1(0) 011 0101	+(–) 1056
		+(–) 1088 to 1152	1(0) 110 0001	1(0) 011 0100	+(–) 1120
		+(–) 1152 to 1216	1(0) 110 0010	1(0) 011 0111	+(–) 1184
		+(–) 1216 to 1280	1(0) 110 0011	1(0) 011 0110	+(–) 1248
		:	:	:	:
		+(–) 1920 to 1984	1(0) 110 1110	1(0) 011 1011	+(–) 1952
		+(–) 1984 to 2048	1(0) 110 1111	1(0) 011 1010	+(–) 2016
7	16×128	+(–) 2048 to 2176	1(0) 111 0000	1(0) 010 0101	+(–) 2112
		+(–) 2176 to 2304	1(0) 111 0001	1(0) 010 0100	+(–) 2240
		+(–) 2304 to 2432	1(0) 111 0010	1(0) 010 0111	+(–) 2368
		+(–) 2432 to 2560	1(0) 111 0011	1(0) 010 0110	+(–) 2496
		:	:	:	:
		+(–) 3840 to 3968	1(0) 111 1110	1(0) 010 1011	+(–) 3904
		+(–) 3968 to 4096	1(0) 111 1111	1(0) 010 1010	+(–) 4032

Notes :-
1. 4096 Normalised value units correspond to 3.14dBm0.
2. VOUT Output Voltage (V_{OUT}) is DC offset by V_{OO}, see Electrical Characteristics.
3. Characters in parenthesis are alternatives for negative values.
4. Alternate Digit Inversion (ADI) is obtained by inversion of the even bits.

Table 2 : A-Law Code.

Segment Number	Number × Size of Interval	Normalised Input Voltage = VIN × (8192 ÷ 3)	PCM DATA CHARACTER msb lsb	Normalised Output Voltage (Note 2) = (V_{OUT}–V_{OO}) × (8192 ÷ 1.5)
1	1 × 1	+(–) 0 to 1	1(0) 111 1111	+(–) 0
		+(–) 1 to 3	1(0) 111 1110	+(–) 2
		+(–) 3 to 5	1(0) 111 1101	+(–) 4
	15 × 2	+(–) 5 to 7	1(0) 111 1100	+(–) 6
		:	:	:
		+(–) 27 to 29	1(0) 111 0001	+(–) 28
		+(–) 29 to 31	1(0) 111 0000	+(–) 30
2	16 × 4	+(–) 31 to 35	1(0) 110 1111	+(–) 33
		+(–) 35 to 39	1(0) 110 1110	+(–) 37
		+(–) 39 to 43	1(0) 110 1101	+(–) 41
		:	:	:
		+(–) 87 to 91	1(0) 110 0001	+(–) 89
		+(–) 91 to 95	1(0) 110 0000	+(–) 93
3	16 × 8	+(–) 95 to 103	1(0) 101 1111	+(–) 99
		+(–) 103 to 111	1(0) 101 1110	+(–) 107
		+(–) 111 to 119	1(0) 101 1101	+(–) 115
		:	:	:
		+(–) 207 to 215	1(0) 101 0001	+(–) 211
		+(–) 215 to 223	1(0) 101 0000	+(–) 219
4	16 × 16	+(–) 223 to 239	1(0) 100 1111	+(–) 231
		+(–) 239 to 255	1(0) 100 1110	+(–) 247
		+(–) 255 to 271	1(0) 100 1101	+(–) 263
		:	:	:
		+(–) 447 to 463	1(0) 100 0001	+(–) 455
		+(–) 463 to 479	1(0) 100 0000	+(–) 471
5	16 × 32	+(–) 479 to 511	1(0) 011 1111	+(–) 495
		+(–) 511 to 543	1(0) 011 1110	+(–) 527
		+(–) 543 to 575	1(0) 011 1101	+(–) 559
		:	:	:
		+(–) 927 to 959	1(0) 011 0001	+(–) 943
		+(–) 959 to 991	1(0) 011 0000	+(–) 975
6	16 × 64	+(–) 991 to 1055	1(0) 010 1111	+(–) 1023
		+(–) 1055 to 1119	1(0) 010 1110	+(–) 1087
		+(–) 1119 to 1183	1(0) 010 1101	+(–) 1151
		:	:	:
		+(–) 1887 to 1951	1(0) 010 0001	+(–) 1919
		+(–) 1951 to 2015	1(0) 010 0000	+(–) 1983
7	16 × 128	+(–) 2015 to 2143	1(0) 001 1111	+(–) 2079
		+(–) 2143 to 2271	1(0) 001 1110	+(–) 2207
		+(–) 2271 to 2399	1(0) 001 1101	+(–) 2335
		:	:	:
		+(–) 3807 to 3935	1(0) 001 0001	+(–) 3871
		+(–) 3935 to 4063	1(0) 001 0000	+(–) 3999
8	16 × 256	+(–) 4063 to 4319	1(0) 000 1111	+(–) 4191
		+(–) 4319 to 4575	1(0) 000 1110	+(–) 4447
		+(–) 4575 to 4831	1(0) 000 1101	+(–) 4703
		:	:	:
		+(–) 7647 to 7903	1(0) 000 0001	+(–) 7775
		+(–) 7903 to 8159	1(0) 000 0000	+(–) 8031

Notes :-
1. 8159 Normalised value units correspond to 3.17dBm0.
2. VOUT Output Voltage (V_{OUT}) is DC offset by V_{OO}, see Electrical Characteristics.
3. Characters in parenthesis are alternatives for negative values

Table 3 : μ-Law Code.

performed by the MV3010-1) on the Receive side of digital trunk lines when the channel is quiet.

Linear Code (16 Bit)

The device may be programmed for linear operation to simplify the design of telephone conference circuits or if additional signal processing is desired. A 2's complement scheme is used with positive values represented by the sign bit equal to 0 (the opposite of the non-linear codes). The resolution is slightly less than the theoretical limit for 16 bits (see Table 4).

Signal Levels and the Digital Milliwatt

Signal levels for A-law and μ-Law codes are defined with respect to a milliwatt reference level in units of dBm0. This means that a signal of 0dBm0 is a reference milliwatt signal i.e. it is at the local reference level. It does not mean that the signal will dissipate 1mW into a 600Ω resistor (i.e. is 2.191V p-p) unless the local reference level, 0dBm0, also corresponds to 0 in units of dBm (600Ω).

The specifications for A-Law and μ-Law codes (CCITT Specification G.711) define that the uppermost coding decision levels for A-Law (4096) and μ-Law (8159) correspond to 3.14dBm0 and 3.17dBm0 respectively.

This means that the 0dBm0 level is about 5.6dBm (600Ω) at the analog input and about -0.4dBm (600Ω) at the analog output.

The digital milliwatt signal provides an example of this in practice. The digital milliwatt is a defined sequence of 8 codes which, if there was no loss on the receive path, would produce a 0dBm0 signal on the analog output. The codes for the digital milliwatt for the three cases are given in Table 5. The actual voltages involved can be determined from Tables 2, 3 and 4.

TRANSMIT AND RECEIVE FILTERS

Both the Transmit and Receive paths contain a 4 Tap FIR filter, as shown in Figure 7. The Z^{-1} sections are a delay by the internal sample rate i.e. 62.5μs (16KHz), with the output a weighted summation (A_0-A_3) of the input and delayed signals. The multipliers, or coefficients A_0-A_3 for each filter, are stored in RAM locations on chip and used by the DSP processing of the MV3010-1 to calculate the output samples. These coefficients are loaded via the Control Interface, as described in the Control and Monitoring section. Thus the output of the filters can be represented by the transfer function:-

$$H(Z) = \sum_{n=0}^{3} A_n(Z^{-n}) = A_0 + A_1Z^{-1} + A_2Z^{-2} + A_3Z^{-3}$$

Normalised Input Voltage VIN × (32,768 ÷ 3)	PCM DATA CHARACTER msb lsb	Normalised Output Voltage $-V_{OO}$ × (32,768 ÷ 1.5)
–32,768 to –32,255.5	1 000 0000 1111 1111	–32,256
–32,255.5 to –32,254.5	1 000 0010 0000 0001	–32,255
–32,254.5 to –32,253.5	1 000 0010 0000 0010	–32,254
:	:	:
–1.5 to –0.5	1 111 1111 1111 1111	–1
–0.5 to +0.5	0 000 0000 0000 0000	0
+0.5 to +1.5	0 000 0000 0000 0001	+1
:	:	:
+32,253.5 to +32,254.5	0 111 1101 1111 1110	+32,254
+32,254.5 to +32,255.5	0 111 1101 1111 1111	+32,255
+32,255.5 to + 32,768	0 111 1111 0000 0000	+32,256

Table 4 : Linear Code.

Phase	A-Law msb lsb	μ-Law msb lsb	LINEAR msb lsb
–7/8 × 180°	0 011 0100	0 001 1110	1 101 1101 1000 0100
–5/8 × 180°	0 010 0001	0 000 1011	1 010 1110 1000 0100
–3/8 × 180°	0 010 0001	0 000 1011	1 010 1110 1000 0100
–1/8 × 180°	0 011 0100	0 001 1110	1 101 1101 1000 0100
+1/8 × 180°	1 011 0100	1 001 1110	0 010 0010 0111 1100
+3/8 × 180°	1 010 0001	1 000 1011	0 101 0001 0111 1100
+5/8 × 180°	1 010 0001	1 000 1011	0 101 0001 0111 1100
+7/8 × 180°	1 011 0100	1 001 1110	0 010 0010 0111 1100

Table 5 : Successive PCM input codes for Digital Milliwatt on VOUT.

The unit delay operator of the digital filter, Z^{-1}, can be represented as:-

$$Z^{-1} = \exp(-i2\pi F \div F_0)$$

where F_0 is the sample frequency (16KHz), F the signal frequency. We can obtain the real part of the filter response from the following:-

$$\mathrm{Re}\{H(z)\} = \sum_{n=0}^{3} A_n \mathrm{Cos}(2\pi nFT) \qquad \text{with } T = 1/F_0$$

$$\text{i.e.} \quad = A_0 + A_1\mathrm{Cos}(\omega T) + A_2\mathrm{Cos}(2\omega T) + A_3\mathrm{Cos}(3\omega T) \quad \ldots ①$$

and similarily the imaginary part of the filter response will be :-

$$\mathrm{Im}\{H(z)\} = \sum_{n=0}^{3} A_n \mathrm{Sin}(2\pi nFT)$$

$$\text{i.e.} \quad = A_1\mathrm{Sin}(\omega T) + A_2\mathrm{Sin}(2\omega T) + A_3\mathrm{Sin}(3\omega T) \quad \ldots ②$$

We can write $\mathrm{Cos}(2\omega T)$, $\mathrm{Cos}(3\omega T)$, $\mathrm{Sin}(2\omega T)$ and $\mathrm{Sin}(3\omega T)$ in terms of $\mathrm{Cos}(\omega T)$ and $\mathrm{Sin}(\omega T)$, so that 1 and 2 become :-

$$\mathrm{Re} = A_0 - A_2 + (A_1 - 3A_3)\mathrm{Cos}(\theta) + 2A_2\mathrm{Cos}^2(\theta) + 4A_3\mathrm{Cos}^3(\theta) \quad \ldots ③$$
$$\mathrm{Im} = \mathrm{Sin}(\theta)[A_1 - A_3 + 2A_2\mathrm{Cos}(\theta) + 4A_3\mathrm{Cos}^2(\theta)] \quad \ldots ④$$

where $\theta = 2\pi FT$. For the amplitude, A, and phase, ϕ, characteristics we can use the following:-

$$A = (\mathrm{Re}^2 + \mathrm{Im}^2)^{\frac{1}{2}}$$
$$\mathrm{Tan}(\phi) = (\mathrm{Im}) \div (\mathrm{Re})$$

Using expressions 3 and 4 for real and imaginary parts of the filter response, then we obtain:-

$$A = \{8Q\mathrm{Cos}^3(\theta) + 4P\mathrm{Cos}^2(\theta) + 2N\mathrm{Cos}(\theta) + M\}^{\frac{1}{2}} \quad \ldots ⑤$$

with $Q = A_0A_3$
$P = A_0A_2 + A_1A_3$
$N = A_0A_1 + A_1A_2 + A_2A_3 - 3A_0A_3$
$M = (A_0 - A_2)^2 + (A_1 - A_3)^2$

and $\mathrm{Tan}(\phi) = \mathrm{Tan}(\theta)\{1 + [2A_2\mathrm{Cos}(\theta) + (A_2 - A_0)] \div \mathrm{Re}\}$ ...⑥

with Re as in 3, as general equations for A and ϕ of the filter response, relative to the filter input signal.

Both Transmit and Receive filters can be switched in and out of the signal path by Control Words input via the Control Interface. This can be done with the device in its power-up or power-down modes of operation. In addition, further Control Words allow both reading and writing of the filter coefficients A_0-A_3, also in both modes.

C FILTER

The structure of the C Filter is shown in outline form in figure 8. In fact the C Filter consists of two separate filters, with identical form, known as the Foreground and Background Filters. The Foreground Filter provides modified samples of the receive path for cancellation of the receive signal (via the echo path) from the transmit signal. The Background Filter is used in adaptive mode to automatically search for any new coefficients that may improve cancellation by the Foreground Filter.

Adaptive Mode, as described, uses the error from both filters to determine whether or not the background coefficients provide better cancellation than the foreground coefficients. Whenever this is the case, then the new coefficients are transferred to the Foreground Filter, and the Background Filter continues searching for even better coefficients. Note that the Error Filter output is used in the

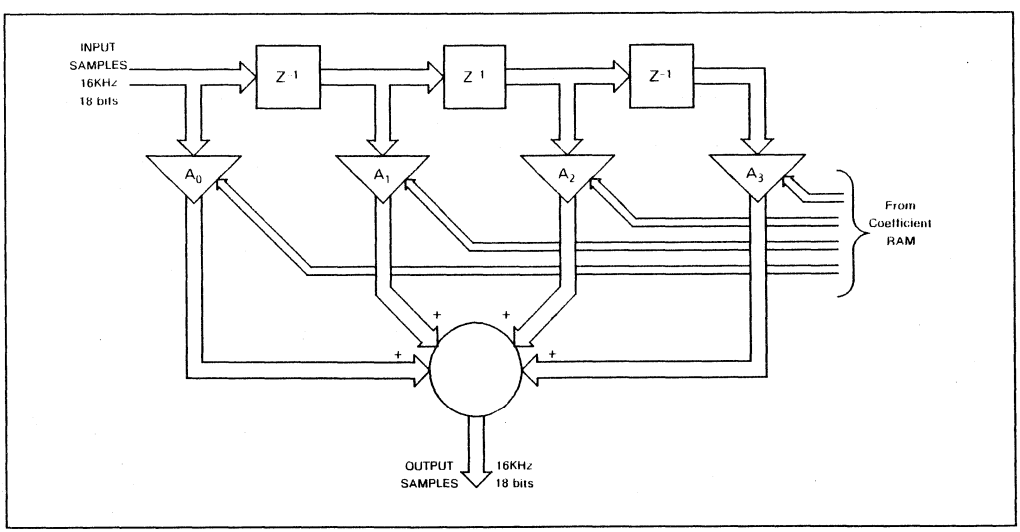


Figure 7 : Transmit and Receive Filter Structure (4 Tap FIR).

decision process for the transfer of new coefficients, with the DC Tap eliminating DC.

In the non-adaptive mode updating of coefficients is inhibited, and the C Filter uses the last set of coefficients entered into the Foreground Filter. These will either be from the Background Filter (adaption has been frozen) or those entered via the Control Interface. Writing or reading of coefficients can be carried out at any time in either the power-up or power-down modes of operation of the MV3010-1.

The nature/value of the coefficients depends on the nature of the echo path. This echo path depends on the interface of the MV3010-1 to the subscriber line (2 to 4 wire conversion). Such an interface might consist of a transformer type Hybrid or a solid state Subscriber Line Interface Circuit (SLIC), such as the GEC Plessey Semiconductors SL373 or SL376 (see separate data sheets). It is normal to expect that the 2 to 4 wire conversion will consist of a mismatch of the receive input to the 2 wire line and not completely (if at all) remove the receive signal from the transmit signal. This Echo Return varies as the conditions of the line (length/impedance etc) vary, so causing differing characteristics of the echo path. It is the job of the C filter to remove this echo from the transmit signal. Thus the C Filter allows several software solutions, with one hardware design, to provide different line interfaces within the telephone network. The C Filter adaptive mode then makes it possible for the MV3010-1 to automatically follow any changing conditions of each subscriber line, so maintaining good Echo Return Loss at the MV3010-1 PCM output.

Note that the echo path will include any D/A and A/D delays within the MV3010-1, which are discussed later on in this section. We need now to discuss the C Filter in more detail.

Figure 9 shows a more detailed model of the C Filter. It can be seen that the filter is 9 taps FIR followed by a tenth tap IIR, which has a 15/16 multiplier in the feedback loop forming the last tap. This last tap allows matching of any long tail of the impulse resonse of the echo path, whilst maintaining a more concise structure. As for the Transmit and Receive Filters, the C Filter also operates at a basic 16KHz (62.5µs taps) rate.

Since both Foreground and Background Filters are of the same structure, we can represent them as being made up from one set of unit delay sections (Z^{-1}). The two filter outputs are then just different summations of the filter sections. Note that only the odd numbered taps of the Background Filter (coefficients A_1, A_3, A_5, A_7, A_9) are involved in the adaptive process. This prevents adaption of the filter to frequencies in the range 4KHz-8KHz.

The adaptive process uses the difference between the Adaptive Error and the Fixed Error to decide whether or not to update the foreground coefficients. Adaptive Error is determined from the difference between the Background Filter output and the Transmit input, as is the Fixed Error from that of the Foreground Filter output and Transmit input. If the long term average of the Adaptive Error is less than 7/8 of the Fixed Error, then a signal will be generated to initiate transfer of the adaptive coefficients (odd taps only) to the Foreground Filter.

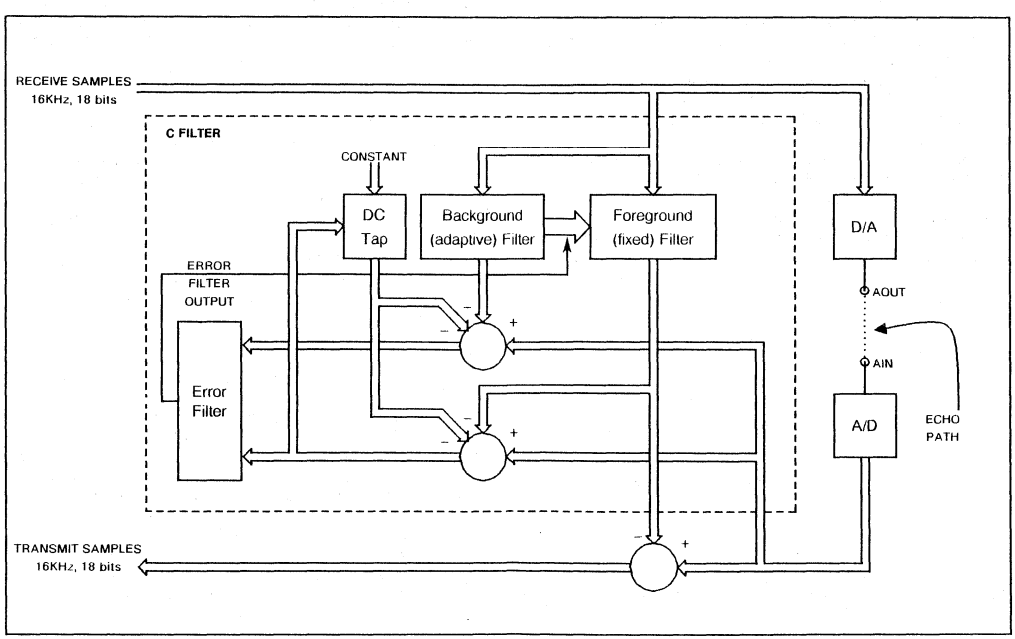


Fig 8 : MV3010-1 Basic C Filter Structure (9 Tap FIR + 1 Tap IIR).

The minimum time for adaption is 64ms under appropriate conditions. Typically adaption may take several hundred ms. New coefficients for the Background Filter are generated using the classic Widrow/Hoff algorithm. The MV3010-1 thus uses the nature of the signal to analyse the echo path. In order to obtain good broadband cancellation using adaption it is necessary to use a broadband signal at the receive input. If a single tone were to be used, for example, then whilst cancellation is achieved at this frequency, there is no guarantee of performance at other frequencies (if the C Filter is now set to non-adaptive mode) since the MV3010-1 was unable to use these frequencies in the echo analysis.

For the C Filter to be operative, it must first be enabled via the control interface. The filter can then be used in either Adaptive mode (able to follow changes in the echo path) or Non-Adaptive mode (fixed modelling of the echo path). Adaption takes place (Adapt Enable, Figure 9) with the C Filter enabled, under two separate conditions. Firstly, it may be controlled by use of enable/disable codes via the Control Interface, as described in the Control and Monitoring section. Alternatively, it is set by the logic level at the Status Input (SI) pin using other control codes. Note that adaption may not occur if there is a large DC bias at the VIN pin. The SI pin also controls adaption as described in the Stand-Alone section. When disabled, Transmit samples remain totally unaffected by the C Filter. As with the Transmit and Receive Filters, all of the coefficients can be programmed and/or read out via the Control Interface, whether or not the MV3010-1 is in Power-Up or Power-Down mode (see Control and Monitoring section).

A signal correlator is incorporated which will detect periodic signals in the receive path. When detected the background filter coefficients, even if deemed to give better cancellation, are not transferred to the foreground. The correlator may be disabled for testing and preprogramming purposes (see control and monitoring section). A double talk detector is also included to prevent adaption while large near end signals are present. A programmable coefficient DTC allows the relative levels of near and far end signals that trigger this detector to be set (see Table 13). Setting this coefficient to zero will disable this feature.

An oscillation quench circuit will reset the adaptive coefficients to their preprogrammed values should an unstable situation occur. This action can be monitored via the control interface (see Table 14).

We can obtain a mathematical representation of the C Filter in the same way as for the Transmit and Receive Filters. Thus we can write:-

$$H(Z) = \sum_{n=0}^{8} A_n Z^{-n} + \{[A_9 Z^{-9}] \div [16-15Z^{-1}]\} \quad ...①$$

with $Z^{-1} = e^{-i\omega T}$ as before. For real and imaginary parts of the filter response (equation 1) we get:-

$$Re\{H(Z)\} = \sum_{n=0}^{8} A_n Cos(n\theta) + \{A_9 X\} \quad ..②$$

$$Im\{H(Z)\} = \sum_{n=0}^{8} A_n Sin(n\theta) + \{A_9 Y\} \quad ..③$$

where $X = \{[16Cos(9\theta)-15Cos(8\theta)] \div [481-480Cos(\theta)]\}$
and $Y = \{[16Sin(9\theta)-15Sin(8\theta)] \div [481-480Cos(\theta)]\}$

which can be used to obtain the amplitude, A, and phase, ϕ, of the filter from :-

$$A = (Re^2 + Im^2)^{\frac{1}{2}} \quad ...④$$
$$Tan(\phi) = (Im \div Re) \quad ...⑤$$

Equations 2 to 5 form the basis of a computer program that calculates the necessary coefficient values required to obtain a given response. More information on this is given in Applications Note AN84, Preprogramming the MV3010-1 C Filter using the measurement method.

When determining coefficients for a given C Filter response, note that the echo path will include the MV3010-1 D/A and A/D delays. In addition, the amplitude of the echo signal is also affected by the difference between the VOUT and VIN dynamic ranges and also includes the 16/15 of the D/A conversion. The combined effect is to add a 5.46dB (×8/15) loss to the echo path, at a delay of 125µs, or 2 Taps (i.e. at A_2).

CONTROL and MONITORING

The MV3010-1 is controlled and monitored through the device control interface. This allows control of the I/O Latches and status interface, PCM coding and modes of operation, the programming of the Transmit and Receive Time Slot and Clock Offsets, the Gain and Filter coefficients, the C Filter modes and the activation and deactivation of the diagnostic functions.

Initialisation, Power-Up/Power-Down

When power is first applied, the MV3010-1 is initialised and goes into its Power-Down mode of operation. This has several consequences: the Transmit PCM Outputs (DXA and DXB) go into their high-impedance state; the Analog Output (VOUT) goes to Analog Ground (AGND); Transmit and Receive Time Slot and Clock Offsets are set to zero; PCM ports A, non-expanded mode are selected; the Digital I/O pins (CP1 to CP5) are configured as inputs; A-Law is selected; Transmit, Receive and Cancellation Filters are disabled; Transmit and Receive Gains are set to 0dB, correlator is enabled, double talk coefficient is set to zero and the adaptive mode of the C Filter is set only if the SI pin is high. None of the MV3010-1 functions are active or meaningful until the device is put into its Power-Up mode. Power-Down mode is thus a standby, low power consumption state of the device. When a power-up command is sent via the Control Interface, then the MV3010-1 becomes fully active with functions as set via the interface or as for Stand Alone operation. Control instructions may be sent to the device 500µs after the first application of power. The Power-Down instruction may be sent to the device at any time to select this mode.

Stand-Alone Operation

If the default conditions established by initialisation are acceptable, Stand-Alone operation can be used. In this mode, the functions remain as set during initialisation with the MV3010-1 only able to change between Power-Up and Power-Down modes, excepting that the SI pin enables the C Filter with adaption (SI Pin high) or disables the filter totally (SI Pin low). Stand-Alone operation is selected by holding the CSB pin low for greater than 8 periods of the clock applied to the DCLK pin. Note, this is easily achieved by connecting the DCLK pin to the adjacent MCLK pin with Power-Up and Power-Down instructions generated by holding the DI/O pin high or low, respectively.

Normal Operation

For Normal Operation, control information is sent to the MV3010-1 as 8 bit bytes input on the DI/O pin, strobed under the control of the DCLK clock and CSB pulse. All the functions of the MV3010-1 can now be set via the Control Interface.

Data entered to the device will be one of two types. Most of the time data will consist of Control Codes to change the device functional status. Some of these Control Codes require subsequent Data bytes to be entered as part of the instruction, or will cause subsequent output of Data relevant to the Control Code.

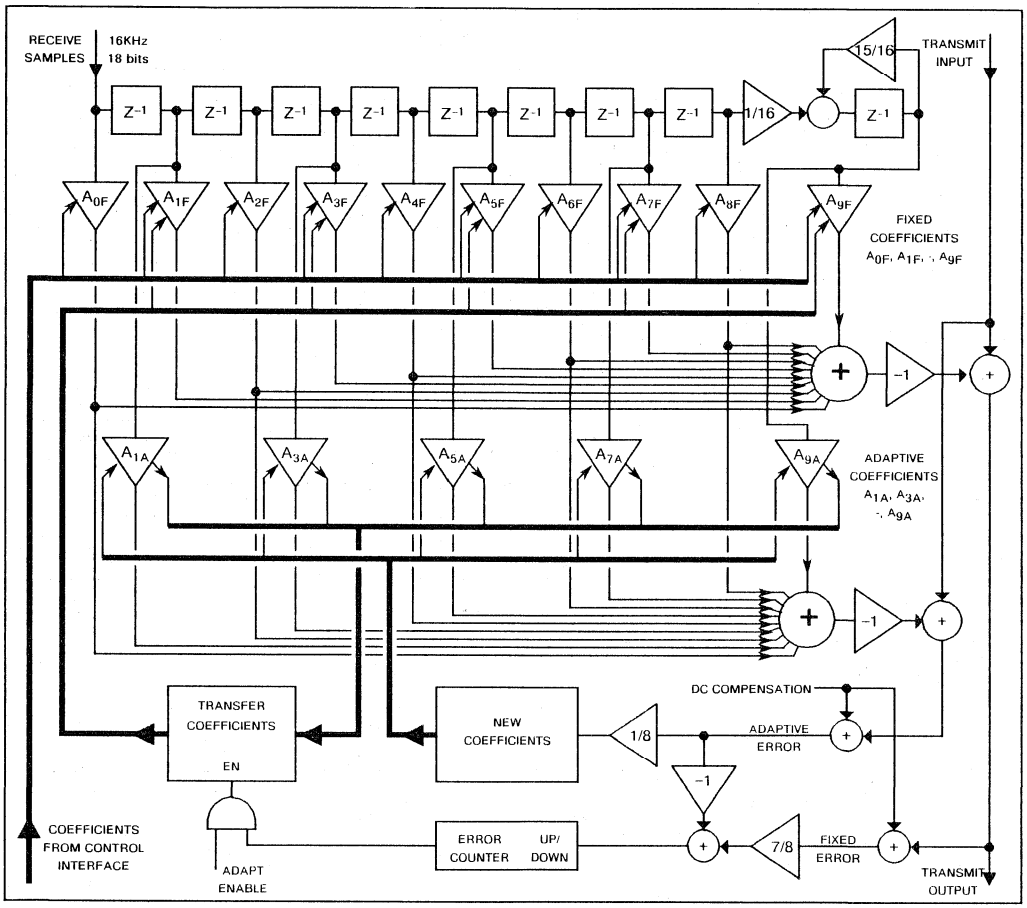


Fig 9 : MV3010-1 Conceptual C Filter Representation (9 Tap FIR + 1 Tap IIR).

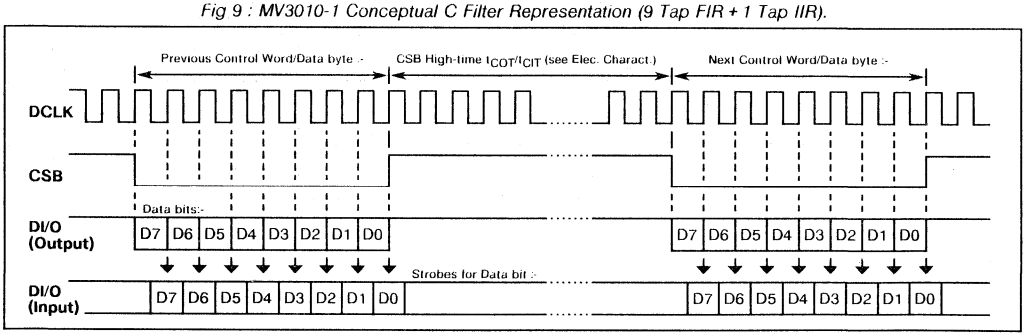


Fig. 10 : MV3010-1 Control Interface Timing Diagram - Normal Operation.

INSTRUCTION DESCRIPTION				MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES
Operating Mode	Set Power-Up			PU	FF	None
	Set Power-Down			PD	00	None
PCM Slot Address	Transmit	Read		STR	75	1 - Output
		Write	Time Slot	STWT	20 to 3F	None
			Clock offset	STWC	60 to 67	None
	Receive	Read		SRR	7D	1 - Output
		Write	Time Slot	SRWT	40 to5F	None
			Clock offset	SRWC	68 to 6F	None
Gain Adjust	Transmit, G_X	Read Coefficient		GTR	71	2 - Output
		Write Coefficient		GTW	72	2 - Input
	Receive, G_R	Read Coefficient		GRR	79	2 - Output
		Write Coefficient		GRW	7A	2 - Input
Filter Commands	Enable Selected Filters			FE	80 to 87	None
	Transmit	Read Coefficients		FTR	A7	8 - Output
		Write Coefficients		FTW	A4	8 - Input
	Receive	Read Coefficients		FRR	AB	8 - Output
		Write Coefficients		FRW	A8	8 - Input
	Cancellation	Control Filter Modes		FCC	BC to BF	None
		Read Coefficients		FCR	A3	20 - Output
		Write Coefficients		FCW	A0	20 - Input
		Read Double - Talk		FCDR	A1	2 - Output
		Write Double - Talk		FCDW	A2	2 - Input
Digital I/O's and Status Input pin (SI)	Digital I/O Configuration	Read Status		IOCR	C1	1 - Output
		Write Status		IOCW	D1	1 - Input
	Digital I/O Data	Read		IODR	C8	1 - Output
		Write		IODW	D8	1 - Input
PCM	Set Coding Scheme			PC	B8 to BB	None
	Association	Read		PAR	77	1 - Output
		Write		PAW	90 to 9F	None
Diagnostic	Reset			DR	B0	None
	High Pass Filter Disable			DHD	B3	None
	Receive	Attenuate Path		DRA	B1	None
		Disable Path		DRD	B2	None
	Loop	Analog		DLA	B7	None
		Digital		DLD	B4	None
	Correlator	Disable		DCD	B5	None

Fig. 11 : MV3010-1 Control Instructions - see also Tables 6 to 16.

Data which is requested from the device is output on the DI/O pin, any attempted input of data being ignored until all data bytes have been output (any input driving DI/O will thus corrupt the output data). Fig. 10 shows the nominal signal timing.

The normal programming sequence is for a Code byte to be sent to the device first. This may be followed by a number of Data bytes sent to/read from the device depending on the specific Control Code preceding them. If the Control Code requires loading of associated Data bytes on DI/O, then programming must continue with the relevant number of data bytes after the Control Code.

All subsequent bytes after the Control Code that are expected to be data will be treated as data for that code. No more Control Codes will be accepted until all data has been entered. The only exception to this is that the programming sequence will be aborted and the device will enter Power-Down mode if a Power-down instruction is sent instead of an input data byte (there is no all zeroes data byte so confusion is avoided). Programming of the device continues normally after the last data byte has been entered, or output if that was the last Control Code.

Figure 11 shows the various Control Codes available with Figure 12 a Control Code Map. The effect of each code is described in Tables 6 to 16.

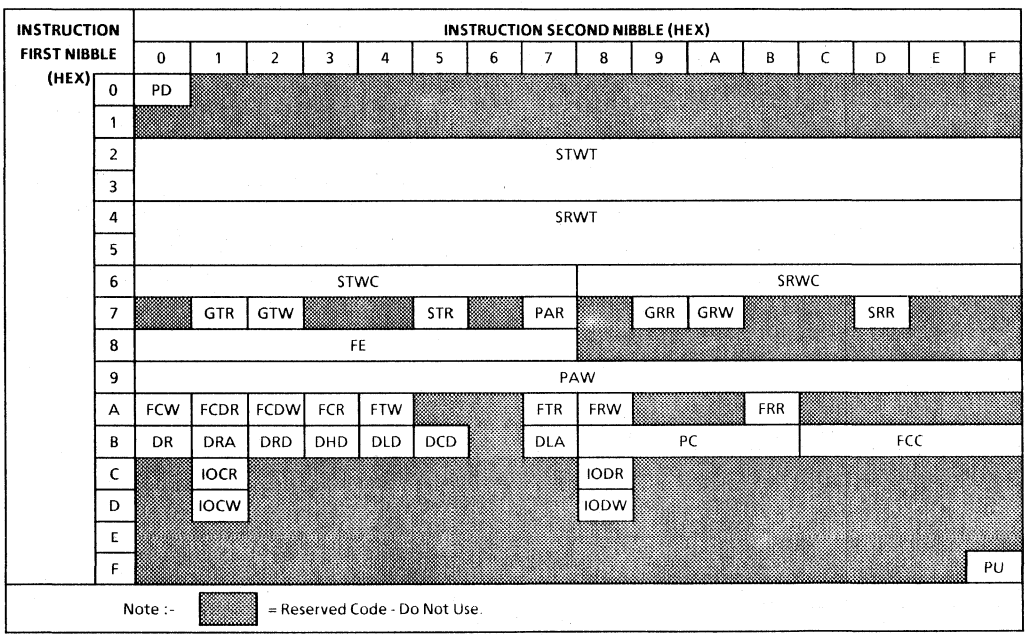


Fig. 12 : MV3010-1 Control Instructions - see also Tables 6 to 16.

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
PU	FF	None	**Power-Up.** This instruction takes the device out of Power-Down. It would normally be preceeded by instructions to configure the device. It has no effect if the device is not in power-down mode.
PD	00	None	**Power-Down.** This instruction puts the device into Power-Down mode. The transmit PCM outputs (DXA and DXB) go into their high impedance state and the analog output (VOUT) goes to V_{AGND}. The device is still programmable in this mode.

Table 6 : Operating Mode Instructions.

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
STR	75	1-Output	**Slot Address - Transmit - Read.** This instruction causes the device to output a data byte which contains the transmit slot address. The data byte contains the 5 Time Slot address bits (msb's) followed by the 3 Clock Offset bits. For example, if the hex data byte is B1, then the Time Slot has been set to 22 and the Clock Offset has been set to 1; i.e. the start of the transmit PCM output is offset by 177 (=22x8+1) clock cycles from FSX.
STWT	20 to 3F	None	**Slot Address - Transmit - Write - Time Slot.** This instruction defines the Transmit Time Slot address. The 3 msb's define the Code type, and the 5 lsb's set the Time Slot. For example the hex code 2A sets the Time Slot address to 10.
STWC	60 to 67	None	**Slot Address - Transmit - Write - Clock Offset.** This instruction defines the Transmit Clock Offset. The 5 msb's define the Code type, and the 3 lsb's set the Clock Offset. For example the hex code 63 sets the Clock Offset to 3.
SRR	7D	1-Output	**Slot Address - Receive - Read.** This instruction causes the device to output a data byte which contains the receive slot address. The data byte contains the 5 Time Slot address bits (msb's) followed by the 3 Clock Offset bits. For example, if the hex data byte is B1, then the Time Slot has been set to 22 and the Clock Offset has been set to 1, i.e. the start of the receive PCM input is offset by 177 (=22x8+1) clock cycles from FSR.
SRWT	40 to 5F	None	**Slot Address - Receive - Write - Time Slot.** This instruction defines the Receive Time Slot address. The 3 msb's define the Code type, and the 5 lsb's set the Time Slot. For example the hex code 4A sets the Time Slot address to 10.
SRWC	68 to 6F	None	**Slot Address - Receive - Write - Clock Offset.** This instruction defines the Receive Clock Offset. The 5 msb's define the Code type, and the 3 lsb's set the Clock Offset. For example the hex code 6B sets the Clock Offset to 3.

Table 7 : PCM Time Slot and Clock Offset Instructions.

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
GTR	71	2-Output	**Gain - Transmit - Read.** This instruction causes the device to output 2 data bytes which contain the Transmit Gain information, G_X, in the format shown in Table 9.
GTW	72	2-Input	**Gain - Transmit - Write.** This instruction sets the Transmit Gain, G_X, to the value defined by two successive data bytes, which must be entered in the format shown in Table 9.
GRR	79	2-Output	**Gain - Receive - Read.** This instruction causes the device to output 2 data bytes which contain the Receive Gain information, G_R, in the format shown in Table 9.
GRW	7A	2-Input	**Gain - Receive - Write.** This instruction sets the Receive Gain, G_R, to the value defined by two successive data bytes, which must be entered in the format shown in Table 9.

Table 8 : Transmit and Receive Gain Instructions.

DATA BYTE FORM									DATA DESCRIPTION
BYTE No.	BIT No. D7	D6	D5	D4	D3	D2	D1	D0	These bytes are in the form of a 2's complement number in the range ±2 which are used to construct the gain Coefficients as follows:-
1	1	G_1	G_0	G_{-1}	G_{-2}	G_{-3}	G_{-4}	G_{-5}	$G = -G_1 \times 2^1 + G_0 \times 2^0 + G_{-1} \times 2^{-1} + G_{-2} \times 2^{-2} + ... + G_{-10}2^{-10}$
2	1	G_{-6}	G_{-7}	G_{-8}	G_{-9}	G_{-10}	X	X	The Receive Gain is $G_R = G$ i.e. –2 to +2.
1 = +5V, X = Dont Care (0/1)									The Transmit Gain is $G_X = 2 \times (G + 1)$ i.e. –2 to +6.

Table 9 : Transmit and Receive Gain Data bytes (Coefficients).

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
FE	80 to 87	None	**Filter - Enable.** This instruction allows the C Filter, Transmit Filter and Receive Filter to be enabled or disabled. The instruction has the format:- D7 D6 D5 D4 D3 D2 D1 D0 1 0 0 0 0 CF XF RF If CF is 1 then the C Filter is enabled. If it is 0 then the C Filter is disabled (i.e. Cancellation subtracts zero). If XF is 1 then the X Filter is enabled. If it is 0 then the X Filter is disabled (i.e. the transfer function is set to 1). If RF is 1 then the R Filter is enabled. If it is 0 then the R Filter is disabled (i.e. the transfer function is set to 1). N.B. Disabling a filter does not change its coefficients.
FTR	A7	8-Output	**Filter - Transmit - Read.** This instruction causes the device to output 8 data bytes which represent the 4 numbers corresponding to the 4 Transmit Filter coefficients that have the format shown in Table 11.
FTW	A4	8-Input	**Filter - Transmit - Write.** This instruction sets the 4 Transmit Filter coefficients to the 4 numbers, represented by the 8 data bytes, of the format shown in Table 11.
FRR	AB	8-Output	**Filter - Receive - Read.** This instruction causes the device to output 8 data bytes which represent the 4 numbers corresponding to the 4 Receive Filter coefficients that have the format shown in Table 11.
FRW	A8	8-Input	**Filter - Receive - Write.** This instruction sets the 4 Receive Filter coefficients to the 4 numbers, represented by the 8 data bytes, of the format shown in Table 11.
FCC	BC to BF	None	**Filter - Cancellation - Control.** This instruction allows the automatic adaption of the C Filter to be enabled or disabled. There is a 2-bit field in the instruction which allows adaption to be enabled with or without polling the SI pin. The instruction has the format:- D7 D6 D5 D4 D3 D2 D1 D0 1 0 1 1 1 1 CD CA If CD is 1 then adaption of the C Filter is disabled. If CD is 0 then adaption is enabled if either CA is 1 or if the SI pin is high.
FCR	A3	20 - Output	**Filter - Cancellation - Read.** This instruction causes the device to output 20 data bytes which represent the 10 numbers corresponding to the 10 Cancellation Filter coefficients that have the format shown in Table 12.
FCW	A0	20 - Input.	**Filter - Cancellation - Write.** This instruction sets the 10 Cancellation Filter coefficients to the 10 numbers, represented by the 20 data bytes, of the format shown in Table 12.
FCDR	A1	2 - Output	**Filter - Cancellation - Double Talk - Read** This instruction causes the device to output 2 data bytes which represent the double talk detector coefficient as shown in Table 13.
FCDW	A2	2 - Input	**Filter - Cancellation - Double Talk - Write** This instruction sets the double-talk detector coefficient to the number represented by the two data bytes as shown in Table 13.

Table 10 : Filter Instructions.

DATA BYTE FORMAT									DATA DESCRIPTION
BYTE No.	BIT No. D7	D6	D5	D4	D3	D2	D1	D0	These bytes contain four 2's complement numbers each in the range ±2 which are used to construct the filter coefficients as follows:-
1	1	A_{31}	A_{30}	A_{3-1}	A_{3-2}	A_{3-3}	A_{3-4}	A_{3-5}	
2	1	A_{3-6}	A_{3-7}	A_{3-8}	A_{3-9}	A_{3-10}	X	X	$A_m = -A_{m1} \times 2^1 + A_{m0} \times 2^0 + A_{m-1} \times 2^{-1} + A_{m-2} \times 2^{-2} + ... + A_{m-10} 2^{-10}$
3	1	A_{21}	A_{20}	A_{2-1}	A_{2-2}	A_{2-3}	A_{2-4}	A_{2-5}	
4	1	A_{2-6}	A_{2-7}	A_{2-8}	A_{2-9}	A_{2-10}	X	X	with m = 0,1,2,3 for the four coefficients.
5	1	A_{11}	A_{10}	A_{1-1}	A_{1-2}	A_{1-3}	A_{1-4}	A_{1-5}	
6	1	A_{1-6}	A_{1-7}	A_{1-8}	A_{1-9}	A_{1-10}	X	X	The transfer function for the filters is:-
7	1	A_{01}	A_{00}	A_{0-1}	A_{0-2}	A_{0-3}	A_{0-4}	A_{0-5}	
8	1	A_{0-6}	A_{0-7}	A_{0-8}	A_{0-9}	A_{0-10}	X	X	$H(Z) = A_0 + A_1 Z^{-1} + A_2 Z^{-2} + A_3 Z^{-3}$
1 = +5V, X = Dont Care (0/1)									where the Z transformation is at 16KHz i.e. Z = exp(–i2πFT) with T = 1/16KHz

Table 11 : Transmit and Receive Filter Data bytes (Coefficients).

DATA BYTE FORMAT									DATA DESCRIPTION
BYTE No	BIT No D7	D6	D5	D4	D3	D2	D1	D0	These bytes contain ten 2's complement numbers each in the range ±2 which are used to construct the filter coefficients as follows:-
1	1	A_{81}	A_{80}	A_{8-1}	A_{8-2}	A_{8-3}	A_{8-4}	A_{8-5}	
2	1	A_{8-6}	A_{8-7}	A_{8-8}	A_{8-9}	A_{8-10}	X	X	$A_m = -A_{m1} \times 2^1 + A_{m0} \times 2^0 + A_{m-1} \times 2^{-1} + A_{m-2} \times 2^{-2} + ... + A_{m-10} 2^{-10}$
3	1	A_{61}	A_{60}	A_{6-1}	A_{6-2}	A_{6-3}	A_{6-4}	A_{6-5}	
4	1	A_{6-6}	A_{6-7}	A_{6-8}	A_{6-9}	A_{6-10}	X	X	with m = 0,1,2,3,...,9 for the ten coefficients.
5	1	A_{41}	A_{40}	A_{4-1}	A_{4-2}	A_{4-3}	A_{4-4}	A_{4-5}	
6	1	A_{4-6}	A_{4-7}	A_{4-8}	A_{4-9}	A_{4-10}	X	X	The transfer function for the filter is:-
7	1	A_{21}	A_{20}	A_{2-1}	A_{2-2}	A_{2-3}	A_{2-4}	A_{2-5}	
8	1	A_{2-6}	A_{2-7}	A_{2-8}	A_{2-9}	A_{2-10}	X	X	$H(Z) = A_0 + A_1 Z^{-1} + A_2 Z^{-2} + ... + A_8 Z^{-8} + \{[A_9 Z^{-9}] \div [16 - 15 Z^{-1}]\}$
9	1	A_{01}	A_{00}	A_{0-1}	A_{0-2}	A_{0-3}	A_{0-4}	A_{0-5}	
10	1	A_{0-6}	A_{0-7}	A_{0-8}	A_{0-9}	A_{0-10}	X	X	where the Z transformation is at 16KHz i.e. Z = exp(–i2πFT) with T = 1/16KHz
11	1	A_{91}	A_{90}	A_{9-1}	A_{9-2}	A_{9-3}	A_{9-4}	A_{9-5}	
12	1	A_{9-6}	A_{9-7}	A_{9-8}	A_{9-9}	A_{9-10}	X	X	Note that only the odd coefficients (A9, A7, A5, A3, A1) adapt. Bits listed as 1 = +5V and X = Dont Care (0/1).
13	1	A_{71}	A_{70}	A_{7-1}	A_{7-2}	A_{7-3}	A_{7-4}	A_{7-5}	
14	1	A_{7-6}	A_{7-7}	A_{7-8}	A_{7-9}	A_{7-10}	X	X	
15	1	A_{51}	A_{50}	A_{5-1}	A_{5-2}	A_{5-3}	A_{5-4}	A_{5-5}	
16	1	A_{5-6}	A_{5-7}	A_{5-8}	A_{5-9}	A_{5-10}	X	X	
17	1	A_{31}	A_{30}	A_{3-1}	A_{3-2}	A_{3-3}	A_{3-4}	A_{3-5}	
18	1	A_{3-6}	A_{3-7}	A_{3-8}	A_{3-9}	A_{3-10}	X	X	
19	1	A_{11}	A_{10}	A_{1-1}	A_{1-2}	A_{1-3}	A_{1-4}	A_{1-5}	
20	1	A_{1-6}	A_{1-7}	A_{1-8}	A_{1-9}	A_{1-10}	X	X	

Table 12 : C Filter Data bytes (Coefficients).

DATA BYTE FORMAT									DATA DESCRIPTION
BYTE No	BIT No D7	D6	D5	D4	D3	D2	D1	D0	These bytes are in the form of a 2's complement number in the range +/- 2.
1	1	A_1	A_0	A_{-1}	A_{-2}	A_{-3}	A_{-4}	A_{-5}	
2	1	A_{-6}	A_{-7}	A_{-8}	A_{-9}	A_{-10}	X	X	$A = -A_1 \times 2^1 + A_0 \times 2^0 + A_{-1} \times 2^{-1} .... + A_{-10} \cdot 2^{-10}$
1 = +5V, X = Dont Care (0,1)									The double talk detector compares the incoming RX signal level with the fixed error signal multiplied by the double talk coefficient (DTC)
									where DTC = 4 * A
									If the RX signal is the smaller then adaption is frozen.

Table 13 : Double Talk Detector bytes (Coefficient).

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
IOCR	C1	1-Output	**Digital I/O - Configuration - Read.** The data byte which is output by the device after this instruction indicates which of the Digital I/O pins are inputs, which are outputs. These have the the format:- D7 D6 D5 D4 D3 D2 D1 D0 CC1 CC2 CC3 CC4 CC5 X X X If CCn is 0 then the CPn pin is an output. If CCn is 1 then the CPn pin is an input (n = 1, 2, 3, 4, 5).
IOCW	D1	1-Input	**Digital I/O - Configuration - Write.** This instruction configures the Digital I/O pins to be inputs or outputs according to the input data byte which has the format:- D7 D6 D5 D4 D3 D2 D1 D0 CC1 CC2 CC3 CC4 CC5 R2 R1 R0 If CCn is 0 then the CPn pin is an output. If CCn is 1 then the CPn pin is an input (n = 1, 2, 3, 4, 5). Note the R2-R0 bits are reserved and should be set to 1, and that first application of power sets all Digital I/O pins to inputs.
IODR	C8	1-Output	**Digital I/O and Status Input - Data - Read.** The data byte which is output by the device after this instruction indicates the status of the Digital I/O pins, C filter Oscillation quench and SI pin. These have the format:- D7 D6 D5 D4 D3 D2 D1 D0 CP1 CP2 CP3 CP4 CP5 X Q SI If the CPn pin is configured as an input then the CPn bit is 1 or 0 depending on whether the input is high or low. If the CPn pin is configured as an output then the CPn bit is 1 or 0 depending on whether the output is high or low (n = 1, 2, 3, 4, 5). The Q bit will normally read 0. If loop oscillation has been detected and the pre-programmed coefficients returned to the adaptive filter then this bit will read 1. This command will reset the Q bit to 0. The SI bit is 1 (0) when the SI pin is high (low).
IODW	D8	1-Input	**Digital I/O - Data - Write.** This instruction controls the output levels of those Digital I/O pins configured as outputs according to the input data byte which has the format:- D7 D6 D5 D4 D3 D2 D1 D0 CP1 CP2 CP3 CP4 CP5 R2 R1 R0 If the CPn pin is configured as an output then it will go high or low depending on whether the CPn bit is 1 or 0. If the CPn pin is configured as an input then the corresponding CPn bit should be held at 0 (n = 1, 2, 3, 4, 5). Note the R2-R0 bits are reserved and should be set to 1.

Table 14 : Digital I/O and Status Input Instructions.

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
PC	B8 to BB	None	**PCM - Code.** This instruction defines the PCM coding scheme used by the device. The instruction has the format:- D7 D6 D5 D4 D3 D2 D1 D0 1 0 1 1 1 0 C1 C0 where C1, C0 select the coding scheme shown by the table:- C1C0 Code 0 0 Linear (16 bits) 0 1 μ-law (8 bits) 1 0 A-law (8 bits) 1 1 Reserved-do not use.
PAR	77	1-Output	**PCM - Association - Read.** The data byte output subsequent to this instruction indicates whether PCM data is associated with the A or B pins (DXA or DXB and DRA or DRB) and with the first or second segment of 256 bits. The data byte has the format:- D7 D6 D5 D4 D3 D2 D1 D0 X X X X R_B X_B R_{SA} X_{SA} $R_B = 1$ means the DRB pin is selected, $R_B = 0$ the DRA pin. $X_B = 1$ means the DXB pin is selected, $X_B = 0$ the DXA pin. If the R_{SA} bit is 0 then the receive segment address is 0 and the receive PCM is associated with the first segment of 256 bits (the standard condition). If it is 1 then the receive PCM is associated with the second segment of 256 bits (Expanded Mode). Likewise, if $X_{SA} = 0$, the segment address is 0 and the transmit PCM is associated with the first segment of 256 bits. If $X_{SA} = 1$ the transmit PCM is associated with the second segment of 256 bits.
PAW	90 to 9F	None	**PCM - Association - Write.** This instruction programs the PCM data association to the A or B pins (DXA or DXB and DRA or DRB) and to the first or second segment of 256 bits. The instruction has the format:- D7 D6 D5 D4 D3 D2 D1 D0 1 0 0 1 R_B X_B R_{SA} X_{SA} $R_B = 1$ selects the DRB pin, $R_B = 0$ selects the DRA pin. $X_B = 1$ selects the DXB pin, $X_B = 0$ selects the DXA pin. If the R_{SA} bit is 0 then the receive segment address is 0 and the receive PCM is associated with the first segment of 256 bits (the standard condition). If it is 1 then the receive PCM is associated with the second segment of 256 bits (Expanded Mode). Likewise, if $X_{SA} = 0$, the segment address is 0 and the transmit PCM is associated with the first segment of 256 bits. If $X_{SA} = 1$ the transmit PCM is associated with the second segment of 256 bits.

Table 15 : PCM Instructions.

MNEMONIC	CONTROL CODE (HEX)	ASSOCIATED DATA BYTES	CONTROL CODE DESCRIPTION
DR	B0	None	**Diagnostic - Reset.** This instruction clears any diagnostic conditions that are set up.
DHD	B3	None	**Diagnostic - High Pass Filter - Disable.** This instruction disables the 50/60Hz notch and DC reject filters.
DRA	B1	None	**Diagnostic - Receive - Attenuate.** This instruction adds 6dB attenuation to the Receive Path.
DRD	B2	None	**Diagnostic - Receive - Disable Path.** This instruction disables the Receive Path. This means that $V_{OUT} = V_{OO}$ regardless of the receive PCM data input to the device.
DLA	B7	None	**Diagnostic - Loop - Analog.** This instruction sets the MV3010-1 to Analog Loop Test Mode which internally switches the transmit signal from D_2 to I_1 (see Fig.3), to the VOUT pin, instead of the normal PCM receive data (Note 1).
DLD	B4	None	**Diagnostic - Loop - Digital.** This instruction sets the MV3010-1 to Digital Loop Test Mode. The Expander output is switched to the Compressor input such that input PCM replaces the normal PCM output (Note 1).
DCD	B5	None	**Diagnostic - Correlator - Disable.** This instruction disables the signal correlator associated with the adaptive cancellation algorithm. This may be done for test purposes or to allow pre-programming using the measurement method.

Notes :- 1. DLA and DLD are mutually exclusive. Selecting one loop Test mode resets the other.

Table 16 : Diagnostic Instructions.

APPLICATIONS

The circuit schematic of Figure 13 shows the basic application for the MV3010-1 in a Line Card architecture. This circuit uses one of the GEC Plessey Subscriber Line Interface Circuits (SLIC) to interface to the 2 wire (subscriber) Line. For details on how these devices are used to control the line status and transmission parameters, separate Data Sheets are available for the SL373, SL376, SL7950, and SL7953 SLICs, in addition to further applications information in Applications Note AN82.

Both analog and digital interfacing is shown in Figure 13. The analog input is kept about 0V due to the low impedance output of the SLIC, and the DC bias of the analog output is blocked by the series capacitor, C5. Networks Z_{TX} and Z_{GR} are used to set nominal Transmit and Receive impedances of the Line Card respectively, as discussed in the related documents mentioned earlier. Modifications to gains and frequency response can be carried out in the MV3010-1 as described in the Functional Description section. Note that in order to ensure the MV3010-1 meets/exceeds all CCITT transmission parameters (see Electrical Characteristics), the split supply pins are separately routed and decoupled at the system power supplies. This reduces coupling of any digital switching transients into the analog path. Optimum transmission performance is achieved when using the supply decoupling components shown.

AV_{CC} should always be provided at the same time as or before DV_{CC} , application of DV_{CC} before AV_{CC} should be avoided. Note that this restriction is necessary as the chip substrate is connected to AV_{CC} and its correct biasing is required to ensure parasitic component latch-up does not occur. Voltage differences between the two power supplies after power-on initialisation should be minimised. It is recommended that they are supplied from the same source.

The SLIC digital inputs are DC level controlled, TTL compatable and control the SLIC functions as described in the related Data Sheets. Since the MV3010-1 has latched outputs (programmed as outputs), then the SLIC inputs can be directly connected to the MV3010-1 in any order. The DETB output of the SLIC can also be connected directly to the MV3010-1. Thus, the SLIC operating modes are controlled via the MV3010-1 I/O pins and the Line Status read via the SI pin. The Line Card is now fully controlled via the MV3010-1 Control Interface, with microprocessor/controller interface options as described in Applications Note AN42.

The PCM Interface can be configured to give a variety of system architectures. This is also discussed further in PABX/Line Card Control Circuit Applications Note AN42.

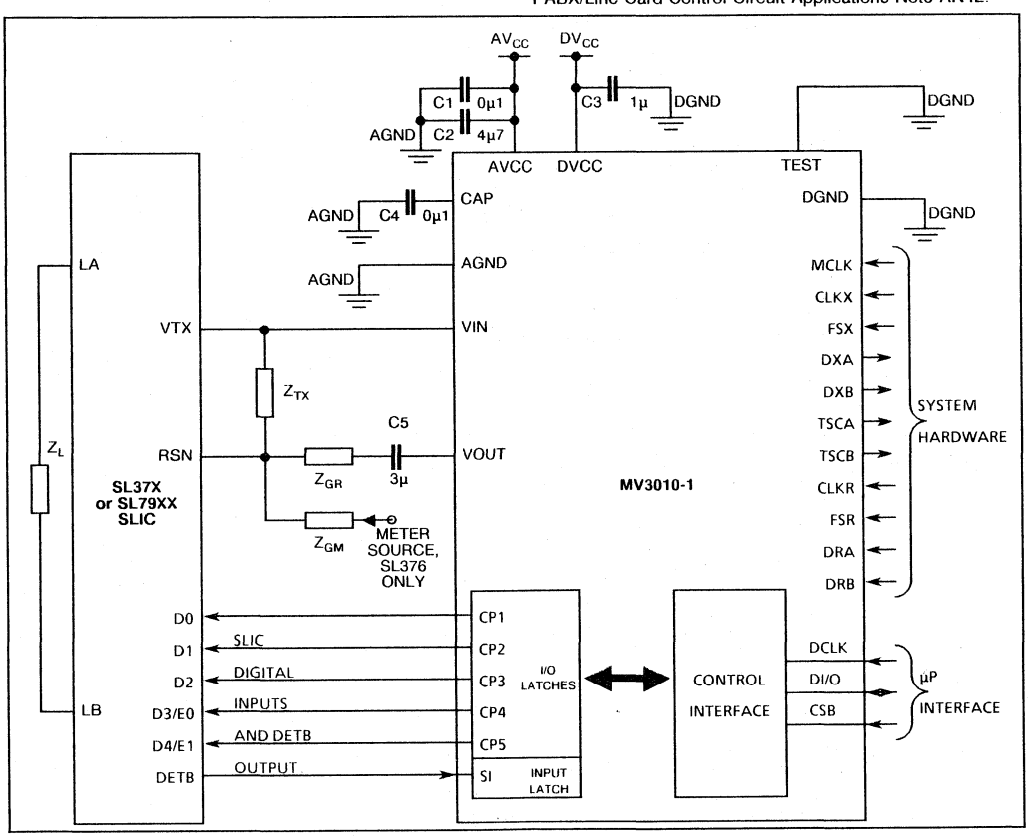


Fig. 13 : Line Card Application Circuit showing SLIC Interface.

PIN DESCRIPTIONS

SYMBOL	PIN No	PIN NAME AND DESCRIPTION
CAP	1	**Capacitor (Analog Node).** A capacitor of 0.1µF should be connected between this pin and analog ground (AGND pin). This is used to decouple the internal voltage reference.
VIN	2	**Input Voltage (Analog Input).** The analog voltage input at this pin is sampled, processed, digitally encoded and then output as PCM data on either DXA or DXB. This signal is referenced to AGND and there is an input impedance of 30KΩ to $\frac{2}{3}V_{REF}$ (≈ 1.66V).
AGND	3	**Analog Ground (Power Input).** This is the ground reference pin for the analog input (VIN pin) and analog output (VOUT pin). Care should be taken to minimise the noise at this pin.
VOUT	4	**Output Voltage (Analog Output).** The analog voltage at this pin is derived from the PCM data input on either DRA or DRB. This PCM data is processed digitally, decoded, converted to analog and then output here. This signal is referenced to AGND but has a DC offset of nominally 2.5V.
SI	5	**Status In (Digital Input).** The data sampled at this input can be read out on the DI/O pin. This allows information about the status of the telephone line to be passed on to a line card controller. This pin can also be used to control the operation of the C-Filter (see Table 10).
CP1 CP2 CP3 CP4 CP5	6 7 8 9 10	**Control Port 1 to 5 (Digital I/O with Pullups).** These pins are independently programmable as either inputs or outputs through the control stream input on DI/O. Pins which are programmed as outputs are also controlled by DI/O. Pins which are programmed as inputs can be read on DI/O. There are pullups of 100KΩ on these pins. These pins allow a line card controller to monitor and control the line card via the MV3010-1 and mean that a single hardware design for a line card can be configured through software for a number of different requirements.
TSCA TSCB	11 18	**Time Slot Control A, B (Open Drain Pulldown Outputs).** The TSCA or TSCB pins are pulled low when PCM data is output on DXA or DXB respectively. These pins on different devices may be connected together with a single pull-up resistor (wire-ored) to generate an enable signal for an output buffer on a line card.
DXA DXB	12 17	**Digital Transmit A, B (Three-State Outputs).** These are the PCM data outputs, which can be 8 bit µ-law, 8 bit A-law or 16 bit linear code. Either DXA or DXB is used as programmed via the serial control input at DI/O. Bit and frame synchronisation are established by CLKX and FSX with the start of the PCM burst relative to FSX determined by serial Control Codes via DI/O. A PCM data word is output once every 125µs, with the pins high impedance between PCM bursts and in Power-Down Mode.
TEST	13	**Test Pin (Internal Connection).** This pin must be connected to DGND during normal operation.
DRA DRB	14 21	**Digital Receive A, B (Digital Inputs).** These are the PCM data inputs, which can be 8 bit µ-law, 8 bit A-law or 16 bit linear coding. Either DRA or DRB is used as programmed via the serial control input at DI/O. Bit and frame synchronisation are established by CLKR and FSR, with the position of the first sampled bit relative to FSR determined by serial Control Codes via DI/O. A data word is sampled once every 125µs.
CLKX	15	**Transmit Clock (Digital Input).** The clock input at this pin establishes bit synchronisation of the PCM data output on DXA and DXB. The clock frequency must be between 64KHz and 4.096MHz and there must be an integral number of clock cycles between pulses on FSX. This clock should be phase locked to MCLK.
FSX	16	**Transmit Frame Synchronisation (Digital Input).** The pulse input at this pin establishes the frame synchronisation of the PCM data output on DXA and DXB. There should be 125µs between pulses and the pulses should be synchronised with CLKX.
CLKR	19	**Receive Clock (Digital Input).** The clock input at this pin strobes the samples of PCM data input on DRA and DRB. The clock frequency must be between 64KHz and 4.096MHz with an integral number of cycles between FSR pulses. This clock should be phase locked to MCLK.
FSR	20	**Receive Frame Synchronisation (Digital Input).** The pulse input at this pin establishes the frame synchronisation on the PCM data input on DRA and DRB. There should be 125µs between pulses and the pulses should be synchronised with CLKR.
DGND	22	**Digital Ground (Power Input).** 0 Volts Supply.
CSB	23	**Chip Select Bar (Digital Input).** This input should be taken low to enable the chip to input or output serial Control or Data bytes, via DI/O, when strobed with DCLK. If held low for more than 8 cycles of DCLK it will force the device into stand-alone operation.
DI/O	24	**Data In/Out (Digital Input/Output).** Serial Control Codes and Data Bytes are input and output via this pin when CSB is low. Input data is sampled by DCLK and output data is clocked out by DCLK. A common data input/output line can be used by a number of devices.
DCLK	25	**Data Clock (Digital Input).** This clock strobes serial input and clocks serial output data via DI/O, in association with the CSB pin. The clock can run at frequencies from DC to 2.048MHz.
MCLK	26	**Master Clock (Digital Input).** This clock controls the sampling for the A/D conversion, signal reconstruction for the D/A conversion, the DSP functions and must be 2.048MHz phase locked with CLKX and CLKR.
DVCC	27	**Digital Positive Supply Voltage (Power Input).** 5 Volts.
AVCC	28	**Analog Positive Supply Voltage (Power Input).** 5 Volts.

RECOMMENDED OPERATING CONDITIONS

Voltages are with respect to analog ground (V_{AGND}).

Parameter	Symbol	Value			Units
		Min.	Typ.	Max.	
Analog Supply Voltage	AV_{CC}	4.75	5	5.25	Volts
Digital Ground Voltage	V_{DGND}	-0.1	0	0.1	Volts
Digital Supply Voltage	DV_{CC}	4.75	5	5.25	Volts
Ambient Temperature	T_{AMB}	0		70	°C
Output Loading	C_O			150	pF

ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless otherwise specified) :-

Supply Characteristics -Voltages are with respect to analog ground (V_{AGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Active Supply Current (Power-Up Mode)	I_{CCA}		24	36	mA	Unloaded
Standby Supply Current (Power-Down Mode)	I_{CCS}		4	6	mA	Unloaded
Analog Power Supply (AV_{CC}) Rejection Ratio, VIN/VOUT	P_{SRA}	35	50		dB	f = 1.02KHz, 200mV pk-pk on supply, Note 1.
Digital Power Supply (DV_{CC}) Rejection Ratio, VIN/VOUT	P_{SRD}	35	50		dB	f = 1.02KHz, 200mV pk-pk on supply, Note 1.
Power Supply Rise Time (AV_{CC} and DV_{CC})	P_{RT}			10	V/µS	Over any part of the power supply ramp, 10% -90%

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Notes 1. For Transmit Path the digital output signal is converted to an equivalent signal amplitude at VIN.

Analog Static Characteristics - Voltages are with respect to analog ground (V_{AGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Pin Capacitance	C_P		8	10	pF	$0<V<AV_{CC}$, DV_{CC}
VIN Input Impedance	Z_I	20	30		KΩ	$-3V<V<+3V$
VIN Input Bias	V_{BI}		$\frac{2}{3}V_{REF}$		V	V_{REF} Internal Reference = 2.5V, VIN = O/C
VIN Input Offset Voltage	V_{IO}	-30		+30	mV	Note 1.
VIN Input Voltage Range	V_{IA}	-3		+3	V	
VOUT Output Impedance	Z_O			20	Ω	$1V<V<4V$
VOUT Output Offset Voltage	V_{OO}	2.3	2.5	2.7	V	
VOUT Output Voltage Range	V_{OA}	V_{OO}-1.5		V_{OO} + 1.5	V	R_L = 10kΩ, C_L = 50pF

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Notes. 1. Full functional operation is possible with $-0.25V \le V_{IO} \le +0.25V$, full transmission performance is not guaranteed.

Analog Dynamic Characteristics - Voltages are with respect to analog ground (V_{AGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Absolute Gain	G_{ABS}	-0.15 -0.2		+0.15 +0.2	dB dB	Transmit or Receive Path, Transmit + Receive Paths, f = 1.02KHz sine, 0dBm0 Signal Level
Transmit 0dBm0 Level	V_{TO}	4.11 4.08	4.18 4.15	4.25 4.22	$V_{P/P}$	A-Law μ-Law
Receive 0dBm0 Level	V_{RO}	2.05 2.04	2.09 2.075	2.12 2.11	$V_{P/P}$	A-Law μ-Law
Transmit Gain	G_T			13	dB	All CCITT G.714 Specifications - as Listed in the following rows
Receive Gain	G_R	-12			dB	All CCITT G.714 Specifications - as Listed in the following rows
Frequency Response, Transmit (As CCITT G.714.7, see Figure 14) F = 0Hz = 50 = 60 = 200 = 300-3000 = 3300 = 3400 = 4000 >4600	FR_T	- - - -1.0 -0.125 -0.35 -0.8 - -		-80 -25 -25 0.0 +0.125 +0.125 0.0 -17.5 -35.0	dB dB dB dB dB dB dB dB dB	Note 1, Note 3, Reference = 1KHz 0dBm0 signal level.
Frequency Response Receive (As CCITT G.714.7,see Figure 14) F = 0Hz = 200 = 300-3000 = 3300 = 3400 = 4000 >4600	FR_R	- -1.0 -0.125 -0.35 -0.8 - -		-80 0.0 +0.125 +0.125 0.0 -17.5 -35.0	dB dB dB dB dB dB dB	Note 2, Note 3, Reference = 1KHz 0dBm0 signal level.
Absolute Group Delay, Transmit	GD_{AT}			300	μs	Note 1, Note 3, Note 4, Min. Delay 1K to 2K6Hz
Absolute Group Delay, Receive	GD_{AR}			200	μs	Note 2, Note 3, Note 4, Min. Delay 1K to 2K6Hz
Delay Distortion, Transmit (Figure 15) F = 500-600Hz = 600-1000 = 1000-2600 = 2600-2800	DD_T			700 350 120 700	μs μs μs μs	Note 1, Note 3, Relative to the Minimum Delay of the Transmit side.
Delay Distortion, Receive (Figure 15) F = 500-600Hz = 600-1000 = 1000-2600 = 2600-2800	DD_R			700 350 120 700	μs μs μs μs	Note 2, Note 3, Relative to the Minimum Delay of the Receive side.

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Notes:- 1. G_X = 0 to +13dB.

2. G_R = 0 to -12dB.

3. All programmable filters disabled.

4. Over the full range of Time Slots and Clock Offsets

Analog Dynamic Characteristics - continued - Voltages are with respect to analog ground (V_{AGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Idle Channel Noise, Transmit	NI_{TA} $NI_{T\mu}$			-68 -75	dBm0p dBm0p	A-law Psophometrically μ-law Weighted, Note 1.
Idle Channel Noise, Receive	NI_R			-84	dBmp	Psophometrically Weighted, Note2, Note 6.
Idle Channel Noise, Single Frequency, Transmit	NI_{TS}			-50	dBm0	200Hz to 3800Hz, Note 1.
Idle Channel Noise, Single Frequency, Receive	NI_{RS}			-50	dBm	200Hz to 3800Hz, Note 2.
Out of Band Signal Rejection 4600Hz-72KHz, Transmit	RJ_{TH}	35			dB	Note 1, V_{IN} = -25dBm0
Out of Band Signal Generation, Receive 4600Hz-100KHz	GN_{RH}			-35	dBm0	Note 2, PCM In 0dBm0, 300-3K4Hz
Spurious In Band Signals, Transmit	GN_{TL}			-46	dB	Applied f = 700-1100Hz, 0dBm0, Note 1.
Spurious In Band Signals, Receive	GN_{RL}			-46	dB	Applied f = 700-1100Hz, 0dBm0, Note 2.
Intermodulation Distortion, Transmit or Receive	IM_{RX1} IM_{RX2}			-35 -49	dB dBm0	Note 1, Note 2, Note 7. Note 1, Note 2, Note 8.
Transmit Gain Variation with Level, sinusoid input (As CCITT G.714.15 method 2, see Figure 16)	G_{XLS}	-0.2 -0.4 -1.2		+0.2 +0.4 +1.2	dB dB dB	+3 to -40dBm0 }-10dBm0 -40 to -50dBm0 }Ref. -50 to -55dBm0 }Level. Note 1, Note 3, Note 4.
Transmit Gain Variation with Level, band limited noise (CCITT O.131) input (As CCITT G.714.15 method 1, see Figure 17)	G_{XLN}	-0.2 -0.3 -0.4		+0.2 +0.2 +0.2	dB dB dB	-10 to -45dBm0 }-10dBm0 -45 to -50dBm0 }Ref.Level -50 to -55dBm0 } Note 3, Note 5.
Transmit Gain Variation with Level, band limited noise (CCITT O.131) input (As CCITT G.714.15 method 1, see Figure 17)	G_{XLNA}	-0.2 -0.3 -0.4		+0.2 +0.3 +0.4	dB dB dB	-10 to -45dBm0 }-10dBm0 -45 to -50dBm0 }Ref.Level -50 to -55dBm0 } +12dB < $G_X \leq$ +13dB, Note 3.

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Notes:-
1. G_X = 0 to +13dB.
2. G_R = 0 to -12dB.
3. All programmable filters are disabled.
4. Non-production test. Figures are included for guidance only.
5. G_X = 0 to +12dB.
6. μ-Law coding = +0 code, A-Law coding = +1 code.
7. Two frequencies f1 and f2 in the range 300 to 3400Hz and of equal levels in the range -4 to -21dBm0. 2f1-f2 products are measured relative to either f1 or f2.
8. Any intermodulation product due to a signal in the range 300 to 3400Hz with input level -9dBm0 and a 50Hz signal with input level -23dBm0.

Analog Dynamic Characteristics - continued - Voltages are with respect to analog ground (V_{AGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Receive Gain Variation with Level, sinusoid input (As CCITT G.714.15 method 2, see Figure 16)	G_{RLS}	-0.2 -0.4 -1.2		+0.2 +0.4 +1.2	dB dB dB	+3 to -40dBm0 }-10dBm0 -40 to -50dBm0 }Ref. -50 to -55dBm0 }Level. Note 2, Note 3, Note 4
Receive Gain Variation with Level, band limited noise (CCITT O.131) input (As CCITT G.714.15 method 1, see Figure 17)	G_{RLN}	-0.2 -0.3 -0.4		+0.2 +0.4 +0.7	dB dB dB	-10 to -45dBm0}-10dBm0 -45 to -50dBm0 }Ref.Level -50 to -55dBm0 } Note 2, Note 3.
Transmit Gain Variation with Supplies	G_{XVCC}		0.05		dB/V	AV_{CC} ± 5%, DV_{CC} ± 5%, Note 1.
Receive Gain Variation with Supplies	G_{RVCC}		0.05		dB/V	AV_{CC} ± 5%, DV_{CC} ± 5%, Note 2.
Transmit Gain Variation with Temperature	G_{XTMP}	-0.1		+0.1	dB	T_A = 0-70°C, Note 1.
Receive Gain Variation with Temperature	G_{RTMP}	-0.1		+0.1	dB	T_A = 0-70°C, Note 2.
Signal to Total Distortion Ratio Transmit, noise (CCITT O.131) input (As CCITT G.714.14 method 1, see Figure 19)	STD_{TX1}	27.0 34.6 32.9 28.3 13.3			dB dB dB dB dB	-3dBm0 } -6 to -27dBm0 }Note 1, -34dBm0 }Note 3. -40dBm0 } -55dBm0 }
Signal to Total Distortion Ratio Transmit, sinusoid input. (As CCITT G.714.14, method 2, see Figure 18)	STD_{TX2}	35 29 24			dB dB dB	0 to -30dBm0 } -40dBm0 }f = 1020Hz -45dBm0 } Note 1, Note 3, Note 4.
Signal to Total Distortion Ratio Receive, noise (CCITT O.131) input (As CCITT G.714.14, method 1, see Figure 19)	STD_{RX1}	28.0 35.6 33.8 29.1 14.1			dB dB dB dB dB	-3dBm0 } -6 to -27dBm0 }Note 2, -34dBm0 }Note 3. -40dBm0 } -55dBm0 }
Signal to Total Distortion Ratio Receive, sinusoid input. (As CCITT G.714.14 method 2, see Figure 18)	STD_{RX2}	36 30 25			dB dB dB	0 to -30dBm0 } -40dBm0 }f = 1020Hz -45dBm0 } Note 2, Note 3, Note 4.
Crosstalk, Transmit to Receive	XT_{TR}			-70	dB	Note 1, Note 2, Note 3.
Crosstalk, Receive to Transmit	XT_{RT}			-70	dB	Note 1, Note 2, Note 3.

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Notes:- 1. G_X = 0 to +13dB.
2. G_R = 0 to -12dB.
3. All programmable filters are disabled.
4. Non-production test. Figures are included for guidance only.

Digital Static Characteristics - Voltages are with respect to digital ground (V_{DGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Input Leakage Current	I_{IL}			10	µA	$0<V<DV_{CC}$
Output High Voltage	V_{OH}	4.0		DV_{CC}	V	I_{OH} (Source) = –2mA
Output Low Voltage	V_{OL}	0		0.4	V	I_{OL} (Sink) = 2mA
Output Leakage Current	I_{OL}			10	µA	$0<V<DV_{CC}$
Input High Voltage	V_{IH}	2.8		DV_{CC}	V	
Input Low Voltage	V_{IL}	0	0.4	0.8	V	

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Digital Dynamic Characteristics - Voltages are with respect to digital ground (V_{DGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Master Clock Period	t_{MCP}	0.48826	0.48828	0.48831	µs	Figure 20.
Master Clock Rise Time	t_{MR}		20		ns	Figure 20.
Master Clock High Time	t_{MH}	50	236		ns	Figure 20.
Master Clock Fall Time	t_{MF}		20		ns	Figure 20.
Master Clock Low Time	t_{ML}	50	236		ns	Figure 20.
Transmit PCM Clock Period	t_{TCP}	244	488	15626	ns	Figure 22.
Transmit PCM Clock Rise Time	t_{TCR}			20	ns	Figure 22.
Transmit PCM Clock High Time	t_{TCH}	100			ns	Figure 22.
Transmit PCM Clock Fall Time	t_{TCF}			20	ns	Figure 22.
Transmit PCM Clock Low Time	t_{TCL}	100			ns	Figure 22.
Transmit PCM Frame Sync. Set-up Time	t_{TFS}	50			ns	Figure 22.
Transmit PCM Frame Sync. Hold Time	t_{TFH}	30			ns	Figure 22.
Transmit PCM Active Delay	t_{TAD}	55		170	ns	Figure 22.
Transmit PCM Passive Delay	t_{TPD}			50	ns	Figure 22.
Transmit PCM Output Hold Time	t_{TOH}	2			ns	Figure 22.
Transmit PCM Output Delay	t_{TOD}			100	ns	Figure 22.
TSC Low Delay	t_{TLD}			150	ns	Figure 22.
TSC High Delay	t_{THD}			150	ns	Figure 22.

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Digital Dynamic Characteristics - continued - Voltages are with respect to digital ground (V_{DGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
Receive PCM Clock Period	t_{RCP}	244	488	15626	ns	Figure 21.
Receive PCM Clock Rise Time	t_{RCR}			20	ns	Figure 21.
Receive PCM Clock High Time	t_{RCH}	100			ns	Figure 21.
Receive PCM Clock Fall Time	t_{RCF}			20	ns	Figure 21.
Receive PCM Clock Low Time	t_{RCL}	100			ns	Figure 21.
Receive PCM Frame Sync. Set-up Time	t_{RFS}	50			ns	Figure 21.
Receive PCM Frame Sync. Hold Time	t_{RFH}	30			ns	Figure 21.
Receive PCM Input Set-up Time	t_{RIS}	50	$\frac{1}{2}t_{RCP}$		ns	Figure 21.
Receive PCM Input Hold Time	t_{RIH}	0	$\frac{1}{2}t_{RCP}$		ns	Figure 21.
Data Clock Period	t_{DCP}	450			ns	Figures 23 & 24.
Data Clock Rise Time	t_{DCR}		25	50	ns	Figures 23 & 24.
Data Clock High Time	t_{DCH}	150			ns	Figures 23 & 24.
Data Clock Fall Time	t_{DCF}		25	50	ns	Figures 23 & 24.
Data Clock Low Time	t_{DCL}	150			ns	Figures 23 & 24.
Chip Select Falling Hold Time	t_{CFH}	150			ns	Figures 23 & 24.
Chip Select Falling Set-up Time	t_{CFS}	50			ns	Figures 23 & 24.
Chip Select Rising Hold Time	t_{CRH}	50			ns	Figures 23 & 24.
Chip Select Rising Set-up Time	t_{CRS}	50			ns	Figures 23 & 24.
Chip Select Low Time	t_{CLT}		$8t_{DCP}$		ns	Figures 23 & 24, Note 1.
Chip Select High Time, Input Mode	t_{CIT}	$7 \times t_{MCP}$			ns ns	Command or Data codes } Figure 23.
Chip Select High Time, Output Mode	t_{COT}	$7 \times t_{MCP}$			ns ns	Command or Data codes } Figure 24.

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

Notes:- 1. If CSB is tied low then the MV3010-1 will operate in Stand Alone Mode.

Digital Dynamic Characteristics - continued - Voltages are with respect to digital ground (V_{DGND}).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.*	Max.		
DI/O Input Set-up Time	t_{DIS}	50	$t_{DCP}/2$		ns	Figure 23.
DI/O Input Hold Time	t_{DIH}	30	$t_{DCP}/2$		ns	Figure 23.
DI/O Active Delay	t_{DAD}			100	ns	Figure 24.
DI/O Passive Delay	t_{DPD}			100	ns	Figure 24.
DI/O Output Hold Time	t_{DOH}	30	50		ns	Figure 24.
DI/O Output Delay	t_{DOD}		100	150	ns	Figure 24.
CP1-CP5 I/O Output Mode, Data False Delay Time	t_{LOF}	0			ns	Figure 25.
CP1-CP5 I/O Output Mode, Data Valid Delay Time	t_{LOV}			$4 \times t_{MCP}$	ns	Figure 25.
CP1-CP5 I/O Input Mode and SI pin, Data Set-up Time	t_{LIS}	0			ns	Figure 25.
CP1-CP5 I/O Input Mode and SI pin, Data Hold Time	t_{LIH}	$4 \times t_{MCP}$			ns	Figure 25.

* Typical figures are for design aid only. They are not guaranteed and not subject to production testing.

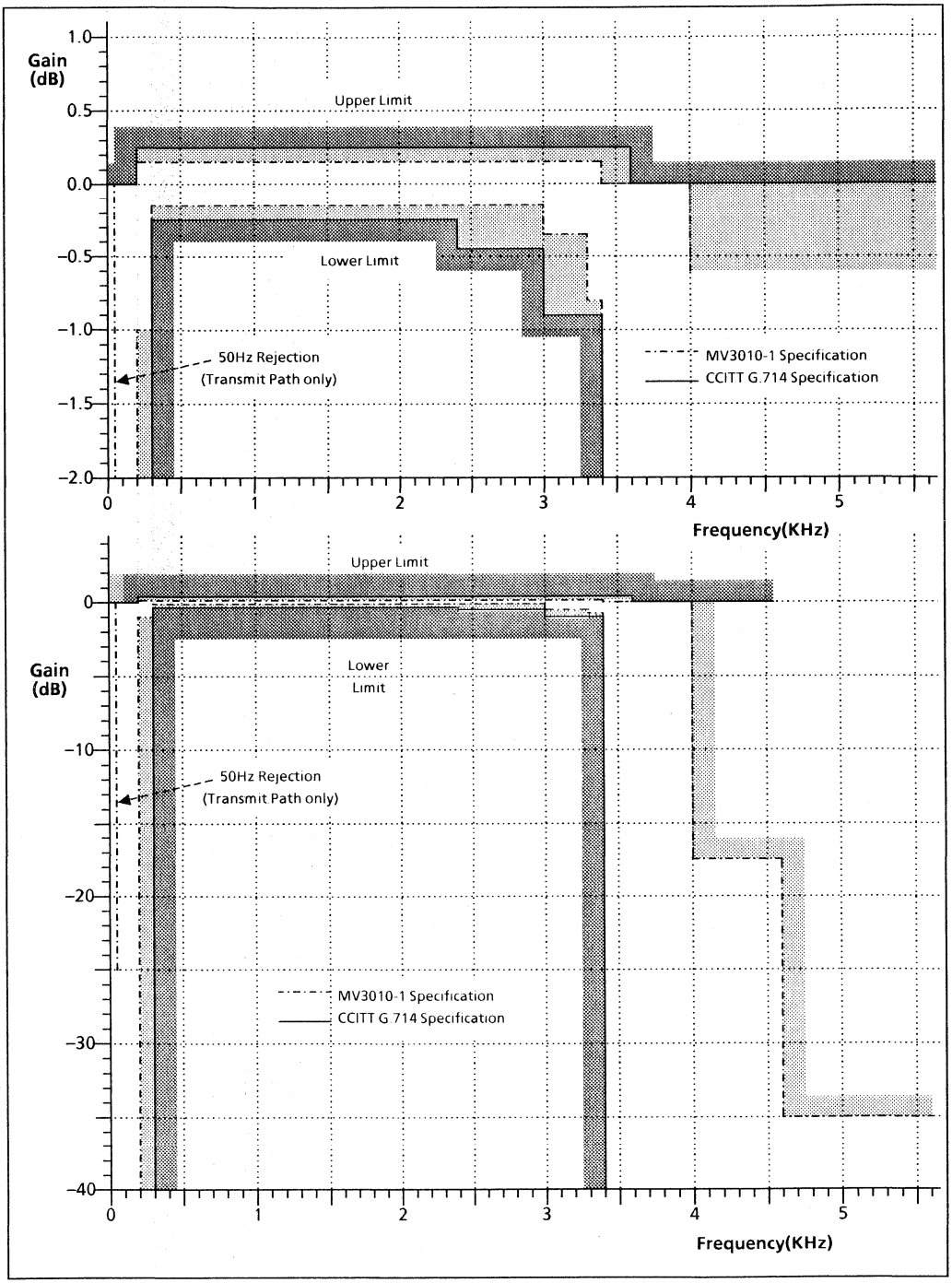


Figure 14 : MV3010-1 Frequency Response.

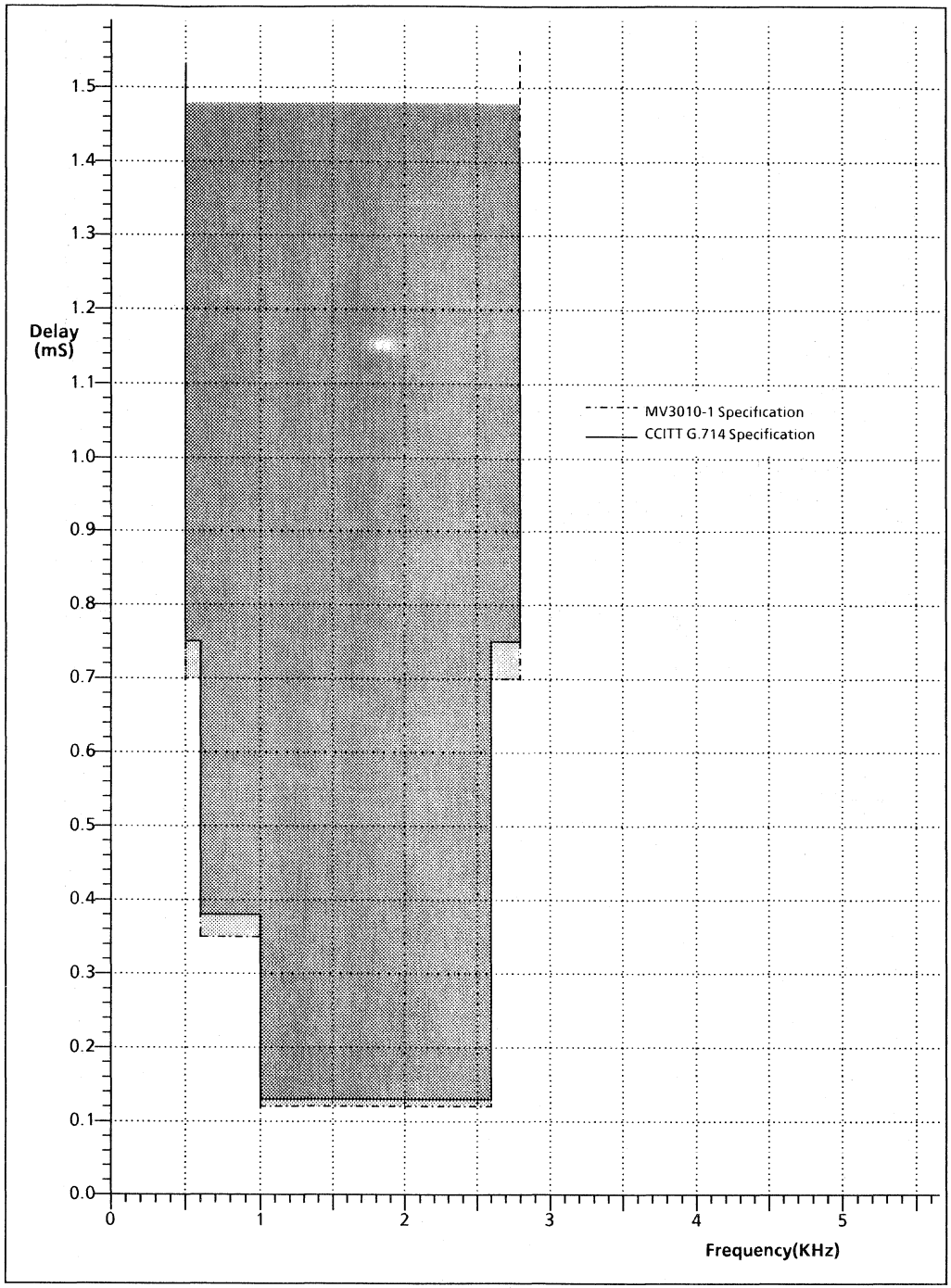


Figure 15 : MV3010-1 Delay Distortion vs Frequency.

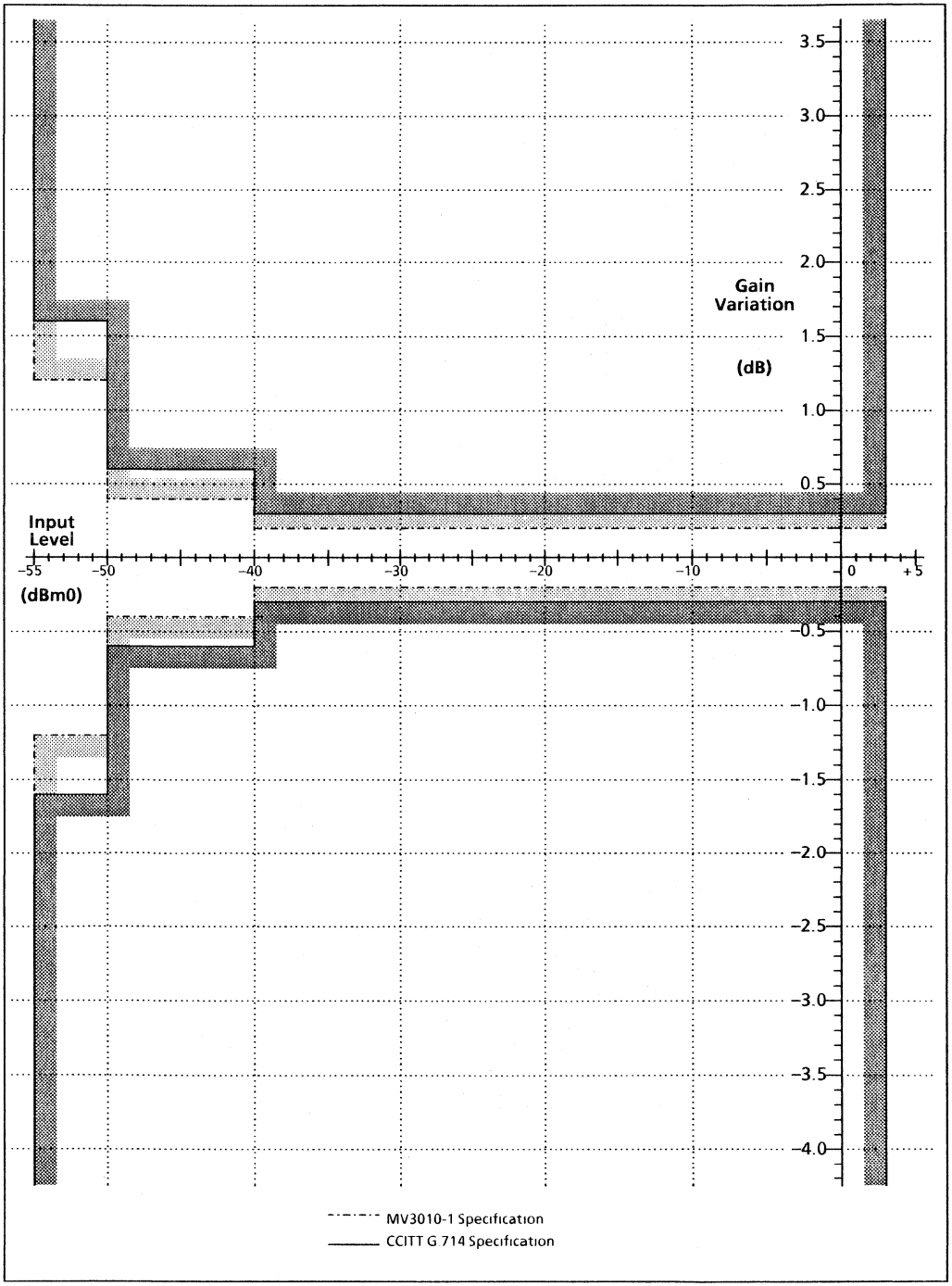


Figure 16 : MV3010-1 Gain Variation vs Level (Sinusoid - Method 2 CCITT G.714.15).

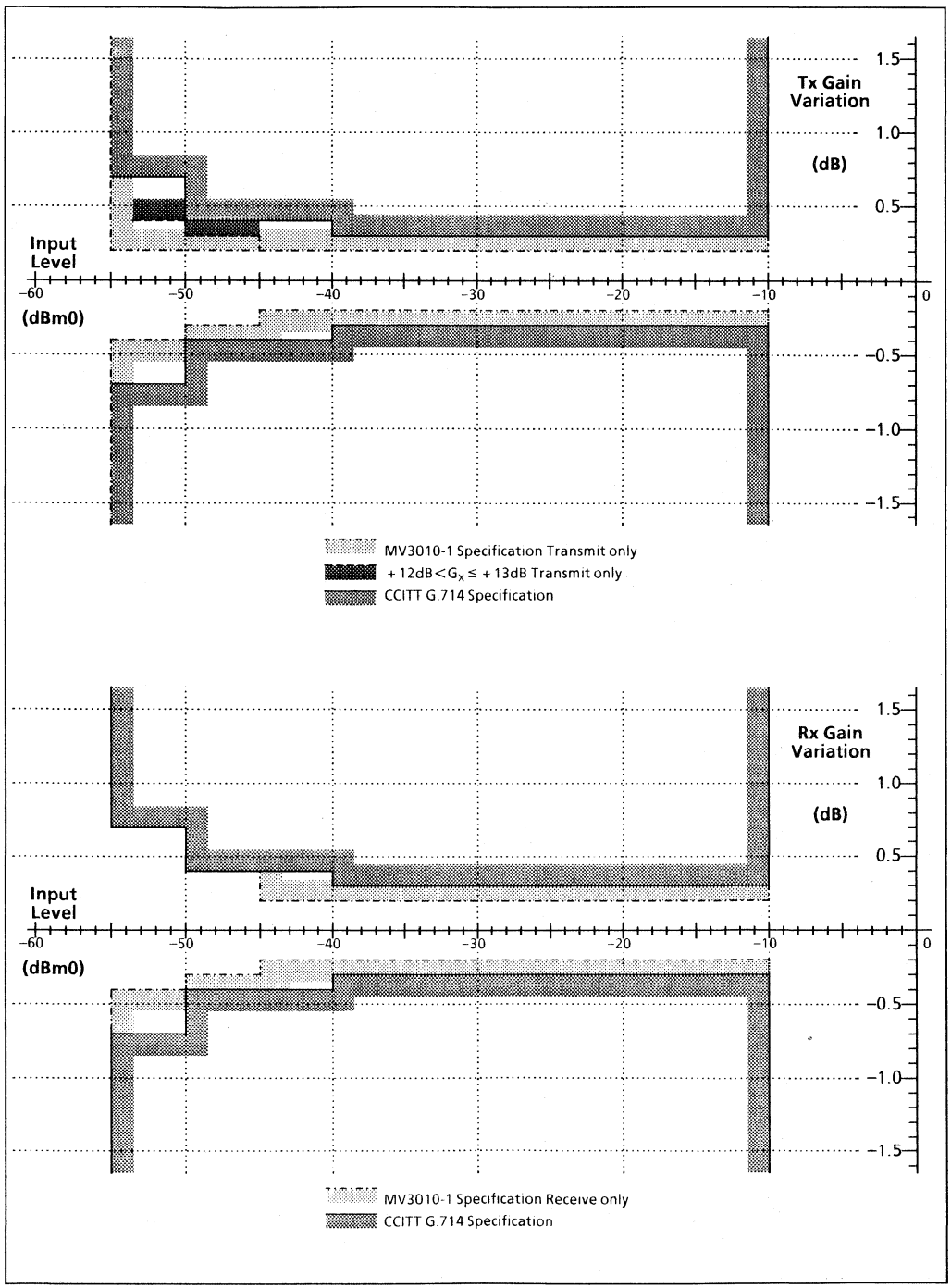


Figure 17 : MV3010-1 Gain Variation vs Level (Noise, O.131 - Method 1 CCITT G.714.15).

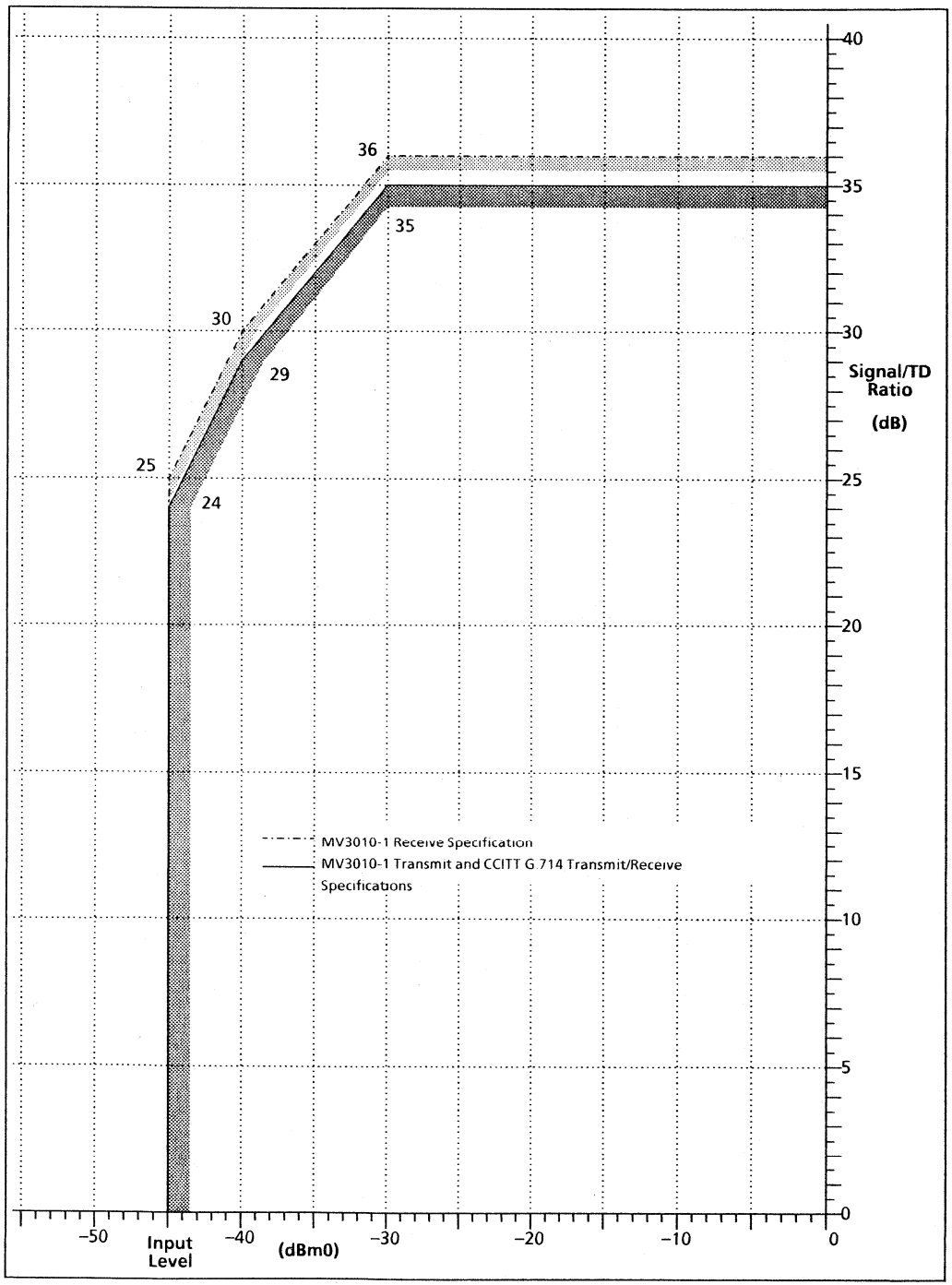


Figure 18 : MV3010-1 Signal to Total Distortion Ratio vs Level (Sinusoid Method 2 CCITT G.714.14).

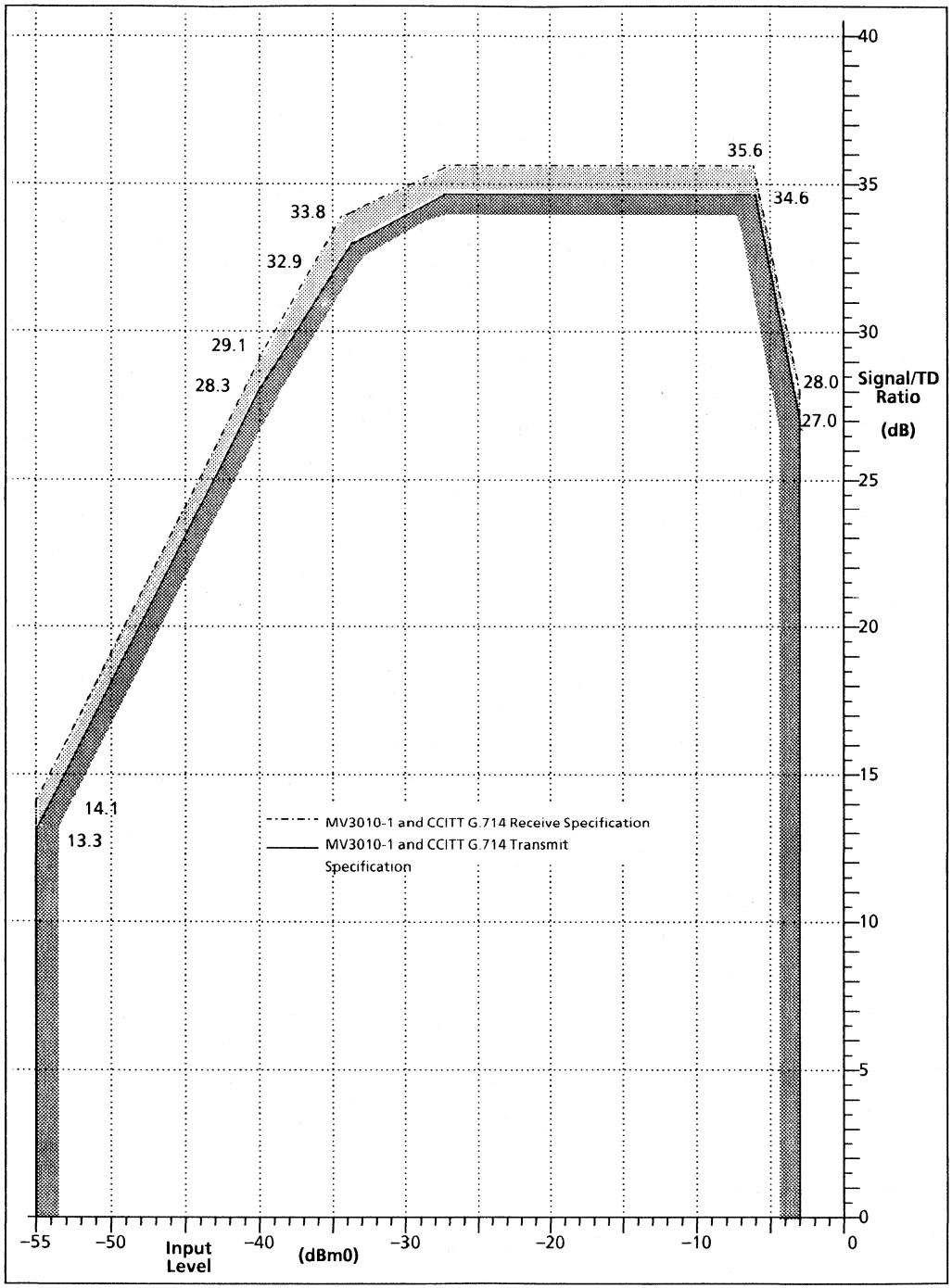


Figure 19 : MV3010-1 Signal to Total Distortion Ratio vs Level (Noise, 0.131 - Method 1 CCITT G.714.14).

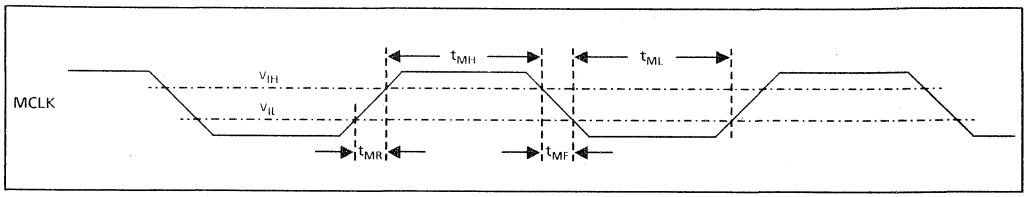


Figure 20 : Master Clock Timing Diagram.

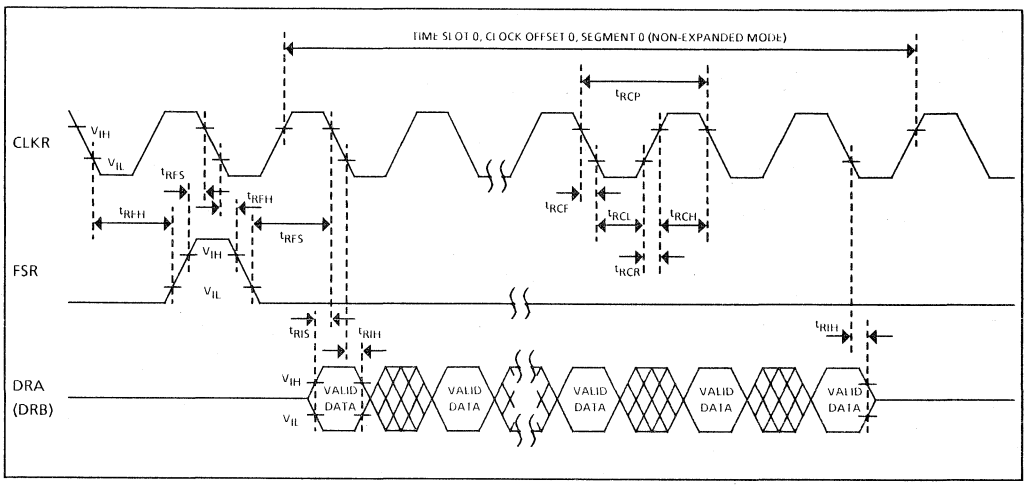


Figure 21 : PCM Data Receive Timing Diagram.

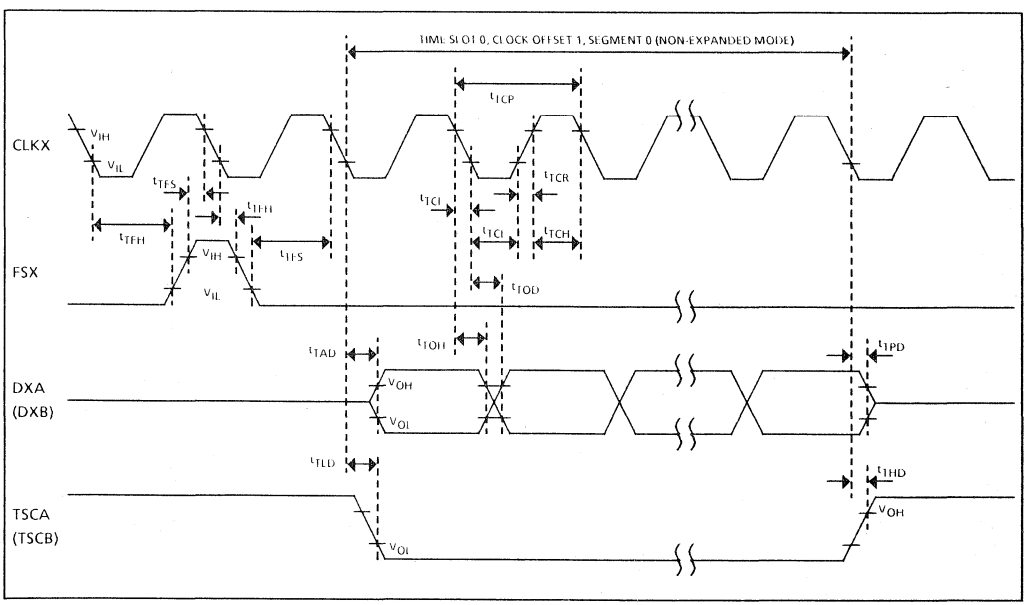


Figure 22 : PCM Data Transmit Timing Diagram.

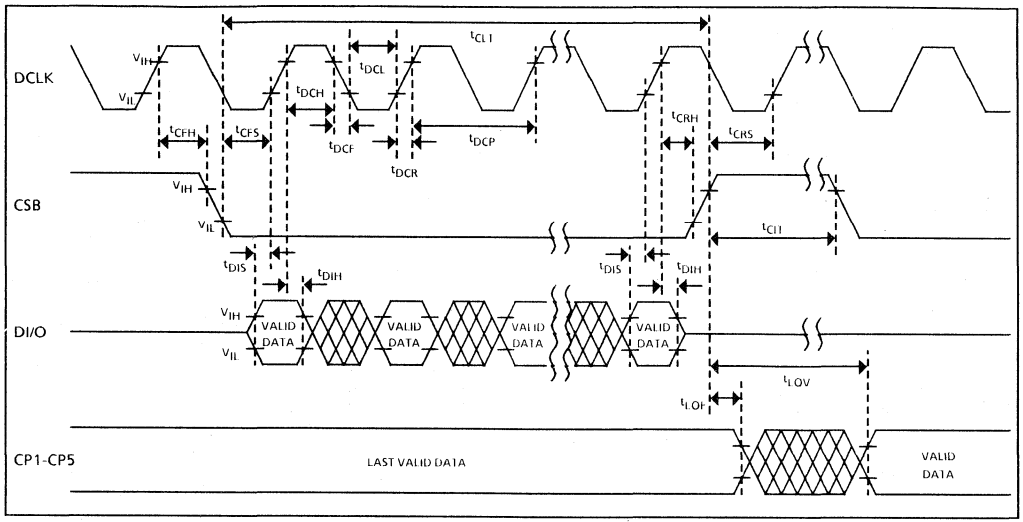


Figure 23 : Control Interface Input Data Timing Diagram.

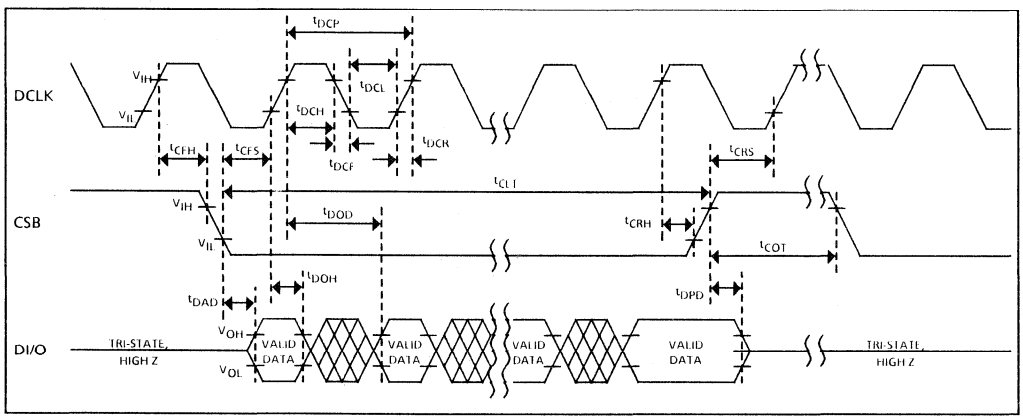


Figure 24 : Control Interface Output Data Timing Diagram.

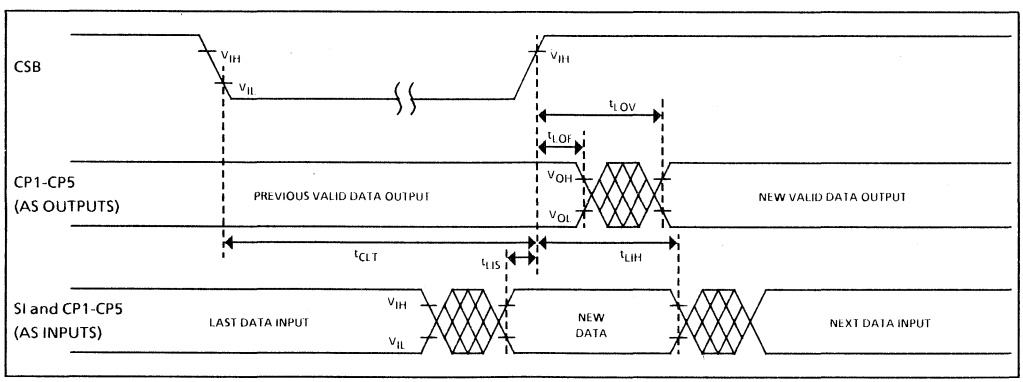


Figure 25 : I/O Latches and SI Pin Timing Diagram.

ABSOLUTE MAXIMUM RATINGS*

Voltages are with respect to analog ground (V_{AGND}).

Parameter	Symbol	Value		Units
		Min.	Max.	
Analog Supply Voltage, Note 1.	AV_{CC}	-0.5	+5.5	Volts
Digital Supply Voltage, Note 1.	DV_{CC}	-0.5	+5.5	Volts
Storage Temperature	T_S	-55	+125	°C
Input Voltage - except VIN pin	V_I	-0.5	DV_{CC} +0.3	Volts
Input Voltage - VIN pin, Note 2.	V_{VIN}	-4.8	DV_{CC} +0.3	Volts
Output Voltage - except VOUT pin	V_O	-0.5	DV_{CC} +0.3	Volts
Output Voltage - VOUT pin	V_{VOUT}	-0.5	AV_{CC} +0.3	Volts
Clamp Current (Sink or Source beyond Power Supply)	I_K		100	mA
Package Power Dissipation	P		800	mW

* Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Notes:- 1. This may be increased to +7.0 volts for a time not exceeding 100mS on an occasional basis.

2. For a time not exceeding 20mS at upto a unity mark-space ratio or for a time not exceeding 100mS at up to a 10% mark-space ratio. The pin should be DC biased close to V_{AGND}.

PCBAN111

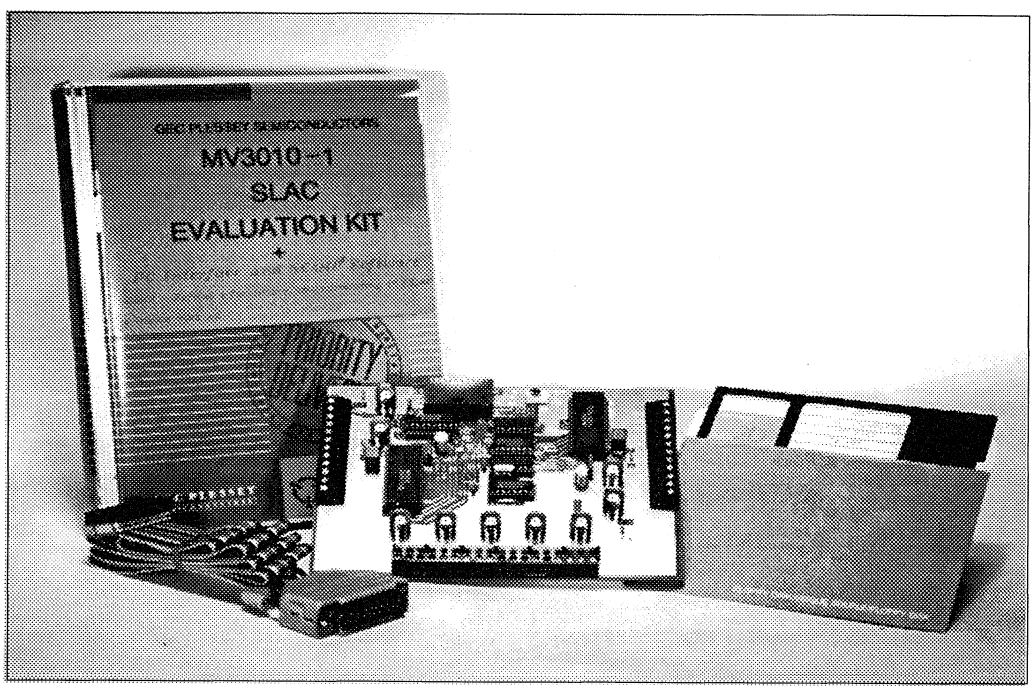
MV3010-1 SLAC EVALUATION PACKAGE

Now available from GPS is a complete evaluation package for the MV3010-1 Subscriber Line Audio Circuit (SLAC). The package includes both hardware and supporting software for use with IBM PCs or compatibles.

Hardware tor the evaluation package consists of a circuit board containing two SLAC devices with full and flexible access to all analog and digital ports. The software (SCAMP) of the evaluation package can be used to fully control/monitor all programmable features of both SLACs. These features are discussed fully in Applications Note AN111-2 which is available separately.

FEATURES

- Full and Flexible Access to all Analog and Digital Ports ot both SLACs of the Hardware.
- Hardware May Be Run as a Stand Alone Board or Interfaced to an IBM PC or Compatible.
- Full Software Control of the Evaluation Board via the SCAMP Software Running on the PC.
- Automated C Filter Preprogramming Software Routine Available within SCAMP.
- Automated Measurement and Display of Echo Return Loss Pertormance tor the Chosen Line Interface Circuit.
- Easy To Use Menu Driven Software.
- Single Screen tor each SLAC Status Readily Displayed by the SCAMP Software.
- Application Note AN111-2 fully describes the Operation and Uses of the Evaluation Package.



The PCBAN111 evaluation package.

Section 4

Other Telecoms Circuits

GEC PLESSEY
SEMICONDUCTORS

MV6001

HDLC/DMA CONTROLLER

The MV6001 is a combined HDLC transceiver and DMA controller capable of providing serial communications at rates up to 128K bits/second, and handling direct memory access clock rates up to 8MHz.

FEATURES

- Data Rates up to 128K Bits/s
- DMA Rate up to 8MHz
- Low Power CMOS
- Simple Interfacing to Popular 8-Bit Processors
- Frame Length up to 2K Bytes
- Low Host-Processor Overhead
- Conforms to ECMA40 and Related Standards (CCITT X25, X75, 1.440, ISO3309, ANSI X3.66, FED-STD 1003, FIPS71)

APPLICATIONS

- ISDN Terminals
- LANs
- X25 p.s.s. Networks

ORDERING INFORMATION

MV6001 B0 DP (Commercial Plastic DIP)
MV6001 B0 DG (Commercial Ceramic DIP)

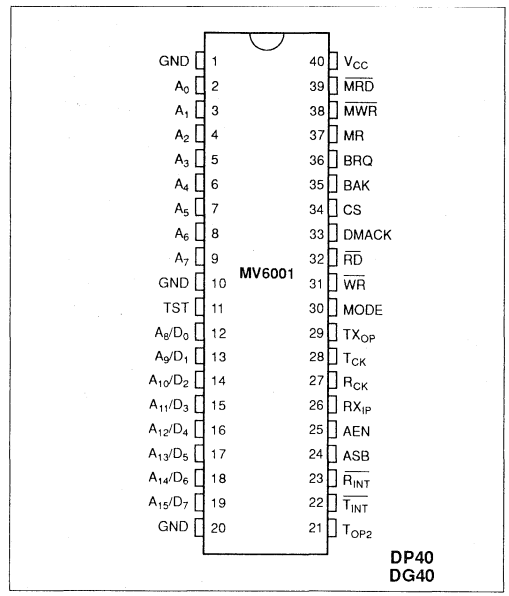


Figure 1: Pin connections - top view

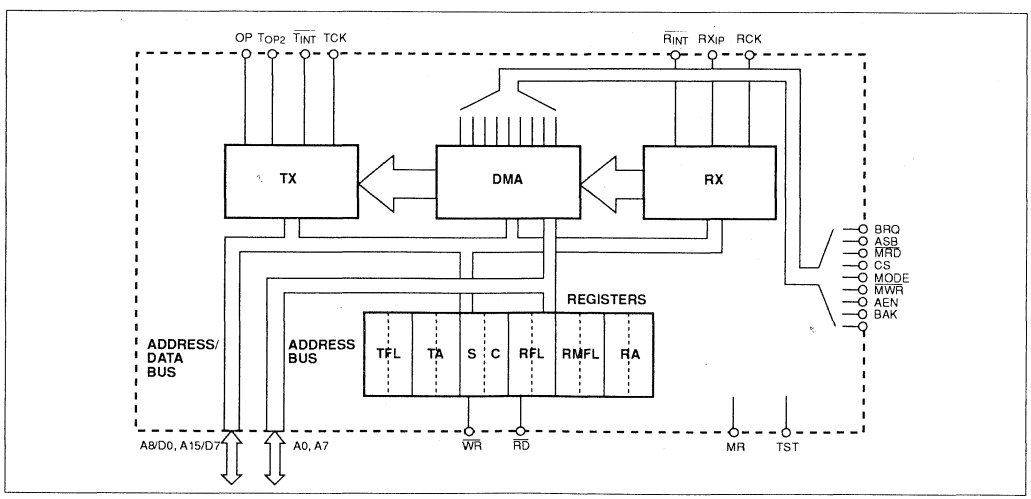


Figure 2: Block diagram

PIN DESCRIPTION

Pin No.	Name	I/O	Function
1,10,20	GND		**0V supply**. All 3 pins must be connected.
2 - 9	A_0 - A_7	I/O	**Address Bus**. Output for memory A_0 - A_7 addressing. Input for register addresses A_0- A_3.
11	TST	I	**Test Enable**. Tie to GND for normal operation.
12-19	A_8/D_0- A_{15}/D_7	I/O	**Data Bus/High Order Address**. Multiplexed data and address bus.
21	TOP2	O	**Transmitter Out**. Alternative output to TX_{OP}. This output is not affected by loop back (see Operating Notes - LOOPBACK).
22	$\overline{T}_{INT}$	O	**Transmitter Interrupt**. An interrupt is generated whenever transmission of a frame is ended, either following the last FCS byte of a complete frame of when an abort sequence is transmitted. The interrupt is reset by the control register.
23	$\overline{R}_{INT}$	O	**Receiver Interrupt**. An interrupt is generated whenever a frame is received. The interrupt is reset by the counter register.
24	ASB	O	**Address Strobe**. Strobes the Address High byte from the Data/Address Bus into an external latch.
25	AEN	O	**Address Enable**. Enables the external address latch.
26	RX_{IP}	I	**Receiver Input**. Serial HDLC data input, clocked in by RCK.
27	RCK	I	**Receiver Data Clock**. Provides clock to the receiver section, frequency should be at the required data rate, this need not necessarily the the same as the transmit data rate.
28	TCK	I	**Transmitter Data Clock**. This input provides a clock signal for the transmitter section and should be set to the desired transmit data rate.
29	TX_{OP}	O	**Transmitter output.** Main transmitter output for serial data.
30	MODE	I	**Bus Control Mode Select**. Controls the polarity of BAK and BRQ. MODE = V_{CC} gives active LOW, MODE = GND gives active HIGH.
31	$\overline{WR}$	I	**Write Register.** Loads data from data bus into register addressed by A_0- A_3.
32	$\overline{RD}$	I	**Read Register**. Reads addressed register onto data bus
33	DMACK	I	**DMA Clock.** This input provides clock to the DMA section. The DMA clock rate should be at least ten times the sum of the transmit and receive data rates.
34	CS	I	**Chip Select**. Enables $\overline{RD}$ and $\overline{WR}$ inputs.
35	BAK	I	**Bus Acknowledge**. Input from processor relinquishing control of bus. See pin 30, Bus Mode Select.
36	BRQ	O	**Bus Request**. Output to processor requesting the bus for a DMA cycle. See pin 30, Bus Mode Select.
37	MR	I	**Master Reset**. Resets everything.
38	$\overline{MWR}$	O	**Memory Write**. This is a three-state output to write data into memory during DMA cycles.
39	$\overline{MRD}$	O	**Memory Read**. 3-state output to read data from memory during DMA cycles.
40	V_{CC}		±5V ±10% supply.

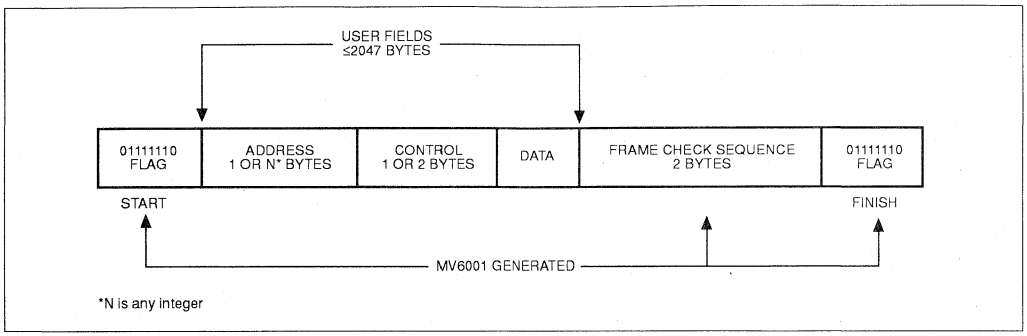


Figure 3

Fig.3 shows the construction of an HDLC frame. The start and finish of the frame are determined by FLAGS (the binary pattern 01111110). To prevent spurious recognition of flags in the user fields, the transmitter automatically inserts a '0' after five successive '1 's. The inserted '0's are removed by the receiver, and hence are not seen by the user. Each HDLC frame contains a 2 byte frame check sequence produced by a cyclic redundancy generator in the transmitter. This sequence is checked by the receiver to validate the frame.

There are two other sequences which have specific meanings - IDLE and ABORT. The IDLE state is the transmission of at least 15 continuous '1's without inserted zeros. ABORT is 7 to 14 consecutive '1's without inserted zeros sandwiched between two zeros.

FUNCTIONAL DESCRIPTION

The MV6001 consists of four main sections; transmitter, receiver, DMA unit and register bank. Each of the transminer~ receiver and DMA unit have their own clocks running at the required data rates. There are no restrictions on the relative timing between transmit and receive clocks, the DMA clock rate should be greater than ten times the sum of the transmit and receive clock rates.

TRANSMISSION

In its steady state the transmitter produces a continuous stream of FLAGS until the control register is loaded with a transmit instruction. The transmitter then, at intervals, requests the DMA unit to fetch a byte of data. This is then transferred from the system memory via the data bus to the transmitter. (If the DMA unit should fail to fetch a byte of data by the time the next request arrives then an under-run will occur and the transmitter will transmit an ABORT sequence). Data is converted into a serial stream with inserted zeros after five ones, and the 16-bit frame check sequence is appended at the end of each frame. As soon as the last bit of the FCS has been clocked out, the TINT OUtPUt goes low to inform the processor that transmission has ended.

INITIALISATION

To start transmission, two items of information are required - the start address for the data to be transmitted, and the length of the user fields are loaded into the TA and TFL registers respectively, after which the transmit enable bit (D0) can be set at any time to start transmission. Once a transmission has been started, the only way it can by stopped is to set the abort bit (D1). The transmitter will then transmit the abort sequence followed by flags. Transmitter reset (D2) resets the transmitter interrupt TINT, clears the TA and TFL registers and bits D0 and D1 of the status register. Transmitter reset is disabled during a transmission.

INTERRUPT

A transmitter interrupt ($\overline{TINT}$) is generated whenever a transmission ceases, the status register can then be read to check if the frame was aborted or not. The interrupt is reset by writing a transmitter reset to the control register. NB. The status register must be read before a transmitter reset as this will alter the contents of the status register.

STATUS

The transmitter has two status bits - transmitting data (Do) and abort (D1) The transmitting data bit should always be low after $\overline{T}_{INT}$ signifying that transmission is ended. The abort bit will be high whenever a frame is aborted either by an abort instruction to the control register, or internally due to an under-run .

RECEPTION

The receiver accepts serlal data, removes inserted zeros and checks the frame check sequence. For each byte of data received, the receiver section generates a DMA request to transfer the data to memory. If the DMA controller fails to make the transfer before the next request from the receiver, then the receiver will drop out and give a receiver. interrupt with the code in the status register for overrun. If the number of bytes received reaches the number in the receive maximum frame length registerthe receiverwilldropoutand give an interrupt with the code in the status register for frame too long.

INITIALISATION

The RA register (2 bytes) is loaded with the address where the first received byte of data is to be stored. The RMFL register (11 bits) is loaded with the maximum number of bytes in the user fields plus 3 bytes (+2 bytes for the FCS, +1 byte because an interrupt will occur when the frame length is equal to the length set by the number in the register) .

CONTROL

The receiver has two control bits in the control register, receive enable (D3) and receive reset (D4). Once the RA and RMFL registers have been loaded, the receive enable bit can be set at any time to allow the receiver to receive a frame. Once set, the receive enable bit cannot be overwritten and receive reset is disabled until a frame has been received.

Receiver reset will reset the $\overline{RINT}$ interrupt bit, registers RFL, RMFL, RA and bits D2 - D7 of the status register.

INTERRUPT

A receive interrupt ($\overline{R_{INT}}$) is generated whenever a frame is received. The status register can then be read to check the status of the received frame. The interrupt is reset by writing a receiver reset to the control register. Since the reset will clear the receiver bits in the status register, the register must be read before writing the reset to the control register.

STATUS

The receiver uses bits D2 - D7 of the status register (see Figs. 5 and 6). A valid frame is indicated by both 'overrun' (D6) and 'frame too long' (D7) bits being high. Following $\overline{R_{INT}}$ the 'free to receive' bit (D2) should be low, indicating that a frame has been received. The abort, overrun and long frame bits will be set according to the state of the frame received. The flag (D4) and idle (D3) bits monitor the incoming signal continuously even when the receiver is disabled.

FRAME LENGTH REGISTER

Having received a frame and read the status reqister, the received frame length can be read from the RFL register. The frame length is given as an eleven bit number and includes the 2 FCS bytes in the count. The reqister should be read before a receiver reset.

LOOPBACK

Bit D7 of the control register, the loopback bit is provided for testing purposes. When the bit is set high an internal connection is made between the transmitter output and receiver input. The main transmitter output (TX_{OP}) transmits IDLE (transmitted data is always available on T_{OP2}). The receiver is clocked from TCK. The loopback bit will respond to every write to the control register.

DIRECT MEMORY ACCESS (FIG.11)

All data transfers to or from memory are carried out by the DMA controller. Each time it receives a request from the transmitter or receiver it will carry out one DMA cycle, i.e. only one byte is transferred at a time. Clashes between transmitter and receiver are resolved in favour of the receiver, otherwise operation is on a first come, first served basis.

REGISTERS

Fig.7 shows the addresses for the various instruction and status registers. All registers are readable from and writable to except for S, C and RFL. The S and C registers have the same address, which one is accessed is determined by whether a read (status) or write (control) operation is carried out. Transmitter registers should not be written to when transmitting (except to ABORT a frame), likewise receiver registers should not be written to when receiving. The TA and RA registers update continuously during transmission and reception respectively, giving the next address to be read from or written to.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
LOOPBACK ENABLE	DON'T CARE	DON'T CARE	RECEIVE RESET	RECEIVE ENABLE	TRANSMIT RESET	TRANSMIT ABORT	TRANSMIT ENABLE

Figure 4: Control register

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
RECEIVED FRAME TOO LONG	RECEIVED OVERRUN FRAME	RECEIVED ABORT	RECEIVING FLAGS	RECEIVING IDLE	FREE TO RECEIVE	TRANS-MISSION ABORTED	TRANS-MITTING DATA

RECEIVE BITS — TRANSMIT BITS

Figure 5: Status register

Status Register								
D7	D6	D5	D4	D3	D2	D1	D0	Condition
X	X	X	X	X	X	0	1	Currently transmitting data
X	X	X	X	X	X	0	0	Transmitter disabled, transmission COMPLETE (status read after an interrupt)
X	X	X	X	X	X	1	0	Transmitter disabled, transmission ABORTED (status read after an interrupt)
X	X	X	X	X	1	X	X	Receiver enabled, free to receive
X	X	X	0	0	X	X	X	Currently receiving data
X	X	X	0	1	X	X	X	Receiving IDLE
X	X	X	1	0	X	X	X	Receiving FLAGS
0	0	1	X	X	0	X	X	Receiver disabled, ABORTED frame received (status read after an interrupt)
0	1	0	X	X	0	X	X	Receiver disabled, OVERRUN frame received (status read after an interrupt)
1	0	0	X	X	0	X	X	Receiver disabled, TOO LONG frame received (status read after an interrupt)
1	1	0	X	X	0	X	X	Receiver disabled, VALID frame received (status read after an interrupt)

Figure 6: Status interrupt

Regisler	Function	Length (Bits)	Address (Hex)	A3	A2	A1	A0	R/W
TFL	Transmitter Frame Length LS Byte	8	2	0	0	1	0	R/W
	Transmitter Frame Length MS Byte	3	3	0	0	1	1	R/W
TA	Transmitter Address LS Byte	8	6	0	1	1	0	R/W
	Transmitter Address MS Byte	8	7	0	1	1	1	R/W
S	Status	8	9	1	0	0	1	R
C	Control	8	9	1	0	0	1	W
RFL	Receiver Frame Length LS Byte	8	A	1	0	1	0	R
	Receiver Frame Length MS Byte	3	B	1	0	1	1	R
RMFL	Receiver Maximum Frame Length LS Byte	8	C	1	1	0	0	R/W
	Receiver Maximum Frame Length MS Byte	3	D	1	1	0	1	R/W
RA	Receiver Address LS Byte	8	E	1	1	1	0	R/W
	Receiver Address MS Byte	8	F	1	1	1	1	R/W

Figure 7: Register addresses

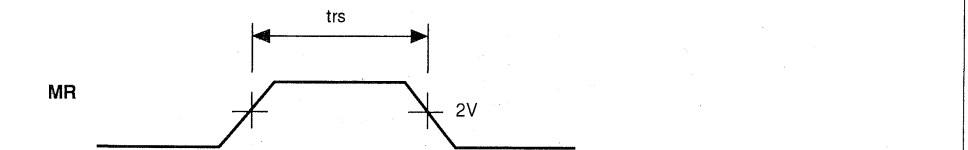


Figure 8(a)

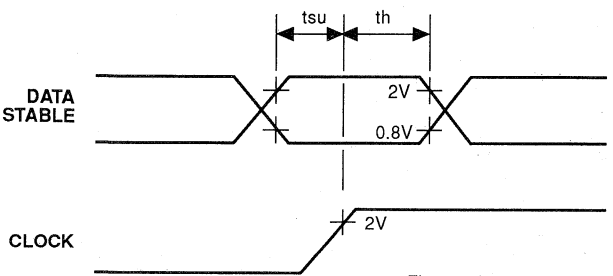


Figure 8(b)

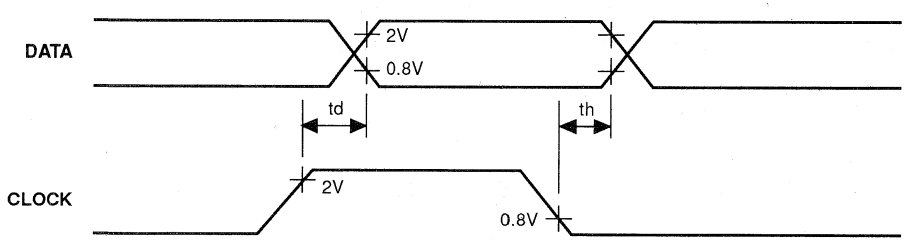


Figure 8(c)

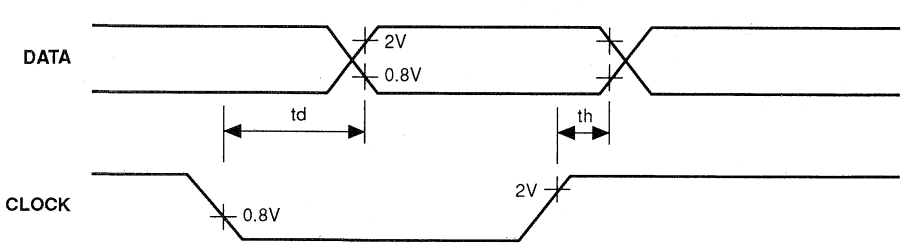


Figure 8(d)

Figure 8: Timing diagram

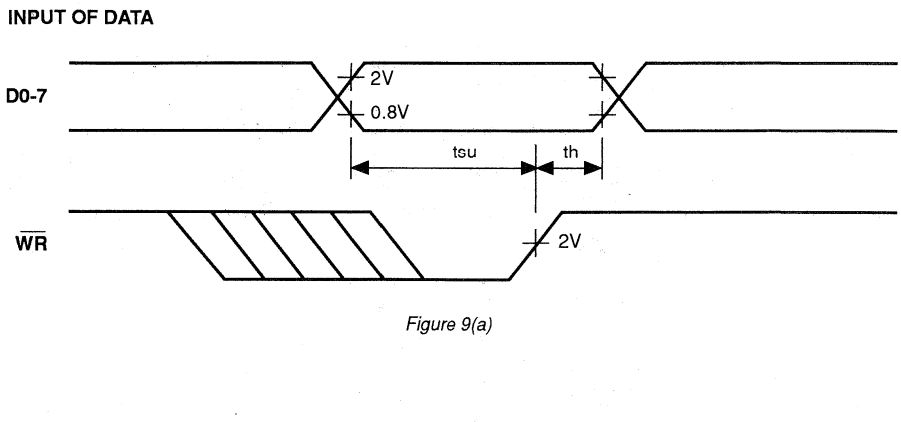


Figure 9(a)

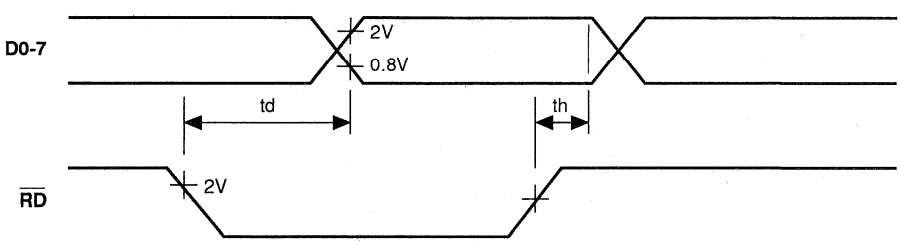


Figure 9(b)

Figure 9: Register timing

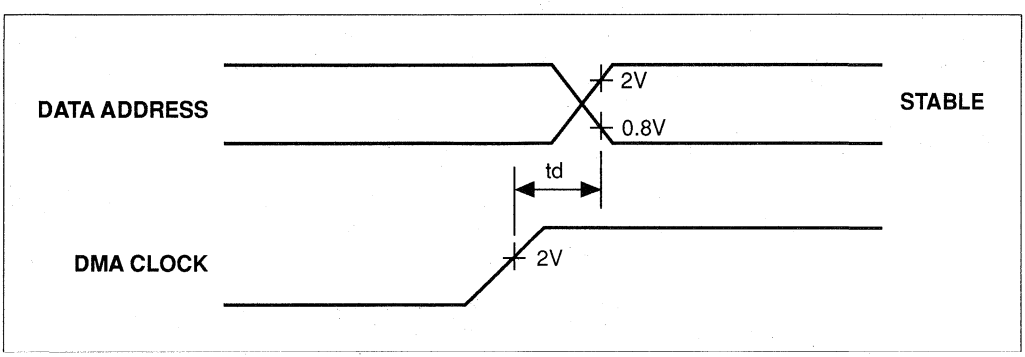


Figure 10: DMA timing

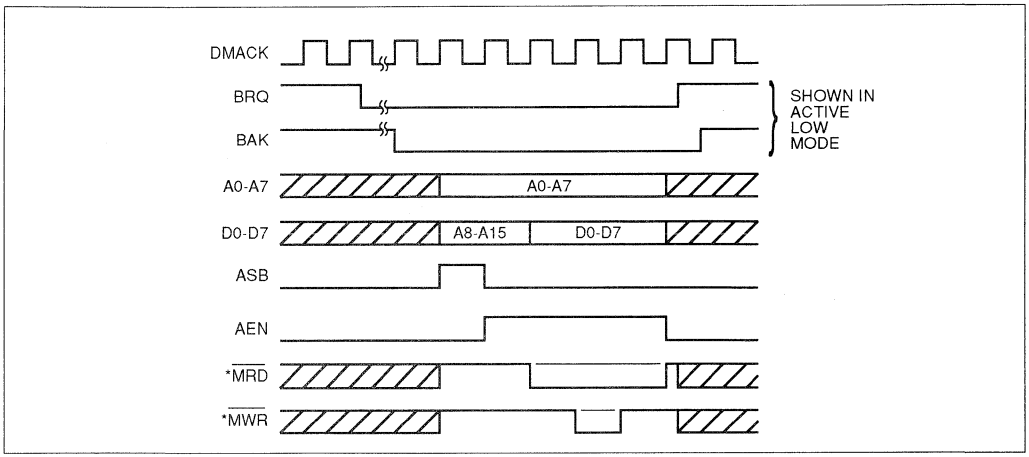


Figure 11: DMA cycle timing

*During a read cycle, $\overline{MWR}$ stays high and similarly during a write cycle $\overline{MRD}$ stays high. All other external signals are the same for both cycles.

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	-0.3V to 7.0V
Input voltage V_{IN}	-0.3V to V_{CC} +0.3V
Output voltage V_{OUT}	-0.3V to V_{CC} +0.3V
Clamp diode current per pin IK (See Note 2)	±18mA
Static discharge voltage	
Storage temperature Ts	-65°C to +150°C
Ambient temperature with power applied T_{amb}	-40°C to +85°C

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied
2. Maximum dissipation of 1 second should not be exceeded, only one output to be tested at any one time

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless othetwise stated):

T_{amb} = -40°C to +85°C, V_{CC} = 5.0V ±10%, Ground = 0V

STATIC CHARACTERISTICS

Characteristic	Symbol	Value Min.	Value Typ	Value Max.	Units	Conditions
Output high voltage	V_{OH}	V_{CC}-2			V	IOH = 0.8mA
Output low voltage	V_{OL}			0.4	V	I OL = 1 .6mA
Input high voltage	V_{IH}	2.2			V	
Input low voltage	V_{IL}			0.8	V	
Input leakage current	I_L	-10		+10	µA	GND ≤ V_{IN} ≤ V_{CC}
V_{CC} current	I CC			1	mA	T_{amb} = -40°C to +85 °C
Output leakage current	I_{OZ}	-50		+50	µA	GND ≤ V_{OUT} ≤ V_{CC}
Output S/C current	I_{OS}	15		80	mA	V_{CC} = Max

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Maximum DMA clock frequency	FDMACK	8			MHz	
Maximum TX clock frequency	FTCK	128			kHz	
Maximum RX clock frequency	FRCK	128			kHz	
Minimum MR duration	t_{rs}				ns	Fig.8(a)
RXIP to RCK set-up time	t_{su}	0			ns	Fig.8(b)
RXIP to RCK hold time	t_h	90			ns	Fig.8(b)
BAK to DMACK set-up time	t_{su}	0			ns	Fig.8(b)
BAK to DMACK hold time	t_h	25			ns	Fig.8(b)
Delay DMA clock to $\overline{MRD}$	t_d		40	55	ns	Fig.8(c)
Delay DMA clock to $\overline{MWR}$	t_d		40	55	ns	Fig.8(c)
Delay RCK ⇓ to $\overline{RINT}$	t_d		50	110	ns	Fig.8(d)
Delay, TCK to $\overline{TINT}$	t_d		60	90	ns	Fig.8(c)
Delay, TCK ⇑ or RCK ⇓ to BRQ	t_d		70	90	ns	Fig.8(c) & (d)
Delay, DMACK to AEN	t_d		40	55	ns	Fig.8(c)
Delay, DMACK to ASB	t_d		40	55	ns	Fig.8(c)
Delay, TCK to TXoP	t_d		70	115	ns	Fig.8(c)
Delay, TCK to ToP2	t_d		60	115	ns	Fig.8(c)
Hold, DMACK to $\overline{MRD}$	t_h		90	130	ns	Fig.8(d)
Hold, DMACK to $\overline{MWR}$	t_h		50	75	ns	Fig.8(d)
Hold, DMACK to BRQ	t_h		60		ns	Fig.8(d)
Hold, DMACK to AEN	t_h		30	55	ns	Fig.8(d)
Hold, DMACK to ASB	t_h		40	55	ns	Fig.8(d)
Data to WR set-up	t_{su}				ns	Fig.9(a)
WR to data hold	t_h				ns	Fig.9(a)
RD to data delay	t_d		50		ns	Fig.9(b)
RD to data hold	t_h				ns	Fig.9(b)
DMACK to data/address delay	t_d		60		ns	Fig.10

SP1404BW

HIGH VOLTAGE INTERFACE CIRCUIT

The SP1404 is a bipolar integrated circuit comprising five individual digital current amplifier circuits. Each circuit accepts a logic input from TTL, CMOS or a similar source and drives a high-current load at the output. The outputs are capable of withstanding high negative voltages in the 'off' state, making the SP1404 particularly suited to telecommunications applications.

CIRCUIT DESCRIPTION (Fig.2)

The SP1404 operates as a power amplifier interfacing from a voltage-level sensitive input to a high-current output switch. The input threshold is TTL-compatible, with a low input current requirement enabling one standard TTL output to drive many interfaces. The low input current requirement also makes it possible to use series current-limiting resistors to protect the SP1404 inputs.

Each element of the device performs as inverting function, i.e. a low voltage level on the input causes a high current in the output. If the input is left open-circuit, the output will be off and the output current will be zero.

The isolation of the integrated circuit is biased to the more negative of the two earth points by diodes D1 and D2 so that differences of up to (V_{CC} - 1) volts can be tolerated between the 'noisy' exchange earth and the 'quiet' electronic earth.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-55°C to +175°C
Chip operating temperature	+150°C
Ambient temperature (I_{OUT} = 50mA)	+85 °C
Load current	80mA
Voltage between output and 'noisy earth'	-65V
V_{CC} to output voltage	75V
V_{CC} to electronic earth	7V
Input voltage	V_{CC} + 1V

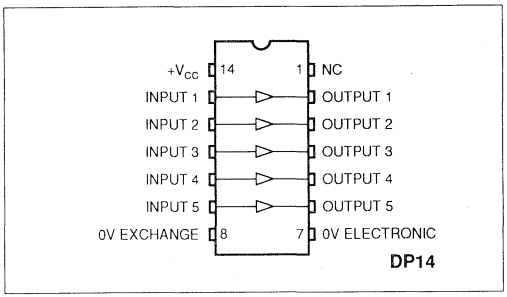


Figure 1: Pin connections (viewed from underside)

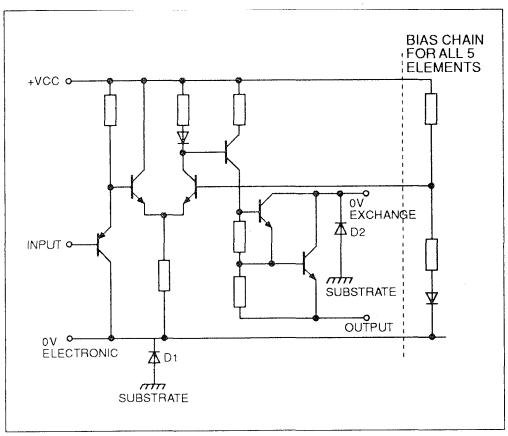


Figure 2: Circuit diagram of one element

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Temperature range = 0°C to +70°C, V_{CC} = +5V ± 0.5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input current		-20		µA	V_{IN} = 0V
				µA	V_{IN} = V_{CC}
Output voltage			1.5	V	V_{IN} = 0.8V, I_{OUT} = 50mA
Output current (Off state)			100	µA	V_{IN} = 2V, V_{OUT} = -60V
Output current (On state)	50	80		mA	V_{IN} = 0.8V
V_{CC} supply current		30		mA	V_{CC} = 5V, all inputs low
Total power dissipation		450		mW	V_{CC} = 5V, all inputs low all outputs I_{OUT} = 50mA

Section 5
Application Notes

GEC PLESSEY
SEMICONDUCTORS

MV1403

PCM MACROCELL EVALUATION BOARD

This application note describes the PCBAN93 evaluation board for the MV1403 PCM Macrocell demonstrator chip. The board has been designed to allow evaluation of the individual macrocells and to demonstrate how the MV1403, along with external circuitry, may be used to implement a 2.048Mbit PCM link in accordance with CCITT Recommendations G.703, G.704 and G.732.

THE 2.048MBIT PCM LINK

This is a digital trunk capable of carrying 30 speech channels plus associated signalling, synchronisation and error checking. The serial structure of the 2.048Mbit PCM link is shown in Fig. 1. There are 8 bits in each timeslot, 32 timeslots in each frame and 16 frames in each multiframe.

The bits of a timeslot are numbered from 1 to 8, whilst the timeslots per frame and frames per multiframe are numbered from 0 to 31 and 0 to 15 respectively. The serial data stream is HDB3 encoded (CCITT Recommendation G.703), ensuring adequate clock recovery at the receiver.

Frame synchronisation is achieved by the receiver searching for and locking on to the Frame Alignment Signal (FAS) 0011011 present in bits 2 to 8 of timeslot zero during even numbered frames. Such frames are designated sync frames since they contain the FAS. Odd frames are designated non-sync frames. During timeslot zero of non-sync frames bit 2 is set to '1' to ensure discrimination between sync and non-sync frames, bit 3 is used as a remote alarm bit and bits 4-8 are spare bits which may be used nationally.

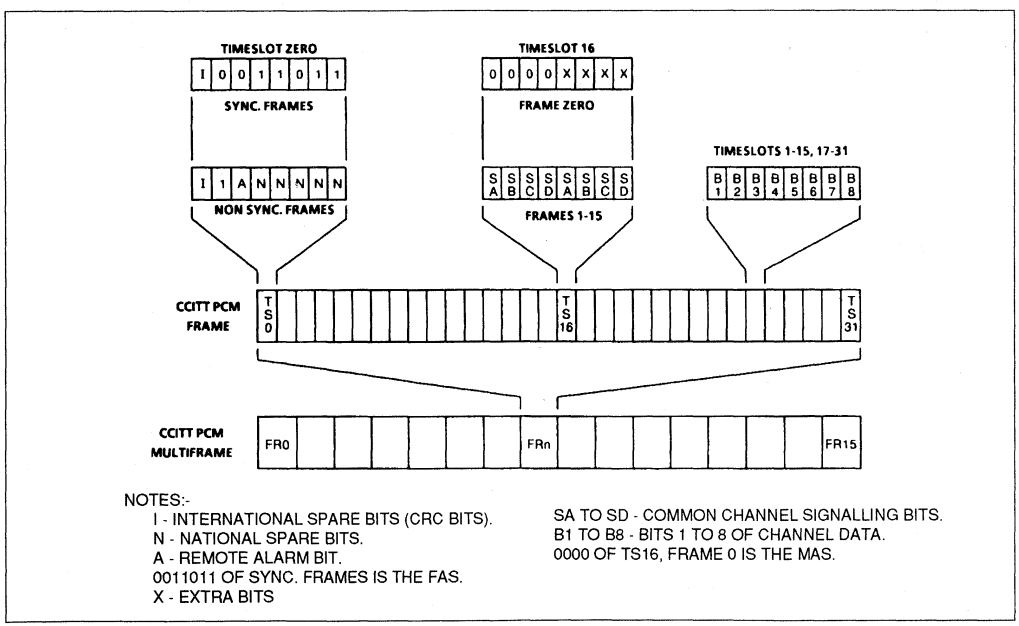


Figure 1: Serial structure of the 2.048Mbit PCM link

Signalling data for the 30 voice channels is transmitted using common channel signalling in Timeslot 16. Multiframe alignment, if required, is achieved by the presence of four 0's, the Multiframe Alignment Signal (MAS), in bits 1 to 4 of timeslot 16 during frame 0. The remaining timeslot 16 in frames 1 to 15 may then be used for signalling by the 30 voice channels.

CCITT Recommendation G.704 describes a possible use for the International spare bits found in the bit 1 position of timeslot 0. Where there is a need to provide additional protection against simulation of the FAS or where there is a need for enhanced error monitoring, then the International spare bit may be used for a Cyclic Redundancy Check procedure. The CRC multiframe consists of two submultiframes, designated SMF I and SMF II, each containing 2048 bits, this being the CRC block size. The 16 frame CRC multiframe structure is not related to the possible use of a multiframe structure implemented within timeslot 16.

During sync frames, bit 1 of timeslot zero contains CRC bits obtained from the previous SMF. There are 4 CRC bits in each SMF, designated C1 to C4. During non-sync frames, bit 1 contains the 6-bit CRC Multiframe Alignment Signal (001011) in frames 1, 3, 5, 7, 9 and 11 and 2 CRC error bits (E-bits) in frames 13 and 15, used to indicate the reception of errored submultiframes.

THE MV1403

The MV1403 contains 8 PCM macrocells plus additional circuitry such as the transmission multiplexer and mode selectors to enable it to function as the basis of a 2.048Mbit PCM link or to allow operation of the individual macrocells to be proven. The 8 PCM macrocells are:

- Timeslot Zero Transmitter - TXTSZ
- Timeslot 16 Transmitter - TXTS16
- CRC Generator - CRCGEN
- HDB3 Encoder - HDB3EC
- HDB3 Decoder - HDB3DC
- Timeslot Zero Receiver - RXTSZ
- Timeslot 16 Receiver - RXTS16
- CRC Checker - CRCCHK

Detailed information about the MV1403 demonstrator chip and the individual macrocells can be found in the relevant data sheets although a brief description of the macrocells is included below.

TIMESLOT ZERO TRANSMITTER

The Timeslot Zero Transmitter macrocell generates the Frame Alignment Signal in accordance with CCITT Recommendation G.704. This is multiplexed together with the other data to be transmitted during timeslot zero and injected on to the PCM highway at the relevant time. In order to do this it requires two timing inputs, a 2.048MHz clock and an active high 8 bit long pulse masking timeslot zero, to enable frame alignment. The latter of these is known as the Frame Sync input, FRS. The data to be transmitted during bits 3 to 8 of non-sync frames is loaded via parallel data inputs, and there is a further input for data to be transmitted during bit 1. The Timeslot Zero Transmitter also produces a timing waveform as output, TZS (Timeslot Zero Sync frame), which is used by other macrocells to determine whether sync frame or non-sync frame data is about to be transmitted.

TIMESLOT 16 TRANSMITTER

The Timeslot 16 Transmitter receives continuous signalling data at 64kbits and converts this into 8-bit packets of data which it transmits at 2.048Mbits during timeslot 16 of successive frames. It again requires a 2.048MHz clock and Frame Sync inputs, and from these it derives its TS16 timing output, which is similar to FRS but masks Timeslot 16.

CRC GENERATOR

The CRC Generator macrocell has two basic modes of operation: CRC mode and non-CRC mode. It has two main external inputs D1S and D1N, which access the data to be transmitted during bit 1 of timeslot zero for sync and non-sync frames respectively. When in non-CRC mode the D1S/D1N data is available at the Q output depending upon whether a sync frame or non-sync frame is about to be transmitted, as specified by the TZS input.

When in CRC mode the CRC generator macrocell has two major functions. One part of the macrocell samples the data being output by the transmission multiplexer during successive submultiframes and from this it derives the CRC word to be output as bit 1 data to the Timeslot Zero Transmitter during the next submultiframe. The second part of the macrocell saves the previously obtained CRC word and outputs this along with the CRC Multiframe Alignment Signal and D1S/D1N data (for the E-bits of frames 13 and 15 respectively) in accordance with CCITT Recommendation G. 704. This is used as an input to the Timeslot Zero Transmitter. It again relies upon the timing input TZS to do this.

HDB3 ENCODER

The HDB3 Encoder macrocell converts the NRZ data being output from the transmission multiplexer into HDB3 pseudo-ternary format in accordance with CCITT Recommendation G.703 Annex A.

HDB3 DECODER

The HDB3 Decoder macrocell decodes the pseudo-ternary HDB3 inputs to NRZ form. It provides a logical 'OR' of the two inputs as an output to be used by a clock regenerator if required. It also provides two alarm outputs, one for Loss of Input (LIA) and another for a Double Violation on the incoming signal (DV).

TIMESLOT ZERO RECEIVER

The main function of the Timeslot Zero Receiver is to search for and lock on to the Frame Alignment Signal present in the incoming data. The synchronisation/loss of synchronisation process is conducted in accordance with the synchronisation strategy described in CCITT Recommendation G.732. The macrocell produces two timing outputs to the other macrocells, TSZ and TZS. The TSZ (Timeslot Zero) output is similar to the Frame Sync input of the transmitter. The TZS (Timeslot Zero Sync-frame) output is used to determine whether a sync or non-sync frame is about to be received.

The national spare bits from timeslot zero non-sync frames are available as parallel data outputs. The bit 1 data from timeslot zero is also available as outputs Q1S and Q1N. These are obtained according to the CRC mode input, and two timing inputs, FRS13 and FRS15, to enable the two E-bits of a CRC multiframe to be extracted.

In addition, the Timeslot Zero Receiver provides three alarm outputs. The first, ER, denotes that a single erroneous FAS has been received. The second, Sync Alarm. (SA), denotes that the receiver is out of synchronisation and the last is the Remote Alarm Indication (RAI), indicating that a remote alarm has been received from the transmitter.

TIMESLOT 16 RECEIVER

The Timeslot 16 Receiver macrocell synchronises to the 2.048Mbit PCM data stream and extracts signalling data during Timeslot 16. This data is stored and then output as a continuous stream at 64kbits.

CRC CHECKER

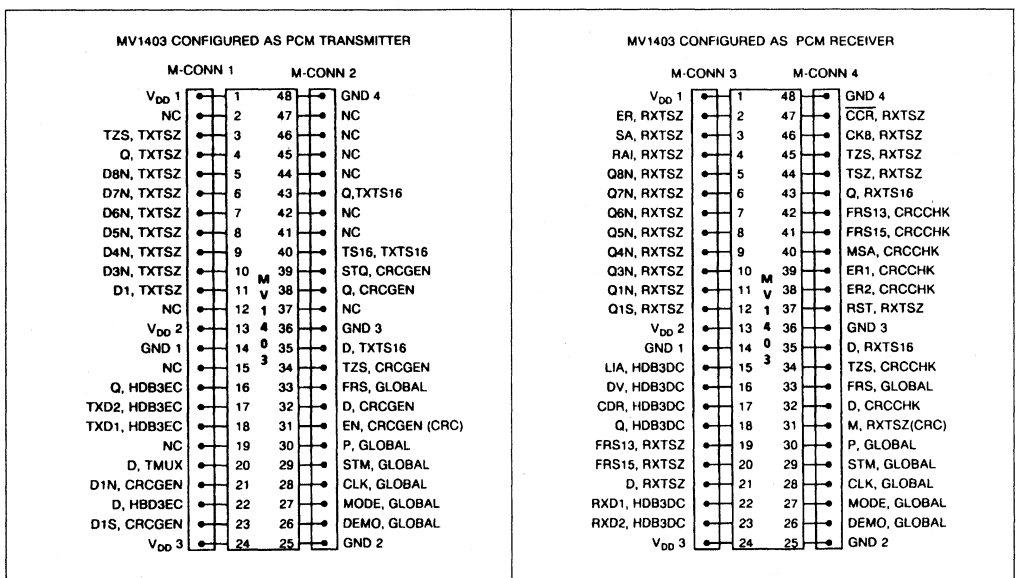
The CRC Checker macrocell has two major functions. One part searches for and locks on to the CRC Multiframe Alignment Signal present in the bit 1, timeslot zero position of non-sync frames. When in sync, the CRC bits are then extracted from bit 1 of sync frames. The second part generates a new CRC word in accordance with CCITT Recommendation G.704 from the incoming data stream and compares this with the CRC bits received in the next submultiframe. The CRC Checker provides three alarm and two timing outputs. The two timing outputs, FRS13 and FRS15, are high during bit 1, timeslot zero of frames 13 and 15 respectively. The Timeslot Zero Receiver uses this information to extract the E-bits of a CRC multiframe.

The three alarm outputs are ER1, ER2 and MSA. The ER1 and ER2 alarms are used to denote that a CRC error has occurred in submultiframe 1 or 2 respectively. The Multiframe Sync Alarm (MSA) indicates that the CRC Checker is out of multiframe alignment.

THE EVALUATION BOARD

MV1403 MODES OF OPERATION

Operation of the MV1403 is controlled by 4 device control inputs: STM, MODE, DEMO and CRC. The STM input is used to put the device in Scan Test Mode and should be tied to ground for normal operation. MODE is used to select whether the device is to be used as either a transmitter or receiver. The MV1403 contains all the macrocells to perform both transmitter and receiver operations but the pin count of the package restricts this to either one function or the other. When MODE is high the device acts as a receiver. The DEMO input selects whether the device is to be used as a system with all the macrocells connected together internally or whether the macrocells are to be accessed individually. When DEMO is high, the device functions as a system. The final control input is CRC. This selects whether or not the device is to be used in CRC generator/checker mode. When CRC is high then CRC generation/checking is enabled.



NOTES: NC - No valid connection in this mode of operation. These pins should be left unconnected.
D, TMUX - This is the speech data input to the transmission multiplexer, which is only used when DEMO is high.

Figure 2: Macrocell Connector Pinouts

EVALUATION BOARD OVERVIEW

Due to the package limitations previously discussed, the evaluation board contains two MV1403 devices to provide a useful demonstration, one configured as a transmitter, the other as a receiver. As such the board will demonstrate a 2.048Mbit PCM link in a single direction, although two boards may be connected together to form a bidirectional link. In addition to this, the two control inputs DEMO and CRC are externally selectable by DIL switches.

The other device of importance to be found on the board is an XR-T5683 line interface circuit. This device has three major functions: in the transmit direction it converts the TTL level pseudo-ternary data being output from the PCM transmitter into true ternary data to be output down a transmission line. In the receive direction it converts the ternary data from the transmission line back into TTL level pseudo-ternary data to be input to the PCM receiver and lastly performs clock recovery from the incoming data. These processes are performed in accordance with CCITT Recommendation G.703.

Although both transmit and receive directions are present in the XR-T5683, the two functions are completely segregated internally with separate power supplies for the two directions. The board is thus split into two halves, one being the PCM transmitter, the other the PCM receiver. The only common parts are the XR-T5683 interface circuit and the power supply. The board only requires a single + 5 Volt supply and will draw approximately 600mA.

To enable access to the individual macrocells, a pair of 0.1 inch pitch 24 way PCB headers are connected to each of the two MV1403s (M-CONN 1-4). The pin layouts of these connectors are shown in Fig. 2 but are only valid when the DEMO mode input is low. When DEMO is high, some of the input pins will no longer have any function since they will be connected internally to the outputs of other macrocells.

The remainder of the evaluation board consists of additional circuitry such as a clock generator to enable the board to function as a useful demonstrator, with as much flexibility as possible. The HDB3 inputs/outputs are accessed via BNC connectors for 75 Ohm unbalanced operation whilst other connections such as an external clock are made via 0.1 inch pitch PCB headers. The position of all connectors, switches and other major components is shown in Fig. 7.

TRANSMITTER CIRCUIT

A full circuit diagram of the transmitter half of the evaluation board, excluding macrocell connectors, is given in Fig. 3. The operation of the transmitter is selectable via two DIL switches (half of SW1-4) to set DEMO (labelled DEMO MODE) and CRC (CRC EN). A further 8 DIL switches (SW5-12) are used to set the user data inputs D1S, D1N and D3N to D8N which are to be inserted into the spare bits of timeslot zero. No external pull-up resistors are required on these pins since all input pins of the MV1403 have internal 100kOhm pull-up resistors.

To enable flexible operation, the transmitter circuit has an on board 2.048MHz clock generator centred around the 74LS321 crystal controlled oscillator circuit. Alternatively, an external 2.048MHz clock may be used, the internal/external clock option being selected by a further DIL switch (INT CLK) driving tristate buffers. Both the external clock input and the clock output along with other connections are accessed via the 0.1 inch pitch PCB connector, TX-CONN.

As well as being used as an input to the PCM transmitter and line interface circuit, the clock is also input to an 8-bit counter, the 74LS590. This counter and associated decoder circuitry are used to derive the FRS signal, an 8-period high-going periodic pulse used to mask timeslot zero. An external FRS input is also available, the option being selected by a final DIL switch (INT FRS).

A final timing output, high during bit 1 of timeslot zero, is also decoded from the counter. This may be used to synchronise codecs requiring a single period pulse at the start of timeslot zero. This output is only valid when the on-board FRS is selected.

The two serial data inputs, one for the 2.048Mbit speech data, the other for the 64Kbit signalling data, may also be accessed by the same connector, as well as by the macrocell connector. An inverter is required between the clock signal driving the MV1403 and that driving the transmitter half of the XR-T5683 (the line interface circuit). This clock inversion is necessary since the XR-T5683 requires that its inputs be active during the high half cycle of clock, whereas the pseudo-ternary outputs of the MV1403 are active during the low half cycle of clock.

LINE INTERFACE CIRCUIT

A full circuit diagram of the line interface portion of the evaluation board is included in Fig. 4. This circuit is built around the XR-T5683 line interface circuit. As mentioned previously, this device consists of separate transmit and receive sections.

The transmitter half of this device accepts the incoming pulses, shapes them in accordance with the pulse mask specified in CCITT Recommendation G. 703 and couples them through the transmit transformer, T1, to generate the differential HDB3 line signal. Depending upon the position of wire link 1 the differential voltage produced by the transformer is used to drive either an unbalanced 75 Ohm, co-axial output or a balanced 120 Ohm twisted-pair output (P-CONN1). Different feed resistor values (39 Ohm for 2.37V into 75 Ohm 30 Ohm for 3.0V into 120 Ohm) are also required to produce the correct peak pulse voltage as specified in CCITT Recommendation G.703. The winding instructions of both the transmit and receive transformers are given at the end of this application note.

On the receive side, either the 75 Ohm unbalanced input or the 120 Ohm balanced input (P-CONN2) is connected across the primary of the receive transformer, depending upon the position of wire link 2. The voltage thus produced on the centre tapped secondary of the receive transformer is fed into the XR-T5683. This converts the received ternary HDB3 pulses back into pseudo-ternary TTL level data to be output to the PCM receiver circuitry. The remainder of the circuitry is associated with the clock recovery circuit of the XR-T5683. This consists of the tuned circuit connected between pins 4 and 6 of the XR-T5683 and decoupling between pin 6 and ground. The clock recovery circuit of the XR-T5683 is not self resonant. The received data pulses are used to set the tuned circuit oscillating, after which the circuit will continue to ring for a number of cycles if no data pulses are subsequently received. The XR-T5683 converts these oscillations into a TTL level clock and outputs this signal to the remainder of the receiver circuitry.

RECEIVER CIRCUIT

A full circuit diagram of the receiver circuitry excluding macrocell connectors is included in Fig. 5. As with the transmitter, the operation of the receiver is selectable via two DIL switches (half of SW13-16) used to set DEMO (DEMO MODE) and CRC. In addition, a momentary action push switch (SW17, RX RESET) is included to reset the Timeslot Zero Receiver if required.

The timeslot zero spare bit outputs, Q1S, Q1N and Q3N to Q8N are buffered by the 74LS541 and are then input to a ULN2803 darlington driver. The open collector outputs of the ULN2803 are then used to drive 8 LEDs to display the data being received in the spare bits. The 8 alarm outputs are fed into the error latch sub-circuit, the diagram of this being shown in Fig. 6. The outputs from this circuit are fed into a second ULN2803 to drive a further 8 LEDs, giving a visible indication of any alarms.

The error latch sub-circuit has a control input, LATCH-EN, to enable latching of the alarms. This input is selected by a DIL switch (ER-LATCH, Fig. 5)). When LATCH-EN is high a single period alarm will be latched and as such will be visible on the LEDs. When LATCH-EN is low, all alarms will just be buffered and not affected in any other way. A momentary action push switch (SW18, ERROR LATCH RESET) can be used to reset any latched alarms.

The circuitry around the 74LS74 (Fig. 5.) is used to derive the bit 1, timeslot zero timing output from the timeslot zero output of the PCM receiver. The inverted timeslot zero output is used to preset the D-type latch, the output from which is then used to set the S-R latch, thus disabling further presets. On the next positive clock edge a logic '0' is clocked in to the D-type latch, thus giving a single period high going pulse. The low going edge of timeslot zero is then used to reset the S-R latch to enable the next preset. This output may be used to synchronise Codecs requiring a single period Frame Sync input.

This bit 1, timeslot zero output, along with TSZ, the 2.048MHz receiver clock, the 2.048Mbit data output and the 64Kbit timeslot 16 data output are all accessed via a 6-way 0.1 inch pitch PCB header, RX-CONN.

Transformer Components (Fig. 4)

T1 and T2 (each)

1 - off RM5 Ferrite pot core pair e.g Philips type 4322-022-59900 (similar to old type LA1577).

1 - off RM5 6 pin bobbin.

2 - off RM5 clamp.

For winding details, see winding instructions opposite.

Transformer Winding Instructions

1. 35/36 SWG wire:
   Start at pin 3, wind 22 turns, tap to pin 4.
2. Insulating Tape: Wind 1 turn.
3. 35/36 SWG wire:
   Continue from pin 4, wind 22 turns, end at pin 5.
4. Insulating Tape: Wind 1 turn.
5. 35/36 SWG wire:
   Start at pin 2, wind 22 turns, end at pin 6.

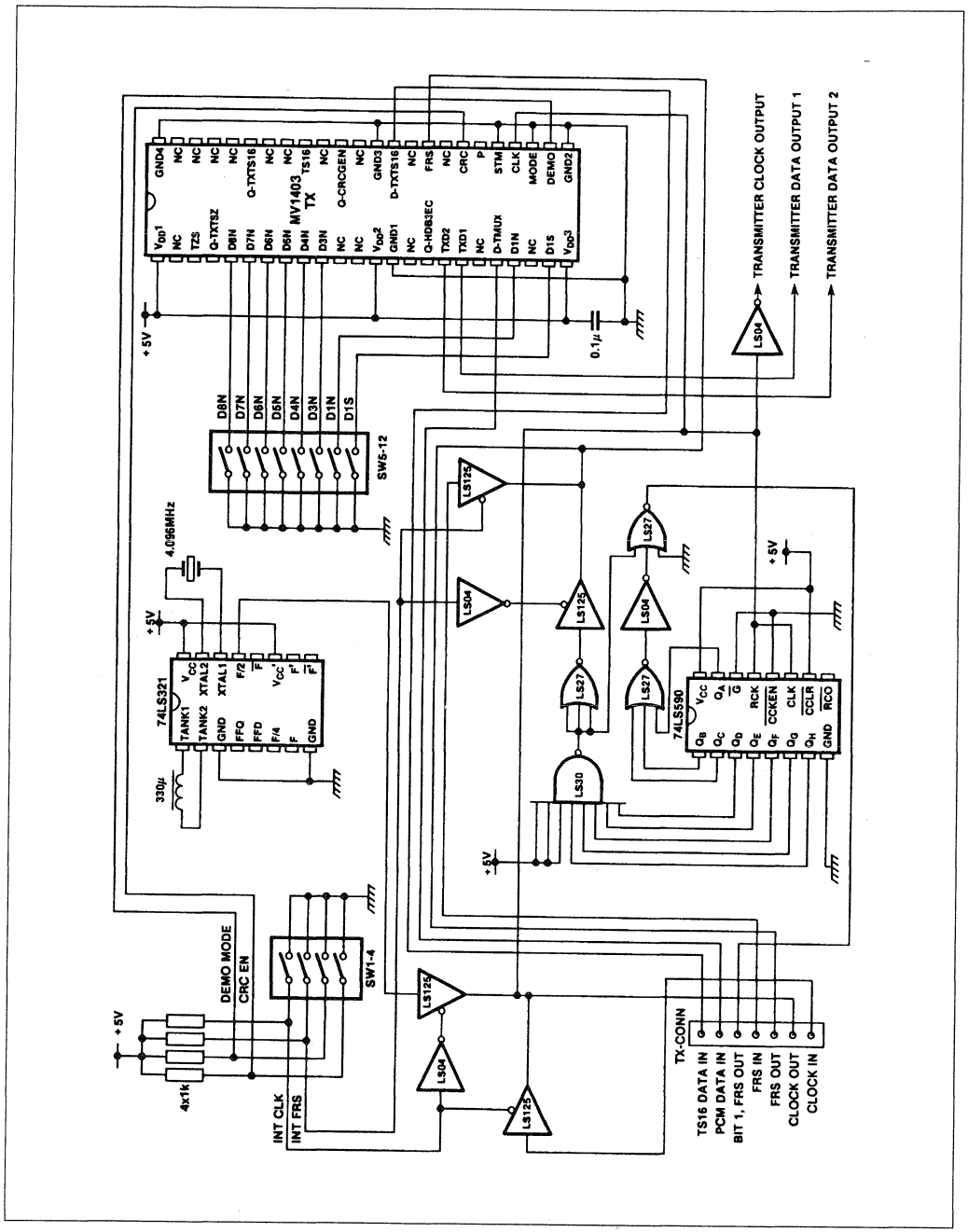


Figure 3: PCM Transmitter circuit diagram

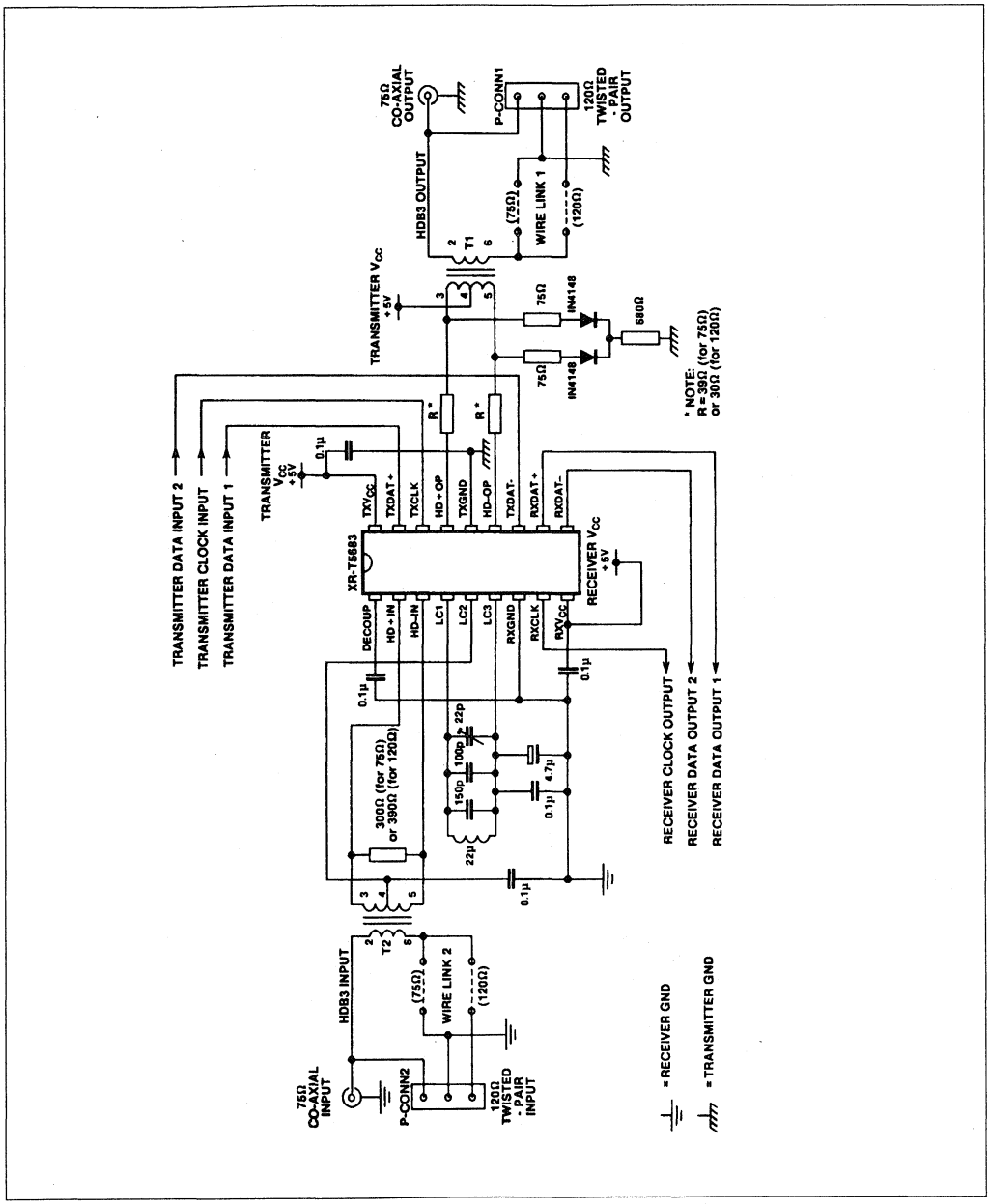


Figure 4: PCM line interface circuit diagram

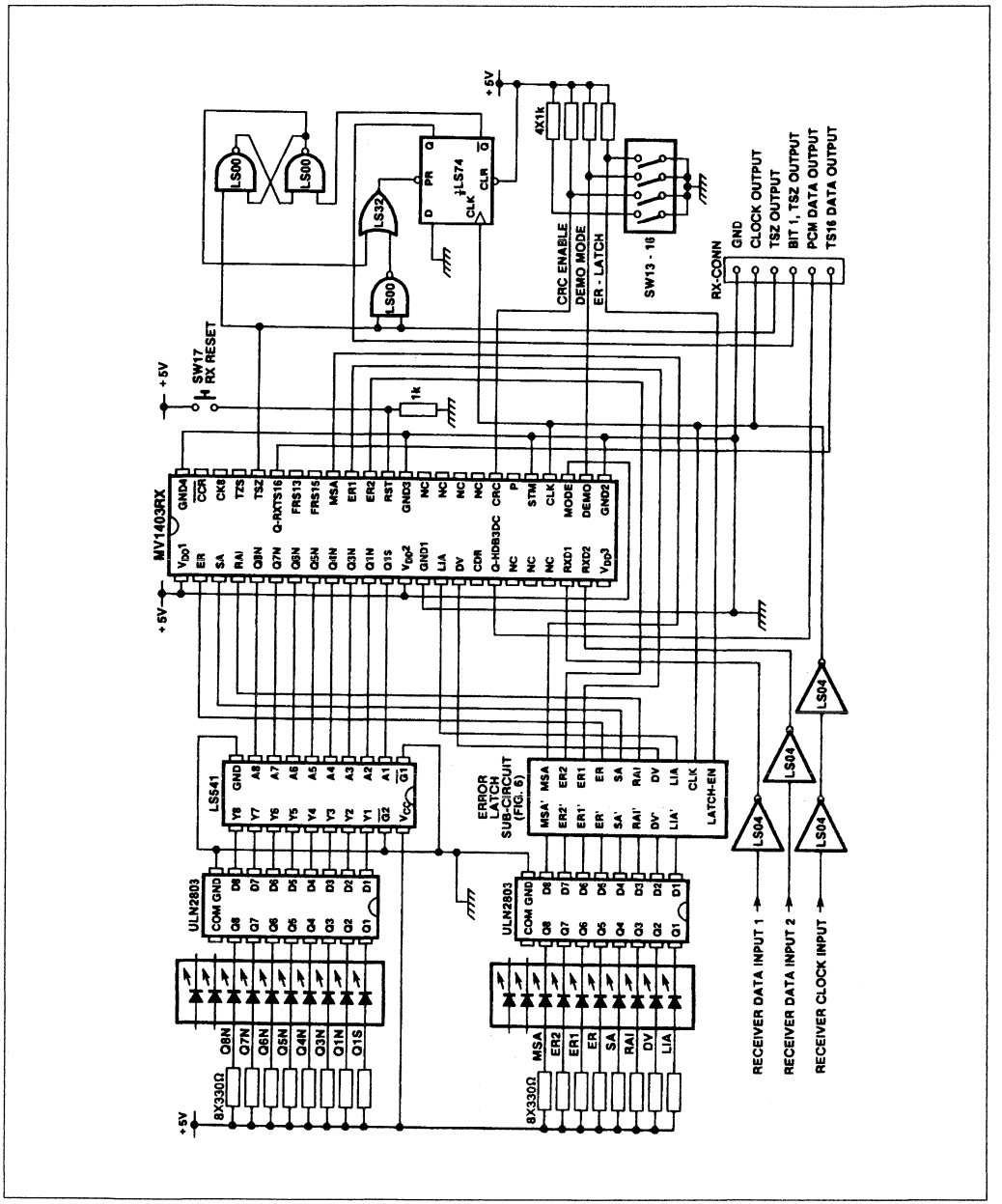


Figure 5: PCM Receiver circuit diagram

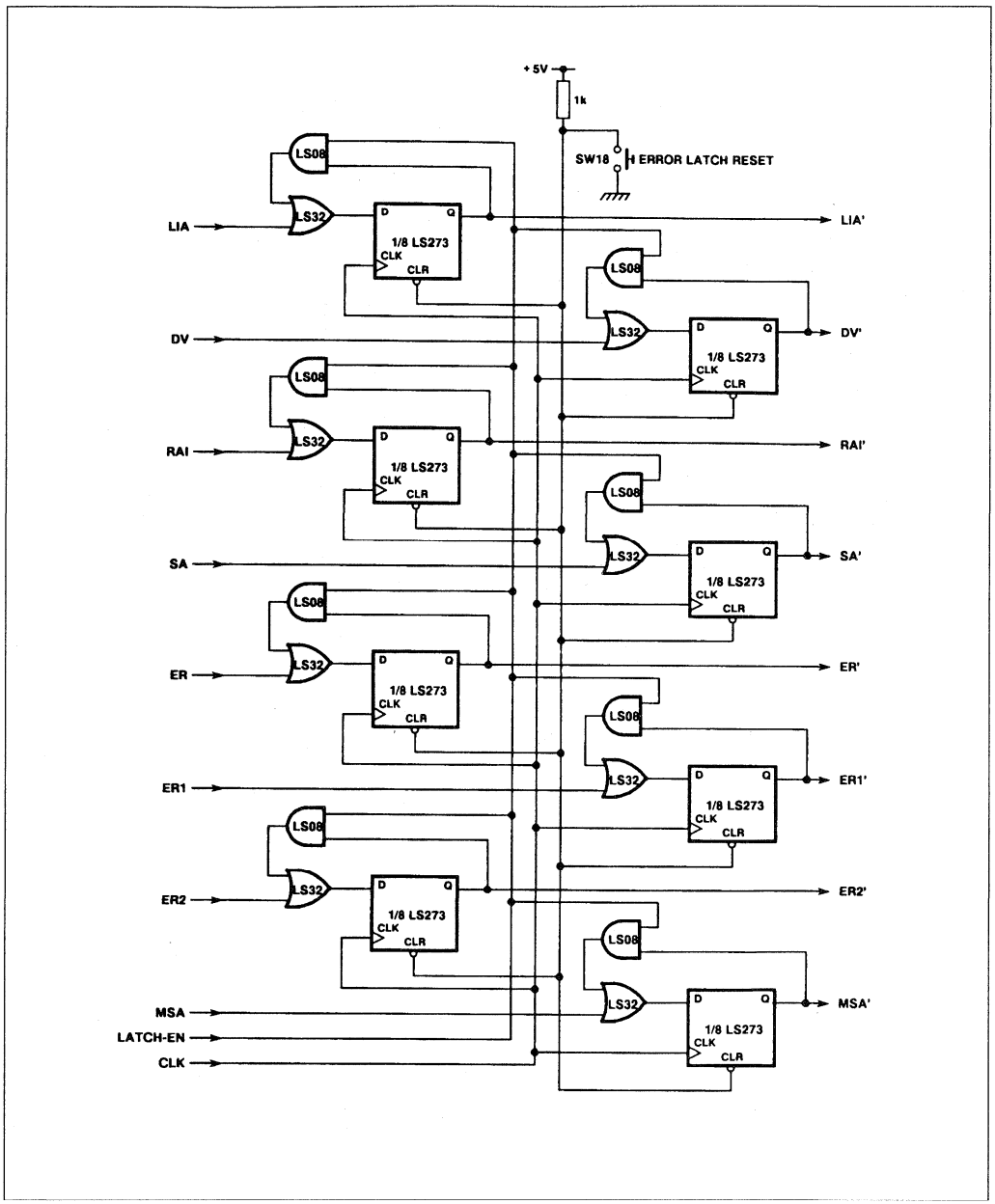
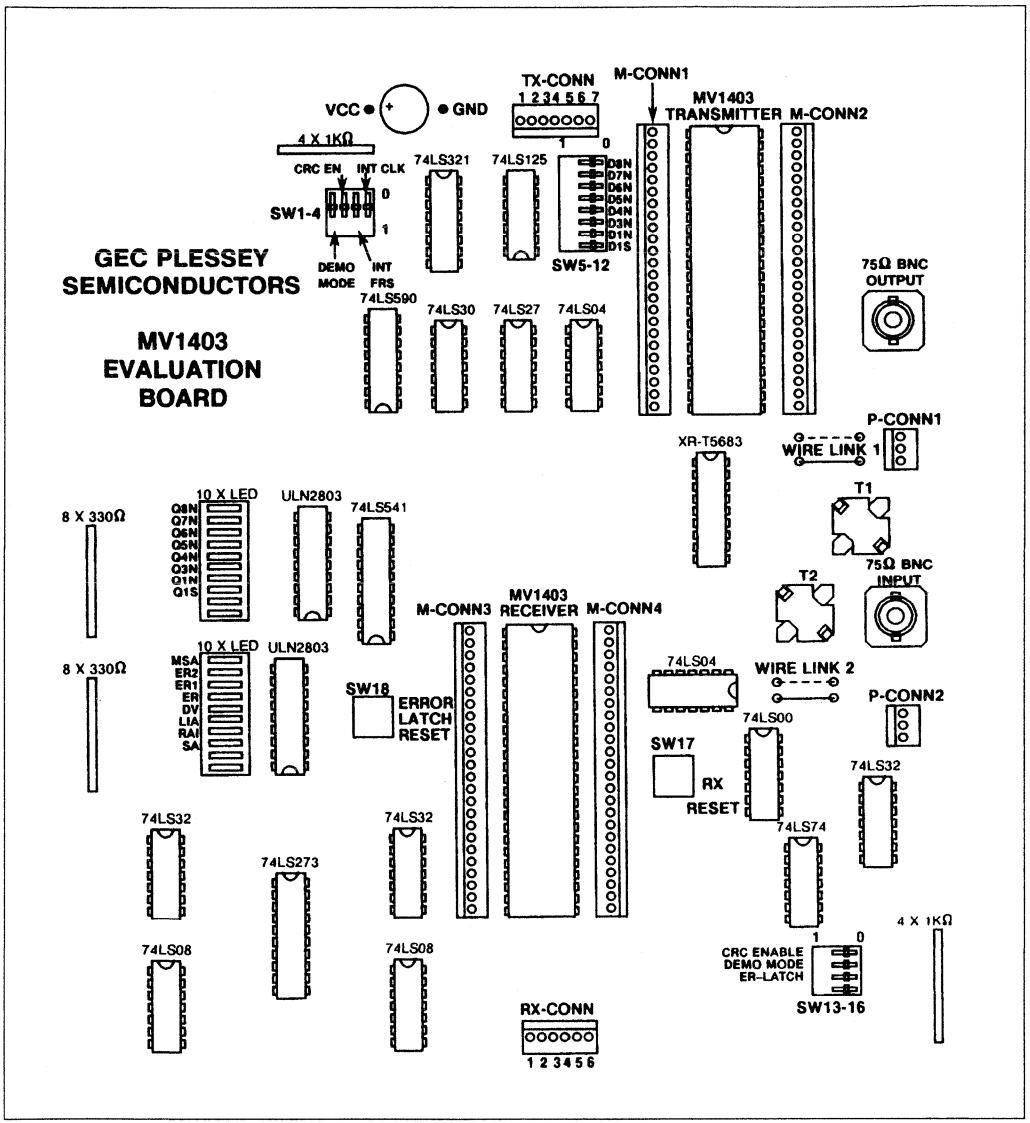


Figure 6: Error Latch Sub-circuit



TX-CONN PINOUT

1	CLK I/P	5	BIT 1, FRS
2	CLK O/P	6	PCM DATA I/P
3	FRS O/P	7	TS16 DATA I/P
4	FRS I/P		

RX-CONN PINOUT

1	TS16 DATA O/P	4	TSZ O/P
2	PCM DATA O/P	5	CLK O/P
3	BIT 1, TSZ	6	GND

Figure 7: Evaluation board layout - main components

Features of the MV3010-1 Subscriber Line Audio Circuit

Subscriber Line Audio Circuits (SLAC and COMBO devices) have been traditionally realised using switched capacitor techniques. Such devices have a mainly analog content with limited programmability. Digital Signal Processing (DSP) techniques have been used to realise the MV3010-1 SLAC (Subscriber Line Audio Circuit). This has allowed the analog content of the device to be minimised in favour of powerful DSP. The device therefore offers many features not found on even the most advanced switched capacitor design. This Application Note provides a ready summary of these features.

DSP REPEATABILITY

DSP techniques ensure excellent transmission parameter repeatability. This applies to such effects as part-to-part variations, long term aging, power supply dependence and temperature variations.

ADAPTIVE ECHO CANCELLATION FILTER

The first important additional feature available from the SLAC DSP routines is the inclusion of an echo cancellation filter. This can be enabled so as to reduce the level of any echo from line interface circuitry (due to a mismatch of terminating and line impedances). The filter can be used to ensure optimum Echo Return Loss (ERL) is achieved over a wide range of line lengths and terminating impedances. Most important of all, is the inclusion of a powerful self-adaptive echo cancellation algorithm, which can maintain required ERL over the life of the line, even if line length and/or telephone instruments should change.

A signal Correlator and programmable Double Talk detector form part of the adaptive algorithm, to ensure that resultant (adapted) ERL can never allow system instability. It is then completely robust, whatever signal types (i.e. frequency spectrum) are presented to it. The algorithm is discussed further in Application Note AN103-2 and a performance summary is given in Application Note AN104-2.

FLEXIBLE FIXED MODE CANCELLATION

The echo cancellation filter can also be used in a programmable fixed mode of operation, to give a predetermined response. It can then be optionally allowed to adapt continuously or for a user defined time period and then frozen (disable adaption).

Programming of a fixed response can be done accurately to meet most of the likely required responses. Each of the nine Finite Impulse Response (FIR) taps of the filter are fully programmable in the range -2 to + 2 using a 12 bit (2s' complement) data format. Each tap is spaced at 62.5µs delay giving at least 562.5µs of echo path delay that can be accurately cancelled. There is also the addition of a tenth tap which contains a recursive loop (Infinite Impulse Response type). This can add an exponential tail to the filter impulse response, so allowing even longer echo delays to be attenuated.

FREQUENCY EQUALISATION FILTERS

The DSP provides the option of user programmable 4 tap FIR type filters in both transmit and receive paths of the SLAC. These can be used to correct for amplitude and phase errors that may be introduced by external circuitry, such as 2-wire to 4-wire and 4-wire to 2-wire conversion. Alternatively, the SLAC's fixed CCITT/AT&T filter responses may be customised by these filters.

WIDE GAIN RANGE

(Transmission parameters fully specified)

The transmit and receive path gains are both programmable over a wide range at small linear step sizes, using a 12 bit (2s' complement) data format (typically <0.1dB adjustment). These ranges are:-

$$-\infty \leq \text{Transmit Gain} \leq +15.56\text{dB}$$
$$-\infty \leq \text{Receive Gain} \leq +6.02\text{dB}$$

The full Transmission path specifications meet or exceed CCITT requirements over most of this range, i.e. with 0 to + 13dB Transmit Gain and/or 0 to + 12dB Receive loss.

SINGLE POWER SUPPLY VOLTAGE

The MV3010-1 requires only a single +5V power supply (±5%), simplifying supply decoupling and board tracking. System reliability is improved over circuits needing dual supplies.

16 BIT LINEAR PCM ACCESS

This is available as a user selectable option alongside the more usual A-Law and µ-Law PCM codes. It can be used to simplify the implementation of such features as conference bridges or further external signal processing (e.g. ADPCM compression). This mode provides full 16-bit accuracy over the complete dynamic range.

CLOCK OFFSET PROGRAMMABILITY

In addition to user defined time slot assignment (up to 64 on each of dual Transmit/Receive PCM ports) it is possible to further offset the chosen time slot by additional PCM clock cycles. These can be from 0 to 7 cycles independently for each transmission path.

The device works in plesiochronous mode (CCITT G.701 2.6) where PCM clocks and synchronisation signals should be frequency locked to the device master clock, the exact phase relationships being unimportant.

PCM CLOCKING CAPABILITIES

The backplane interface of the SLAC has been made completely flexible, supporting a wide range of clock rates independently for the transmit and receive directions. Thus, either transmission path can be set with a clock rate between 64kHz and 4096kHz. In addition the inclusion of dual transmit and receive ports (via one of two selectable pins for each path) provides additional security of transmission, or can be used as a simple means of space switching in the exchange.

TRANSMISSION DIAGNOSTIC FUNCTIONS

The normal range of transmission diagnostic functions has been complemented by further user selectable functions. These include receive path disable, receive path 6 dB attenuate and a code to disable the fixed high pass filters of the SLAC.

STAND ALONE OPERATION

In most applications, the design of a line card utilising all the benefits of the MV3010-1 SLAC will require an actlve digital control interface to the device. This is used to fully control all the features, including the self adaptive cancellation filter, of the SLAC. However, a further possible mode of operation is possible with the MV3010-1, namely Stand Alone operation.

Stand Alone operation works by setting the functions of the device to its default conditions (as given in the data sheet). For this mode to be active, the control interface is hard-wired to predetermined input conditions. These input conditions may be changed to allow the device to be set to active or standby status (providing power saving capability) and to enable (with adaption) or disable the Cancellation filter. Thus for some applications, a greatly simplified line card design is possible.

MV3010-1 Achieves Stable Robust Adaption

This Application Note discusses the issues affecting the performance of the MV3010-1 Subscriber Line Audio Circuit (SLAC) Cancellation Filter (C Filter), giving particular regard to conditions under which the self adaption algorithm achieves stable and robust operation. Fig. 1 illustrates the basic system architecture for a line card application and shows the basic terminology used throughout this document. Specifically, the 'Near End' is considered to be the line card with the adaptive SLAC. The 'Far End' may be any other form of line card architecture, including an MV3010-1 based design.

Normal convention for the term Echo Return Loss is considered to be the level of receive PCM signal that appears in the transmit path. However, this parameter will change with any alterations to both Transmit and Receive gains programmed within the MV3010-1 (assuming an echo path exists). For this reason the term Cancellation is preferred, this being the attenuation of the PCM receive signal at DRA/DRB by the MV3010-1's C Filter, in combination with the line interface 'starting point', at the PCM transmit output DXA/DXB. The term 'starting point' is the basic echo level between the V_{OUT} and V_{IN} pins of the MV3010-1.

INTRODUCTION

The MV3010-1 contains a user-programmable echo cancellation filter (C Filter). This attenuates any part of the receive signal that may be present in the transmit path due to an imperfect hybrid (i.e. 2-wire/4-wire conversion) function. Retransmission of this signal back to the far end is therefore minimised. When optimally programmed, this filter can give excellent echo cancellation. Most lines in a real network will of course never be optimally programmed as the performance of each individual line's hybrid function will not be known to the system. In addition, the coefficients needed for optimum cancellation for each line will change with time, for example due to component aging or a change to the telephone instrument being used.

These limitations can be overcome by the use of self adaptive echo cancellation. In this set up, filter coefficients self adapt to changing echo conditions to maintain a minimum level of receive signal present in the transmit path. The MV3010-1 implements a Clipped LMS type adaptive filter based on the classic Widrow-Hoff algorithm. Particular care has been taken in its design to ensure that this algorithm is optimised and sufficiently well controlled to prevent any undesirable adaptions that may lead to network instability.

The algorithm has been extensively tested using various single and multiple sinusoids, prerecorded and live speech with a wide range of near and far end echo path combinations. In all cases (except where preprogramming was particularly accurate) adaptions have resulted in improved cancellation. Unwanted adaptions that may have led to network instability were always prevented. The features of the MV3010-1 C Filter are now described in greater detail.

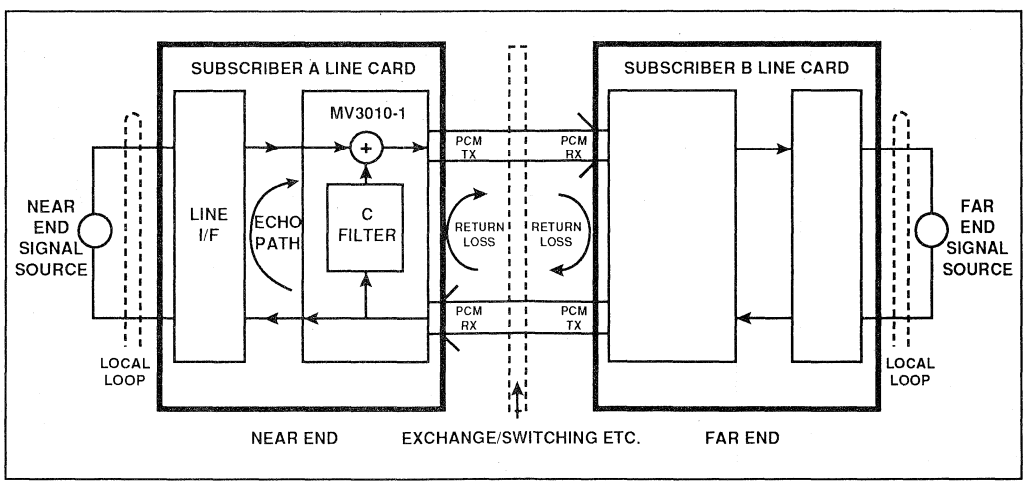


Fig. 1 Basic system architecture, End - End loop.

ADAPTION - THE PROBLEMS

The normal requirements for good adaption include a dominantly wideband far end signal. Note that we assume the adaptive filter to be operating at the near end; the far end signal is therefore received in PCM form from the network. The echo response around the near end line circuit is then readily cancelled by the adaptive filter. Fig. 2 illustrates a typical response to a wide band far end signal.

If the incoming far end signal is narrow band periodic (e.g. single tone or whistle) then a simple LMS adaptive filter would optimise cancellation for the frequencies present with no regard for the resultant response at other frequencies. Whilst this may give extremely good cancellation at the signal frequencies almost arbitrary cancellation will be obtained at other frequencies within the audio band. A possible degradation in overall ERL may then result. An example of this type of behaviour is given in Fig. 3. If far end overall ERL is also poor (as is likely if the far end has non-adaptive cancellation) then loop gain may approach unity at some frequencies. This may then allow oscillation to be triggered by noise components in the end-end loop. The filter may then re-adapt to attenuate this oscillation, allowing oscillation at some other frequency to build up. This behaviour is clearly unacceptable.

Periodic signals generated at the near end can also cause problems because the adaptive filter cannot determine from which end it originates. Adaption to minimise near end echo is only possible with a signal originating at the far end. However, if there is a large amount of far end echo, an adaptive filter can try to cancel a near end originating periodic signal using the echo from around the far end loop. Doing this may result in large adaptive coefficients in the C Filter (the near end signal is larger than the far end echo level). If there is also gain programmed in the transmit and/or receive directions (for a long line condition) then under these circumstances, oscillations can build up in the end-end loop.

ADAPTION - THE SOLUTIONS

The MV3010-1 solves these problems by adding a signal correlator circuit to detect periodic signals in the receive path, inhibiting adaption until a reasonably broad band signal is available.

A second feature, added to the basic algorithm, is the addition of a Double Talk detector. This has been added to give extra protection against undesirable adaptions. If we again consider the case of near end originating signals (and large far end echo), there may be some correlation which is not enough to cause the correlator to inhibit adaption (while the ideal signal to adapt to is a wide band noise source, the MV3010-1 must adapt to speech signals which contain some degree of correlation). It is very unlikely that signals which are not detected by the correlator will be a problem, but the addition of the double talk detector allows extra robustness to be built in.

The double talk detector compares the receive signal (which is being output to the analog line interface) with a reprocessed version of the incoming signal (i.e. near end plus echo at the analog input to the SLAC). This reprocessed signal is obtained by subtracting the C Filter output and any DC component from it, then multiplying this by the programmable (via the Control Interface) Double Talk Coefficient (DTC). Fig.4 shows a conceptual model of the detector operation. If the receive signal is smaller than the reprocessed transmit signal the adaption process is paused. Note that a zero or negative value for the DTC will disable the detector, whilst values up to +8.0 give a range of sensitivity to cater for different line interface circuits.

As double talk is equivalent to poor ERL, (the detector cannot distinguish the signal origin) the sensitivity of the detector must be less than the worst case echo level else adaption is effectively inhibited. Thus an optimum value for the DTC can be obtained after the C Filter has been preprogrammed. Thus by comparing the signal after the C Filter output has been

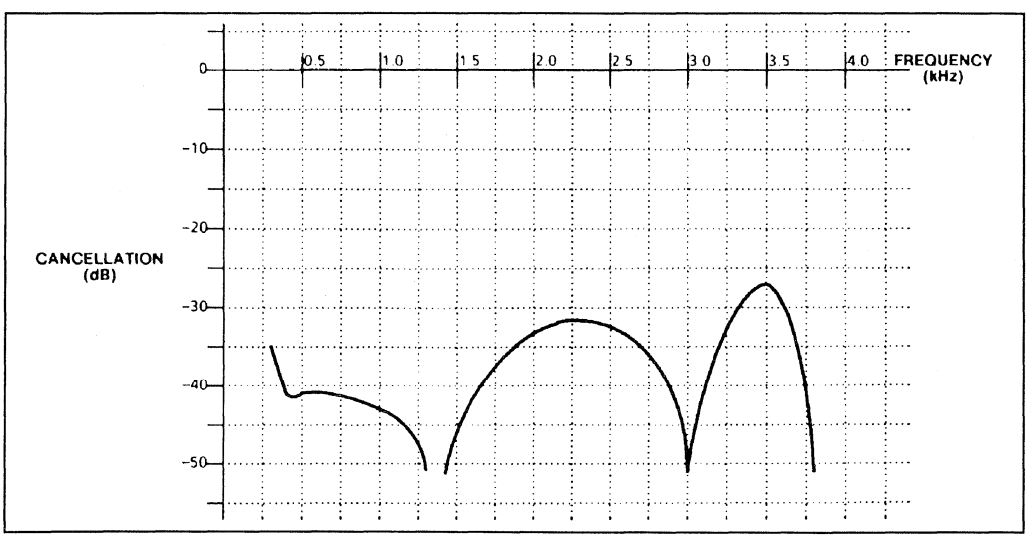


Fig.2 Typical Cancellation after preprogramming and Adaption to wide band far end signal.

subtracted from the transmit path, the double talk sensitivity can be improved (as opposed to comparing the incoming signal before the C Filter output has been removed) by the minimum Echo Return Loss Enhancement that the C Filter preprogramming gives with the expected loads.

Finally, an Oscillation Quench circuit has been built into the MV3010-1 to cater for the extremely unlikely event that a set of C Filter adapted coefficients result in oscillations in the end-end loop. If such an oscillation is detected, the last set of preprogrammed coefficients are restored to the C Filter foreground filter so as to quench the oscillation. Of course, the basic system must be stable with any programmed gains (transmit and/or receive), preprogrammed C Filter coefficients and far end echo, but this is an obvious requirement of even a stable nonadaptive system. It is not expected that the oscillation quench feature will ever be invoked in normal usage.

In summary, the MV3010-1 allows the advantages of adaptive echo cancellation (over a range of unknown conditions) to be obtained without using any special test signals other than the normal speech traffic, yet has built in immunity to conditions/signals that would otherwise cause undesirable adaptions. Full control of the adaption process is thus available by enabling/disabling (freezing the current set of coefficients) adaption, preprogramming the C Filter, controlling the correlator and programming the Double Talk Coefficient.

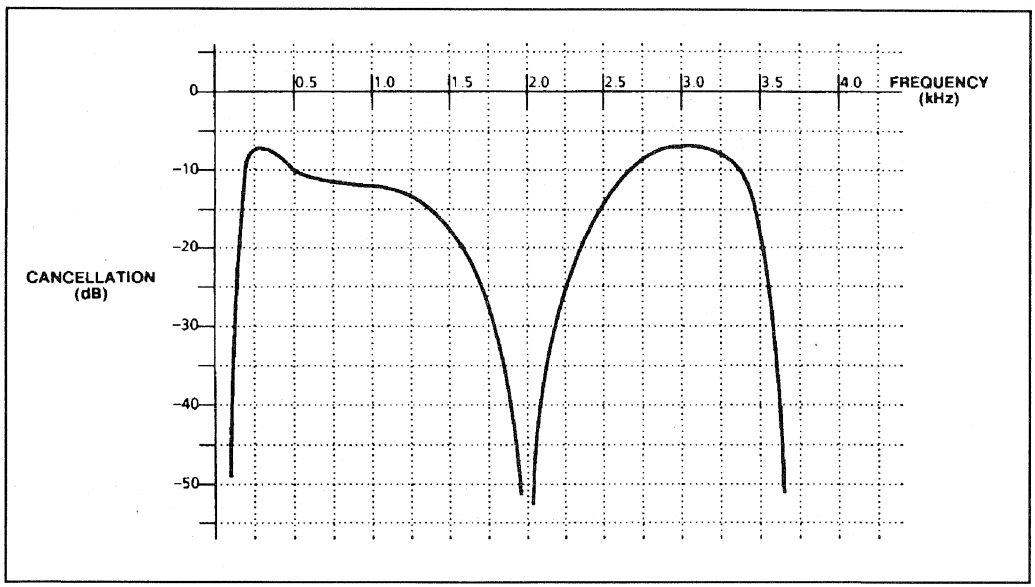


Fig.3 Typical Cancellation after Adaption to single tone far end signal.

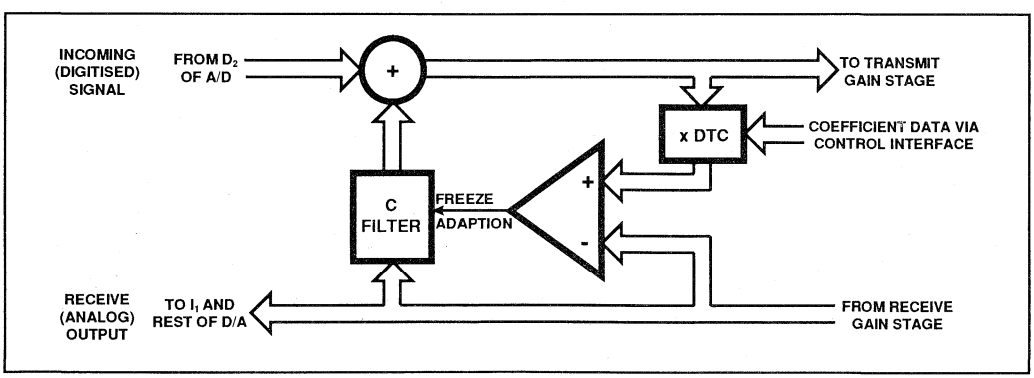


Fig.4 Double Talk Detector, conceptual model.

Benefits of the MV3010-1 Adaptive Echo Cancellation Filter

AN104-2

This Application Note summarises the typical echo cancellation performance of the MV3010-1 Subscriber Line Audio Circuit when used in Line Card type applications.

TEST CIRCUITS

Two different types of Interface Circuit to the 2-wire line were used in obtaining the results given. In each case, an MV3010-1 Demo Board and Controller PCB (see Application Note AN42) was used in association with the Line Interface. This is connected to the circuits shown in Figs. 1 and 2, to form two all-analog test circuits.

In Fig.1, an Op Amp drives the 2-wire line via 600Ω and a 600Ω-600Ω isolating transformer (type HED 25819). A single pole complex impedance is used as the line load (Z_N), with or without a simulated 7-mile line connected in series. For Fig.2, a real telephone (GPT designer phone type 5010) is used as the 2-wire line load (Z_N) and the line is driven by the GPS SL377 Subscriber Line Interface Circuit (SLIC). The SLIC circuit is terminated with a complex impedance, and again, a simulated 7-mile line may be connected in series with the phone. For both circuits, no cancellation circuit is provided externally to the MV3010-1 and the C Filter performance is evaluated by programming and enabling/disabling its various features.

TEST RESULTS

Two tables of results are given below. Table 1 summarises the results for the circuit of Fig.1, whilst the results in Table 2 are for the circuit of Fig.2.

The performance of the C Filter is given for six different conditions in each case. These are obtained by the following test procedure:

Step 1. C Filter disabled, 0 mile line.
Step 2. C Filter enabled after pre-programming for 0 mile line (using the technique described in AN84).
Step 3. C Filter adapted to white noise following step 2.
Step 4. C Filter disabled, 7 miles of line.
Step 5. C Filter enabled and pre-programmed with the coefficients of step 3 (7 mile cable still connected).
Step 6. C Filter readapted from step 5 to optimise the adaptive taps of the filter for the 7 mile line.

Measurements were taken with a nominal end-end gain, for both transmit and receive directions, of 0dB (i.e. both MV3010-1s on the demo board have transmit gain of 0dB and receive gain of 6dB to remove the effect of the difference in SLAC analog input and output dynamic ranges). The figures are quoted for the demo board analog output level relative to the analog input level. For each step in the tests, the worst case cancellation only that occurred at any frequency within a 200-3800Hz bandwidth, is quoted. Note that for each circuit, a small amount of cancellation results from the interface circuit, of a nominal 6dB, with a matched line load (i.e. $Z_N = Z_I$). Also, the line model assumes a specification of 277Ω/mile and 82nF/mile of cable.

CONCLUSION

The results of Tables 1 and 2, steps 3 and 6, show that the MV3010-1 C Filter can provide at least 20dB of Cancellation without any external circuitry. This is maintained over a wide range of line lengths (i.e. 0 to 7 miles), by use of its self-adaptive algorithm, starting from a single set of pre-programmed coefficients. Note that the structure of the filter, with multiple taps in the time domain, is well suited to matching real lines which may suffer from several reflections.

Test step	Line length	Worst case cancellation	Frequency
1	0 Miles	4.7dB	500Hz
2	0 Miles	12.1dB	300Hz
3	0 Miles	24.4dB	1010Hz
4	7 Miles	3.3dB	400Hz
5	7 Miles	17.7dB	300Hz
6	7 Miles	22.2dB	300Hz
Line Load = Z_N = 370Ω + (620Ω || 310nF) Input Impedance = Z_I = 600Ω			

Table 1 Transformer interface circuit results (See Fig.1)

Test step	Line length	Worst case cancellation	Frequency
1	0 Miles	5.5dB	2800Hz
2	0 Miles	25.5dB	1500Hz
3	0 Miles	31.1dB	3300Hz
4	7 Miles	4.7dB	300Hz
5	7 Miles	15.8dB	500Hz
6	7 Miles	23.0dB	200Hz
Line Load = Z_N = GPT Designer Phone 5010 Input Impedance = Z_I = 300Ω + (1kΩ || 220nF)			

Table 2 SLIC interface circuit results (See Fig.2)

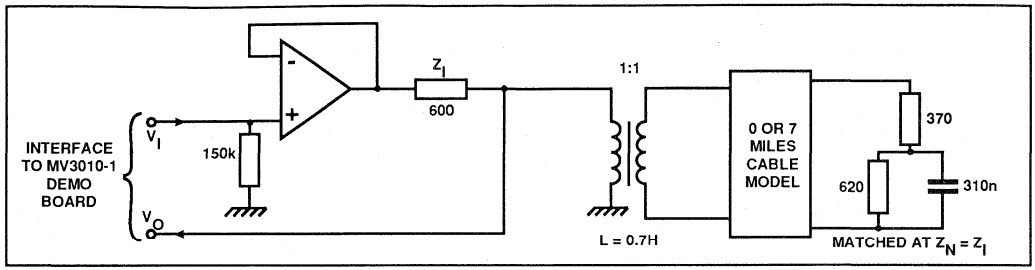


Fig.1 Cancellation test circuit, simple op amp line interface

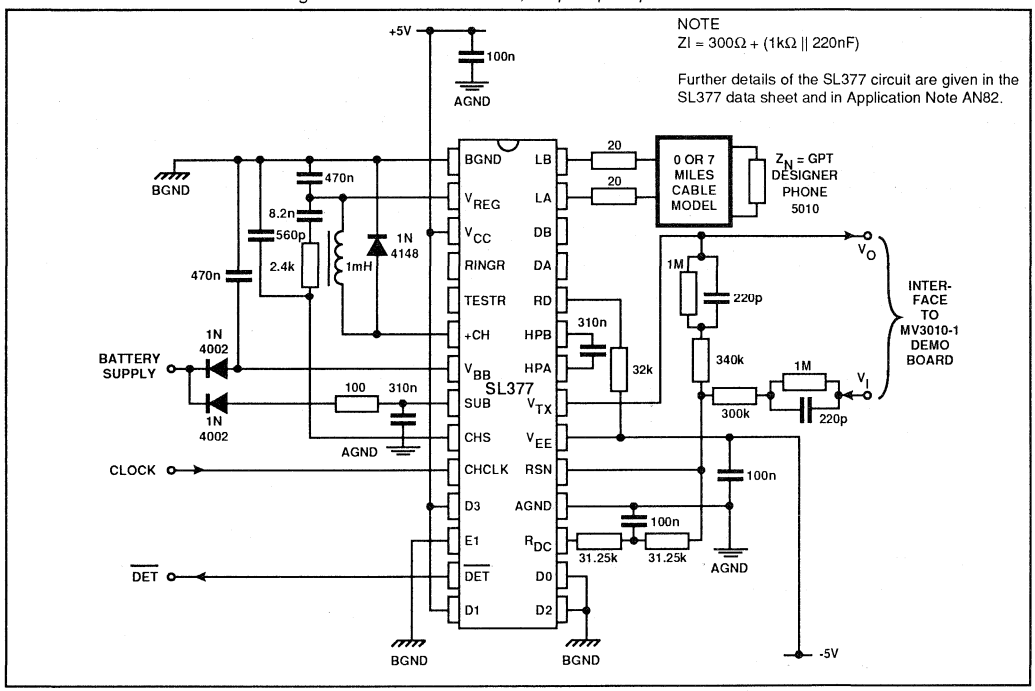


Fig.2 Cancellation test circuit, SL377 SLIC

Preprogramming the MV3010-1 C Filter using the Measurement Method

AN84-2

A major feature of the MV3010-1 SLAC is the C Filter and its adaptive mode, which is used to provide echo cancellation in various applications, such as line card architectures/line interfaces in a telephone system. Data on the MV3010-1 functions, including the C Filter operation, is given in the MV3010-1 data sheet.

In certain circumstances, reasonable echo cancellation can be obtained using only the adaptive taps of the MV3010-1 C Filter (A_1, A_3, A_5, A_7, A_9), as would be obtained if adaption starts from an all coefficients at zero condition. However, improved echo cancellation is usually obtained by preprogramming some, or all, of the taps of the C Filter. This provides a good starting point/initial cancellation with a known set of line and terminating impedances (preprogramming). The adaptive mode of the C Filter is then used to maintain or improve cancellation as these known conditions vary.

Calculating such coefficients for preprogramming the MV3010-1 C Filter for a known initial condition/echo level of the SLAC's line interface can be done in various ways. Since it is recognised that numerous different line interfaces and line/terminating impedances may be used in association with the SLAC, differing coefficients will be needed for each case. To make the job of determining these coefficients for preprogramming in a given application easier, this document describes a simple preprogramming technique. This technique, which uses the SLAC adaptive mode of the C Filter, avoids the need for software models and/or arduous calculations. It is therefore applicable to any type of line interface.

This preprogramming technique has been fully automated as part of a complete SLAC Evaluation Package. Application Note AN111-2 describes both the hardware (PCB evaluation board) and software (for IBM/compatibles) that are included in this package. It is recommended that this evaluation package be used for preprogramming the C Filter, although the technique described in this document may still be done manually if so required.

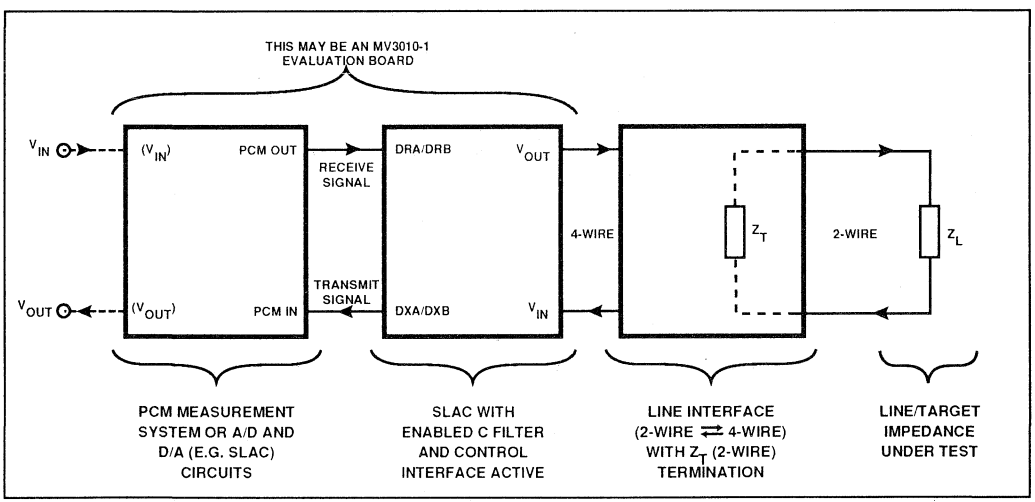


Fig.1 Preprogramming test set up

DESCRIPTION

The C Filter of the MV3010-1 is a ten tap FIR structure operating at a sample rate of 16kHz. The last tap has a recursive loop to provide better matching of the echo path should there be a long tail in the input response of the echo. The transfer function of the C Filter can be written as:-

$$H(z)= A_0 + A_1Z^{-1} + A_2Z^{-2} + .. + A_8Z^{-8} + \frac{A_9Z^{-9}}{[16 - (15Z^{-1})]}$$

where $Z= e^{j\omega t}$ with t= 1/16kHz and only the odd taps (A_1, A_3, A_5, A_7, A_9) are adaptive. This filter structure is described fully in the MV3010-1 Data Sheet.

Preprogramming the MV3010-1 uses the self-adaptive nature of the C Filter to characterise the echo path over the audio bandwidth. This is possible since even without preprogramming the C Filter, cancellation of a single tone to better than 50dB is possible using only the adaptive (odd) taps. (Note that the C filter correlation should be disabled to allow adaption to a single tone. The correlator is normally enabled for use in line card environments to prevent adaption under certain systems/line conditions that otherwise may cause instabilities/oscillations to occur if adaption was to take place - see AN103-2, for details.) C Filter coefficients obtained in such a set up are then a measure of the real and imaginary parts of the echo path transfer function, at the frequency of the single tone used. Thus, if this type of measurement is repeated at various frequencies across the audio bandwidth, then the resulting sets of coefficients obtained are a measure of the echo path transfer function across the band.

After this information has been obtained, a single set of coefficients is generated such that when these are programmed back into the C Filter (nonadaptive mode), then good echo cancellation will result for the characterised echo path.

This calculation is achieved using a simple computer program that utilises the individual sets of coefficients as input data. Firstly the program calculates the nature of the echo path as measured. Secondly, assuming all zero coefficients as a starting point, the program uses an iterative technique to search for a set of coefficients that best match this calculated response. This is achieved by varying each tap value in turn, by the largest possible step size, and calculating the error between the required response and that obtained from this new set of coefficients. The greatest improvement in this error by a change (±) in a single coefficient by the step size is stored for comparison. The program now searches for the next best change of a single coefficient to produce the least error. This process continues until it is no longer possible to reduce the error (between the required response and these search coefficients) by changing a single tap by the largest step size. The step size is reduced by a factor of two, and the program repeats the search procedure. This process continues until the smallest possible step size of a coefficient is reached. The program then prints out the final set of coefficients giving the best match of the C Filter response to the measured echo response.

TAKING THE MEASUREMENTS

The measurement technique involved is very straightforward, and is now described in detail in this section. However, it is recommended that the MV3010-1 Evaluation Package is used to automate this procedure. If this is not possible, then measurements may be made manually at a customer site or by a GPS Applications Engineer.

The initial measurements at spot frequencies are made using the test set up shown in Fig. 1. The line interface circuit 4-wire port, with the desired termination impedance (Z_T), is connected to the 4-wire port of the MV3010-1 (i.e.V_{IN}/V_{OUT}) with the target line impedance connected to the 2-wire port. MV3010-1 transmit and receive gains are set to 0dB with all filters, except the C Filter (nonadaptive), disabled. Connections to the PCM ports of the MV3010-1 are now made in order to apply a test tone of about 2Vp-p equivalent to the DRA input. This signal can be generated by a PCM Test System, another MV3010-1 'back to back' (as for the MV3010-1 Evaluation Board - see Application Note AN111-2) or other suitable A-D/D-A system. The frequencies used for these spot frequency measurements are shown in the blank form 'C Filter Preprogramming Measurements' at the end of this application note.

Under the conditions just described, the signal level at the MV3010-1 PCM output (DXA), depends on the echo level of the line interface. If C Filter adaption is enabled (both the double talk detector and correlator features of the C Filter should be disabled), this signal should now be reduced to a level 50dB, or better, below the original level. Note that the better the cancellation obtained, then the better the coefficients represent the characteristics of the echo path at the test frequency, so the greater is the accuracy of the final preprogramming (broadband) result. Single tones can cause adaption to converge on many different sets of coefficients with differing resultant cancellation. If sufficient cancellation does not result, it may therefore be necessary to readapt by momentarily switching the test frequency to another value, or changing to a broadband signal. The input signal should be returned to the original setting to ensure the C Filter now cancels to better than 50dB. Once this situation has occurred, adaption should be disabled, and the coefficient values read out via the MV3010-1's DI/O pin (as described in the data sheet). The resulting Hex data should be recorded on the blank form mentioned earlier. The whole procedure is then repeated at each frequency, listed on this form, in turn.

EXAMPLES

This section illustrates the preprogramming technique by presenting some examples of line interfaces/echo paths that are connected to the MV3010-1. In all cases, note that the term cancellation refers to the attenuation of the receive PCM input signal (DRA/DRB) by the SLAC C Filter/line interface, at the PCM transmit output (DXA/DXB). The actual Echo Return Loss (ERL) from PCM input to PCM output will exhibit an extra 6dB loss due to the difference between V_{OUT} and V_{IN} dynamic ranges (assuming both transmit and receive gains are set to unity i.e. 0dB). Where adaption has been done after preprogramming, a broadband signal (a suitable signal would be white noise or a sinusoid swept from 0-4kHz at a 50ms rate) has been used to ensure broadband cancellation. All measurements of cancellation are done with the C Filter in its nonadaptive mode or disabled to show starting conditions.

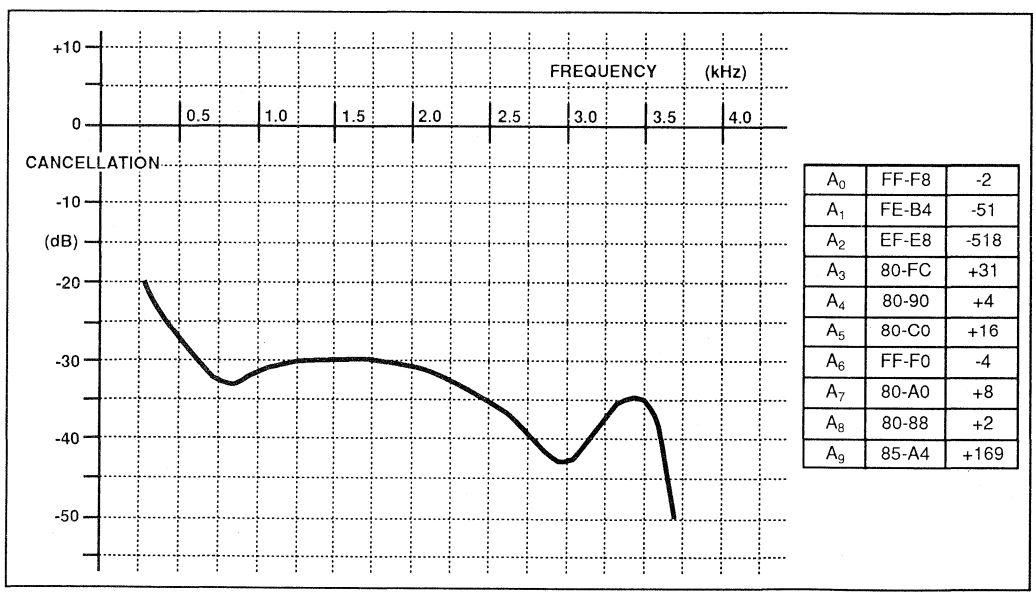
EXAMPLE 1

This directly links the MV3010-1 V_{OUT} pin to the V_{IN} pin via a 10µF DC blocking capacitor. The results confirm that the MV3010-1 internal delays from the point where the receive signal is input to the C Filter, through the analog interface and back to the C Filter output summing node, is nominally 125µs ($\approx A_2$ of the C Filter) with a gain around the loop of nominally -8/15 (A_2 = -0.533 or coefficient value -546/Hex EE-F8).

Fig. 2 lists the coefficients obtained at the spot frequencies, whilst Fig.3 gives the cancellation obtained after preprogramming the MV3010-1. Also listed are the coefficients obtained as output by the computer program. Note the close correlation between the A_2 theoretical and preprogramming values. Fig. 4 shows the enhancement obtained after adaption to a broadband signal, and again lists the coefficients that result.

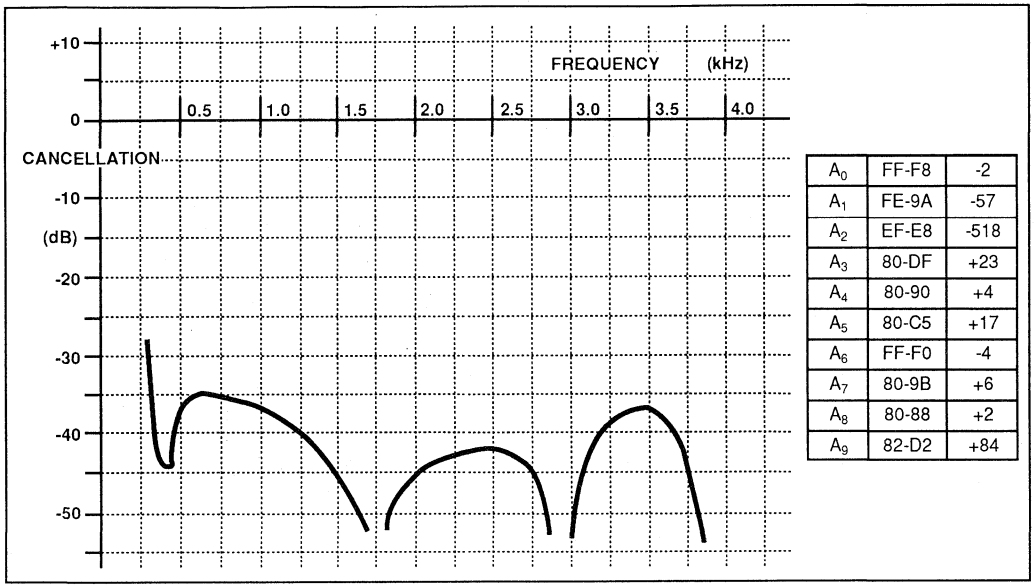
Frequency (Hz)	A_9	A_7	A_5	A_3	A_1
200	84-C9	FD-A4	81-9F	F9-D1	F6-9C
300	82-F3	FD-EC	83-FE	F7-EA	F5-B7
500	88-CD	FE-A3	82-AA	F8-87	F7-DC
800	88-B2	FF-C0	82-B0	F7-EA	F6-A6
1200	83-97	FC-8B	82-DC	F6-FA	F2-A6
1700	FF-93	FF-9B	80-D5	F5-EE	F3-EE
2100	80-EE	80-8B	81-FB	F5-A1	F3-EF
2400	95-9E	FE-A4	84-B2	F3-AD	F6-8D
2700	8B-E2	FA-DD	85-F2	F6-D3	F9-A8
3000	82-B2	FC-9C	84-B7	F5-92	F2-A6
3300	8C-D5	F9-F4	86-87	F8-F6	F0-C7

Fig.2 Spot frequency coefficients for Example 1



A_0	FF-F8	-2
A_1	FE-B4	-51
A_2	EF-E8	-518
A_3	80-FC	+31
A_4	80-90	+4
A_5	80-C0	+16
A_6	FF-F0	-4
A_7	80-A0	+8
A_8	80-88	+2
A_9	85-A4	+169

Fig.3 Cancellation after preprogramming; Example 1



A_0	FF-F8	-2
A_1	FE-9A	-57
A_2	EF-E8	-518
A_3	80-DF	+23
A_4	80-90	+4
A_5	80-C5	+17
A_6	FF-F0	-4
A_7	80-9B	+6
A_8	80-88	+2
A_9	82-D2	+84

Fig.4 Cancellation after preprogramming and adaption; Example 1

EXAMPLE 2

This makes use of a simple operational amplifier and transformer line interface circuit, as shown in Fig.5. The interface was designed to be matched with R_L=560Ω and assumes an inductance from the transformer of 0.7H. Under these conditions this circuit gives a reasonable 30dB of initial cancellation without use of the MV3010-1. This degrades significantly as the line impedance becomes mismatched with the 2-wire termination impedance. The example given uses a mismatch of 430Ω as the echo test network (Z_L = 430Ω), the cancellation obtained being shown in Fig.6. Similar to example 1, Fig.7 shows the spot frequency coefficients and Fig.8 the cancellation resulting from preprogramming. Lastly, Fig.9 shows the enhancement obtained by adaption together with the new set of coefficients.

EXAMPLE 3

Example 3 makes use of one of the range of Subscriber Line Interface Circuits (SLICs) available from GEC Plessey Semiconductors, the SL377, to interface the MV3010-1 to the line. The circuit diagram of the SL377 application is shown in Fig.10, with a full description of the device given in the data sheet and applications information given in the SL376/SL377 Application Note AN82-2.

The SL377 makes no attempt to separate the directions of transmission such that 100% of the received 2-wire signal is returned to the 4-wire output. With the line impedance balanced at the 2-wire termination (set to 600Ω in this case) this means the nominal 4 to 4-wire gain (echo) is 0dB, as shown in Fig.11. Spot frequency measurements gave the coefficients of Fig.12, with better than 45dB of cancellation in each test. The resulting preprogramming coefficients and cancellation are both given in Fig.11. Following self adaption, an improvement of ~ 5dB to better than 25dB across the band was obtained as illustrated in Fig.13, along with the modified coefficients. Lastly, comparing the two curves of Fig. 13 shows the necessity of preprogramming, in this case. This is because the SL377 echo is dominantly centred on coefficient A_2, which is not involved in the adaptive process.

THE COMPUTER PROGRAM

The software for this preprogramming technique was written in PASCAL. It forms part of the MV3010-1 Evaluation Package, or can be supplied separately for use at a customer location on the IBM PC or compatibles. Alternatively, the blank form at the end of this application note can be copied, filled out as appropriate, and returned to GEC Plessey Semiconductors as indicated. After this has been processed by the computer, the results can be returned to the customer. It must be remembered that the resulting coefficients, so returned to the customer, will only provide the necessary degree of preprogramming if the spot frequency measurements were made correctly. Finally, as mentioned earlier, the entire preprogramming procedure can be carried out by GEC Plessey Semiconductors if the customer makes the relevant circuit diagrams and/or hardware available.

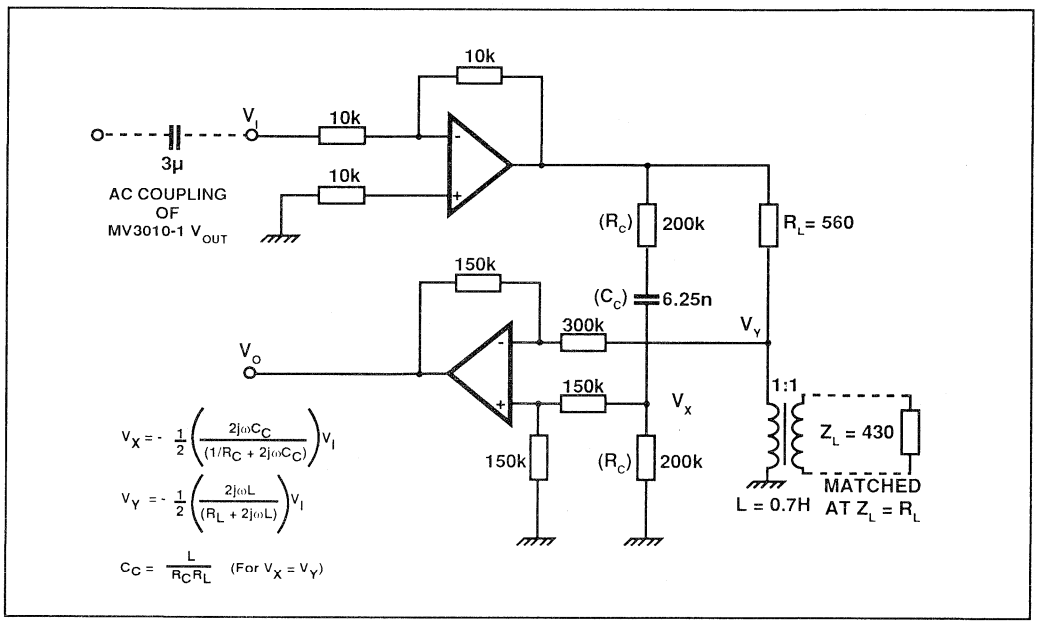
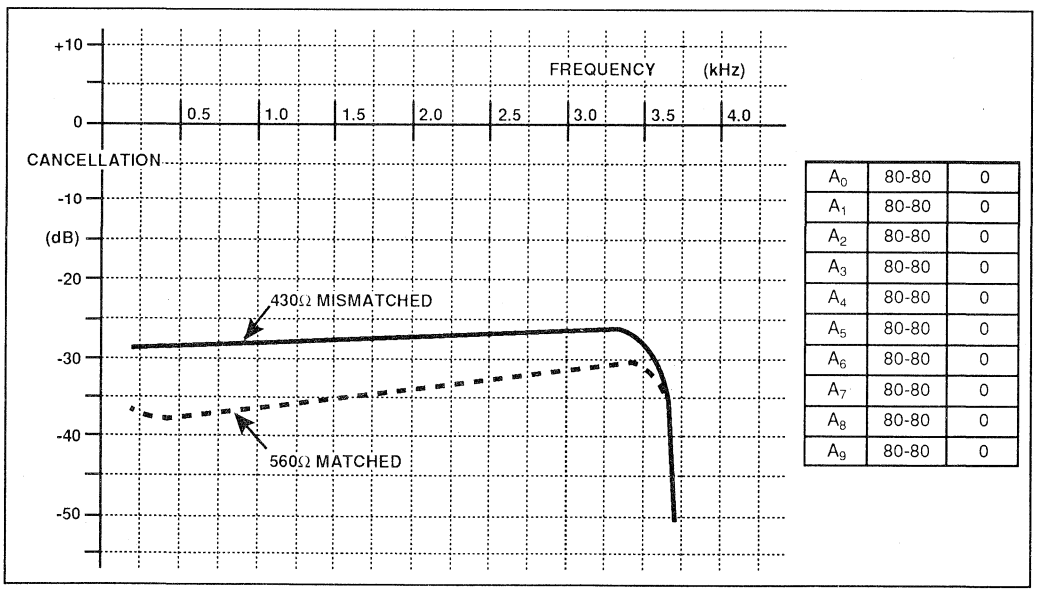


Fig.5 Simple op amp & transformer line interface circuit; Example 2.

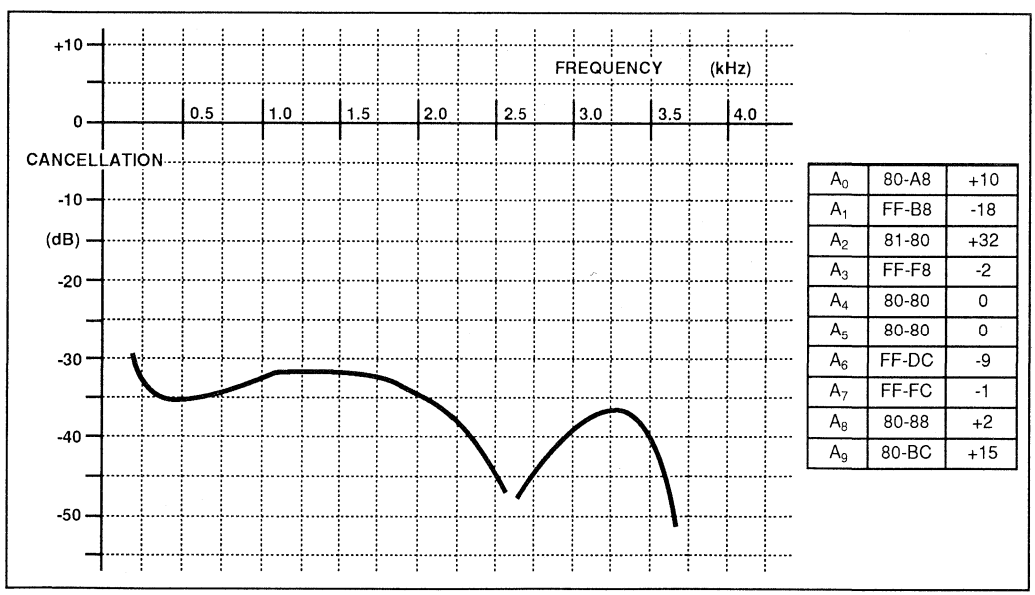


A_0	80-80	0
A_1	80-80	0
A_2	80-80	0
A_3	80-80	0
A_4	80-80	0
A_5	80-80	0
A_6	80-80	0
A_7	80-80	0
A_8	80-80	0
A_9	80-80	0

Fig.6 Initial cancellation produced using circuit of Fig.5 (Example 2)

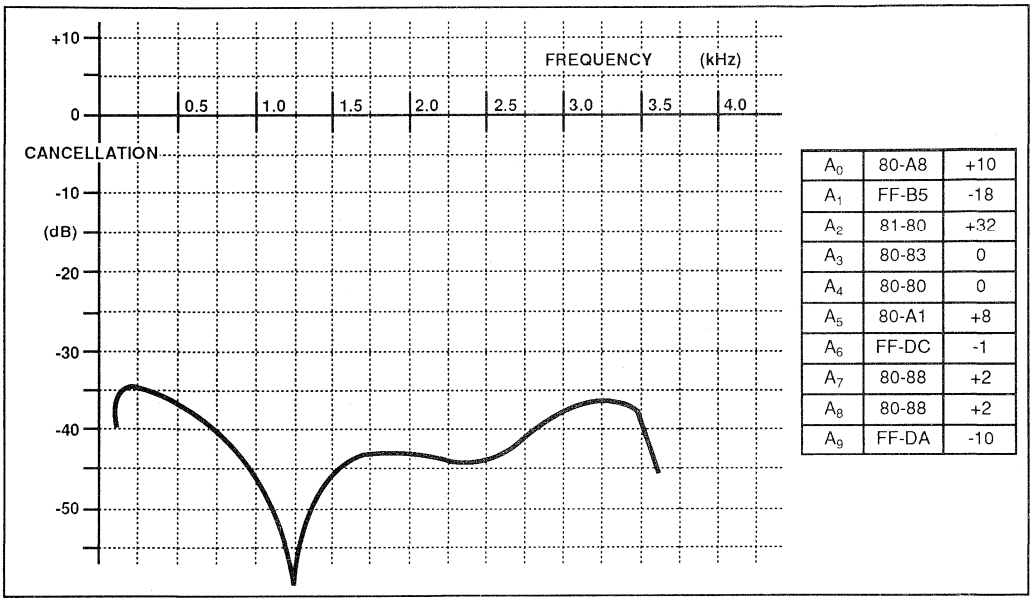
Frequency (Hz)	A_9	A_7	A_5	A_3	A_1
200	81-F9	FD-A2	FF-AA	FE-F8	84-C4
300	FC-F5	81-DB	FF-B4	81-AA	FE-86
500	82-EC	FF-CA	FF-AA	81-B9	80-E8
800	FC-A0	80-C3	FE-99	81-E3	FF-A9
1200	FB-EA	83-91	FA-B5	85-A0	FE-EC
1700	FE-E9	80-D3	FE-D6	81-E3	80-8A
2100	FF-B1	FF-E2	80-80	80-C3	80-AF
2400	FF-CE	FF-F7	FF-F8	80-DF	80-AD
2700	FE-E6	80-94	FF-BC	80-AD	FF-DA
3000	FD-EE	FF-F3	FF-CC	80-C7	80-9F
3300	FF-87	80-95	FF-D8	80-C8	80-AB

Fig.7 Spot frequency coefficients for Example 2



A_0	80-A8	+10
A_1	FF-B8	-18
A_2	81-80	+32
A_3	FF-F8	-2
A_4	80-80	0
A_5	80-80	0
A_6	FF-DC	-9
A_7	FF-FC	-1
A_8	80-88	+2
A_9	80-BC	+15

Fig.8 Cancellation after preprogramming; Example 2



A_0	80-A8	+10
A_1	FF-B5	-18
A_2	81-80	+32
A_3	80-83	0
A_4	80-80	0
A_5	80-A1	+8
A_6	FF-DC	-1
A_7	80-88	+2
A_8	80-88	+2
A_9	FF-DA	-10

Fig.9 Cancellation after preprogramming and adaption; Example 2

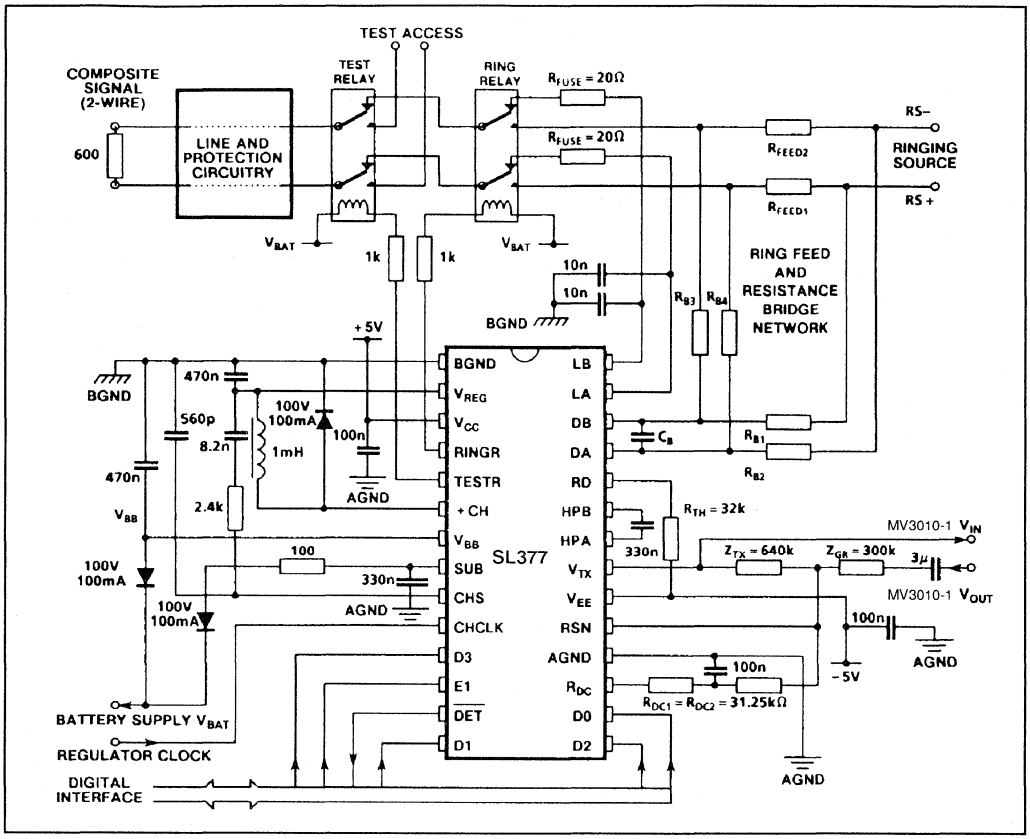
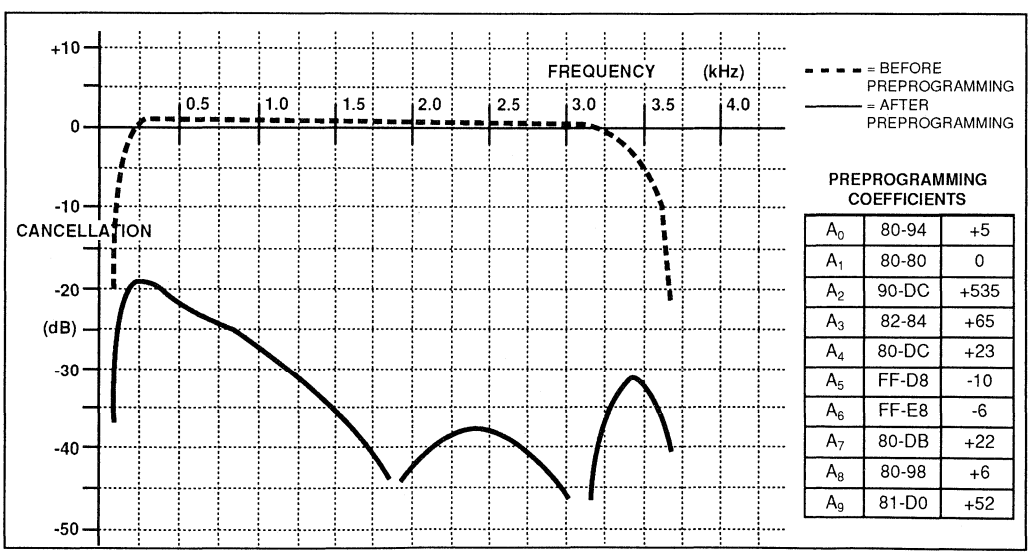


Fig.10 SLAC with SL377 SLIC line interface (See SL377 data sheet and AN82-2 for details); Example 3

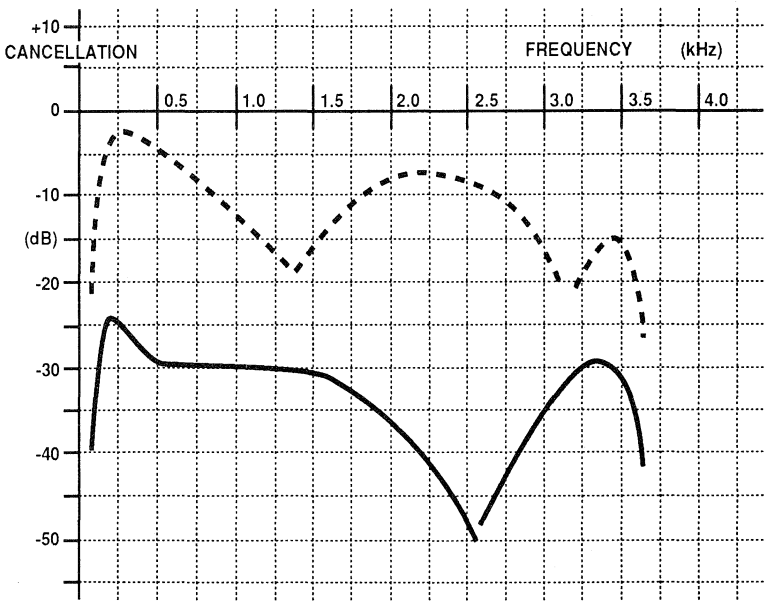


A_0	80-94	+5
A_1	80-80	0
A_2	90-DC	+535
A_3	82-84	+65
A_4	80-DC	+23
A_5	FF-D8	-10
A_6	FF-E8	-6
A_7	80-DB	+22
A_8	80-98	+6
A_9	81-D0	+52

Fig.11 Cancellation before and after preprogramming; Example 3

Frequency (Hz)	A_9	A_7	A_5	A_3	A_1
200	80-C6	80-AE	FF-91	88-8F	8A-E8
300	FE-B3	84-9D	FB-86	8A-D8	88-EB
500	F1-DC	85-B3	FB-A2	8A-9F	85-D5
800	86-91	82-B6	FB-C9	8E-DF	88-CA
1200	8E-C1	FF-DC	80-F5	8C-B7	88-A7
1700	85-B4	FC-83	84-DB	87-84	8D-99
2100	80-F7	80-F8	FA-EC	8E-BC	88-91
2400	FE-DF	84-A5	FA-E3	8E-D7	87-DD
2700	FE-D4	82-E9	FA-DE	8D-E6	88-FC
3000	F4-AD	83-E6	FA-EC	8C-EE	8A-DA
3300	FC-B1	86-C4	FA-9F	8B-BE	8D-ED

Fig.12 Spot frequency coefficients for Example 3



COEFFICIENTS AFTER ADAPTING FROM A_0-A_9 = 0

A_0	80-80	0
A_1	8E-98	+454
A_2	80-80	0
A_3	8E-C0	+464
A_4	80-80	0
A_5	FD-8F	-93
A_6	80-80	0
A_7	85-C6	+177
A_8	80-80	0
A_9	87-B5	+237

COEFFICIENTS AFTER ADAPTING FROM A_0-A_9 = PREPROGRAMMED

A_0	80-94	+5
A_1	FF-D7	-11
A_2	90-DC	+535
A_3	81-DA	+54
A_4	80-DC	+23
A_5	FF-B6	-20
A_6	FF-E8	-6
A_7	80-A2	+8
A_8	80-98	+6
A_9	FD-CB	-78

Fig.13 Cancellation due to adaption from C Filter empty and after preprogramming; Example 3

SLAC MV3010-1 C FILTER PREPROGRAMMING MEASUREMENTS

Complete Section B and Return to:- TELECOMS MARKETING MANAGER
GEC PLESSEY SEMICONDUCTORS
CHENEY MANOR
SWINDON
WILTS SN2 2QW
UNITED KINGDOM
TELEPHONE (44) 0793 518000
FAX (44) 0793 518411

[A] DESCRIPTION

The GEC Plessey Semiconductors recommended method of preprogramming the SLAC C Filter, for fixed or self adaptive mode of operation, uses the self adaptive mode to characterise the line interface (echo path) between SLAC V_{OUT} and V_{IN} pins. This should be carried out using the SLAC Evaluation Package. If this is not possible, then the measurement may be done manually using this form. The line interface should be terminated with the desired 'Target Impedance' with the SLAC operating with default conditions (i.e. transmit and receive gains set to unity). The C Filter is enabled and set to adapt from all coefficients at zero (80-80) for each frequency listed below, ensuring that the correlator is disabled (code B5) to allow adaption to a single tone. The procedure is summarised as follows:-

1. Apply a test signal at the PCM input port (DRA) equivalent to 2V p-p (the exact level is not important).
2. Measure the level of Echo Return Loss (ERL) at the PCM output port (DXA) at the test frequency. This should be at about -50dB for most line interfaces. If this level is not achieved then re-adapt until good ERL results. Adaption can be initiated by switching to another frequency (or to a broad band signal) before returning to the test frequency, should any difficulties be obtained.
3. With the C Filter now set to its nonadaptive state, read out the Hex values of the coefficients via the SLAC DI/O pin. Details of how this is done are given in the SLAC Data Sheet. The coefficient order will be A_8, A_6, A_4, A_2, A_0, A_9, A_7, A_5, A_3, A_1 (fixed or nonadaptive taps will of course read zero i.e. 80-80).

[B] SPOT FREQUENCY RESULTS (Hex Values)

Frequency (Hz)	A_9	A_7	A_5	A_3	A_1
200					
300					
500					
800					
1200					
1700					
2100					
2400					
2700					
3000					
3300					

[C] COMPUTER COMBINED COEFFICIENTS

COEFFICIENT	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9
VALUE (HEX)										
BINARY (Normalised to 1024)										

[D] ADDITIONAL INFORMATION

CUSTOMER AND CONTACT:-
LOCATION:-
TELEPHONE:-
APPLICATIONS INFORMATION:-

Form for recording spot frequency measurements

PABX/Line Card Control Circuit

This application note details how a control circuit and up to 128 Subscriber Line Audio Circuits (SLACs such as the GPS MV3010-1 SLAC) can be connected together to form a simple PABX.

The two possible modes of operation of the control circuit are described, showing in each case how it is connected to the matrix of SLACs. The controller has been designed to interface to an industry standard microprocessor (such as an Intel 8051), and to allow control data to be written and read via the SLAC's serial control port.

The whole circuit has been designed using 74HCT logic throughout and operates from a single 4MHz clock source generating antiphase 2MHz clock signals.

DESIGN CONCEPT

The basis of the Line Card/PABX controller design utilises the time slot switching capabilities of the SLAC (MV3010-1). Each SLAC can transmit/receive PCM data in 32 (64 in expanded mode of operation) time slots, which can appear on either of two transmit ports and may be input at either of two receive ports, A and B. This gives a maximum capacity of 128 time slots, each associated with one SLAC (i.e. telephone).

Operation of the controller simply allows the serial control information of the SLACs to be generated by a microprocessor. This processor provides all the necessary intelligence to control call routing, off hook status, gain variations etc in software. Communication with the controller is via the microprocessor interface, designed to suit an industry standard processor, such as the Intel 8051.

CIRCUIT DESCRIPTION (Refer to Fig. 1)

Microprocessor Interface

This allows control data to be written to and read from the controller. In addition the Control Address data is written to the device, which is then used to control either up to 8 SLACs directly or one of up to 128 SLACs at an individual address.

Control Data or Control Address is written under the determination of the A0 input. If A0 = 0, then the data byte from the microprocessor is designated as Control Address. This is then loaded into an eight bit latch on the rising (+ve) edge of the $\overline{WR}$ input. If A0 = 1, then the data byte is designated Control Data. This is loaded into the '299 shift register by a positive edge of the 2M clock during the $\overline{WR}$ = 0 period (see timing diagram, Fig. 2).

It is necessary to ensure that the $\overline{WR}$ pulse is long enough (> 500ns) for a 2M rising edge to occur. This limits the 8051 to 10MHz operation. This data will then be sent to the SLACs, as determined by the $\overline{CAM}$ input, when the $\overline{WR}$ input returns to a logic 1. Note that control data must not be written again to the controller during the next 8µs in order to avoid corruption of the previous data byte.

In order to read Control Data from a SLAC, the following considerations must be observed. First, note that the SLAC outputs data following a relevant Control Data word in. Each data byte that is to follow is then clocked out of the SLACs DIO pin during subsequent SLAC $\overline{CS}$=0 (active) periods.

Due to the I/O structure of the SLAC control interface, the output data of the controller must be all ones at these times. This ensures that the controller does not output data that will corrupt the SLAC output data (open collector output). The microprocessor must therefore write FFH during the referred to $\overline{CS}$ active periods.

Secondly, note that only one data byte out will be held by the controller (in the '299) at any one time. This means that the microprocessor must read from the controller after each successive write of FFH, thus forming an organised sequence. This will ensure that no data is lost. Since it is only possible to read from one SLAC at a time (see also Control Address Outputs), then a suitable operational procedure would be as follows:

(a) Write Control Address
(b) Write Control Data
(c) Write FFH
(d) Read first Data byte
(e) Write FFH
(f) Read second Data byte
(g) Repeat FFH/Read as necessary until all data has been output.

When the $\overline{RD}$ input=0, the '299 I/O pins are configured as outputs and shift register data is available at the µD0-µD7 pins.

The $\overline{CS}$ input disables the microprocessor interface when this pin is at logic 1. For normal operation as described, this pin should be held at logic 0.

Output Port

This provides the three connections normally associated with the serial control of a single SLAC. That is specifically Control Data Input/Out (CDIO) providing input/output for the SLAC, Control Pin Address ($\overline{CPA}$) providing SLAC $\overline{CS}$ and Control Clock (CCO) Output providing the DCLK input.

The CDIO and $\overline{CPA}$ pins become active only after a Control Data byte has been written from the microprocessor (i.e. A0=1). Following the $\overline{WR} \rightarrow 1$ transition, the '169 counter counts down through a controlled sequence. This counter provides the $\overline{CPA}$ output directly, and also instructs the '299 register to shift right, providing a CDO output as shown in the timing diagram of Fig. 2.

To obtain acceptance of the CDIO data from the SLAC, it is first retimed to the 2MB clock. CDIO data is then loaded into the '299 register as the CDO data (all ones) is clocked out. When the once off sequence stops, SLAC output data is held in the register ready to be read by the microprocessor (see also Microprocessor Interface).

Control Address Outputs & Mode Input

Control Address data from the microprocessor is held in the '574 latch. The outputs of this device can be used in two ways, depending on the $\overline{CAM}$ input.

If the $\overline{CAM}$ input = 1, then the $\overline{CPA}$ signal will strobe the

CA0-7 outputs during the SLAC Control Data load sequence (see section Output Port). If the pins CA0-7 have pull-up resistors to +5V connected, then those outputs that have a 0 loaded into the latch will go low as $\overline{CPA}$. Thus, if one SLAC $\overline{CS}$ input is connected to each control address output (Fig. 3), control data is sent to each of the 8 SLACs that has a $\overline{CS}$ low as previously described. This mode can be used when reading data from the SLACs, only if one of CA0-7=0.

Alternatively, if $\overline{CAM}$=0, then the '574 outputs are permanently enabled. The 8-bit output byte can now be decoded as an individual SLAC address. This mode can be used to write/read data to/from a single SLAC only, of which up to 128 in a PABX are permissible.

Note that in both modes, the CDIO and CCO outputs are common to all SLACs.

SYSTEMS APPLICATIONS

Line Card Controller

The configuration of controller and SLACs to form a line card is shown in Fig. 3. Each $\overline{CS}$ input of a SLAC is driven by one of the CA0-7 outputs. For this application the $\overline{CAM}$ (mode input, Figure 1) = 1 mode is used.

When initialising, or sending common commands to the SLACs, a Control Address value of 00H can be written to the '574 latch. When the Control Data is written, then all 8 SLACs are loaded with this data.

If the writing of a Control Data word will cause a SLAC control data output, or a single SLAC is to be written to, the Control Address word must contain only one 0 (such as FEH, BFH etc). This ensures that only one SLAC will output data at a time.

PABX Application

The interconnection of controller and SLACs to form a simple PABX is shown in Fig.4. In this application, the SLACs are organised in 16 blocks of 8 (a line card), each block selected by a one-of-sixteen decoder (Line Card Address). This decoder (e.g. a 74 series '154 or two '138s) acts on the next four most significant bits of CA7-0, that define the Line Card Address (i.e.CA6-3). Each output of the '154 enables a one-of-eight decoder, associated with each block of 8 SLACs. All sixteen of these 1-of-8 decoders (eg '138) act on the three least significant bits of CA7-0, that define a SLAC Address. The second enable input of each '138 ($\overline{G2B}$) is driven by $\overline{CPA}$ so that the finally decoded output is enabled as $\overline{CPA}$. Then, since the first enable input ($\overline{G2A}$) of each '138 is enabled exclusively by the '154, only one SLAC can have an active $\overline{CS}$ input at any one time. This SLAC is defined by the Line Card Address, CA6-3, and SLAC Address, CA2-0.

Control Data to and from each SLAC is achieved on an individual basis. The address of the required SLAC is sent (written) first to the controller (A0=0). With A0= 1 writes/reads via the microprocessor interface are concerned with this SLAC only.

PABX Application with Multiple Control

To speed up operation of control when using 128 SLACs, more than one controller can be used. In this case each controller works in $\overline{CAM}$=1 mode controlling 8 SLACs. This then requires a total of 16 controllers.

Improved operation is obtained by writing Control Address 00H to all controllers for subsequent loading of Control Data to all 128 SLACs simultaneously. For successful capture of Control Data from the SLACs the Control Address of every controller is next loaded with an address value containing only one 0 (such as DFH). This ensures only one SLAC sends data to each controller at this time. Each controller can then be read individually (addressed) by the processor. To obtain Control Data from the other SLACs, a different Control Address, containing one 0, is used in the same manner just described. Control Data can thus be obtained from each SLAC by using all of the 8-possible CA0-7 combinations that contain one 0.

Finally, note that when writing Control Data to a common number of SLACs (not all 128), then using differing combinations of Control Address in each controller can load subsequent data to any number of SLACs in any combination. Similarly, by using different combinations of CA0-7 (with one or no 0) in each controller, then up to 16 SLACs in any combination of one per controller can send Control Data to their respective controller.

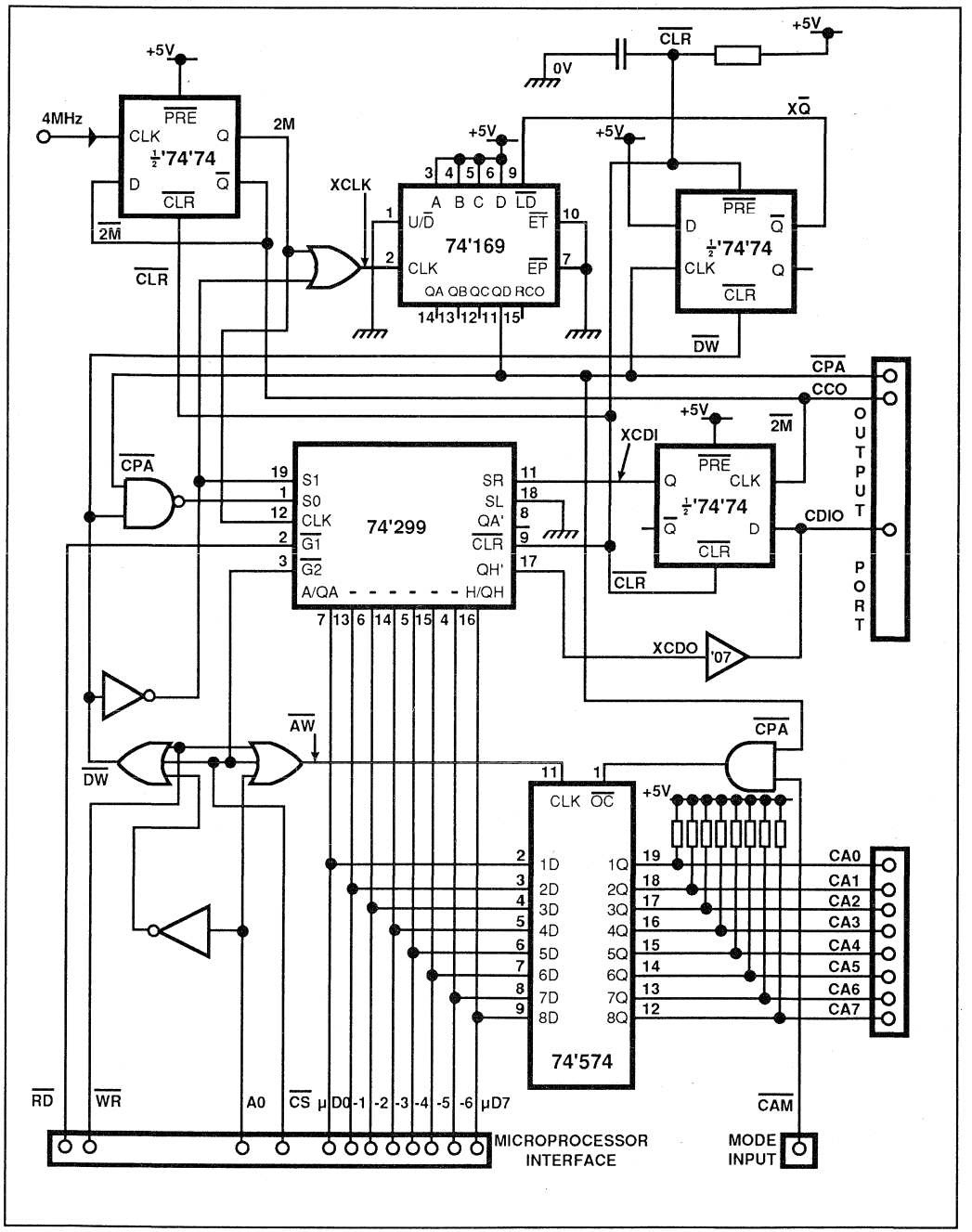


Fig. 1 Line Card Controller logic diagram

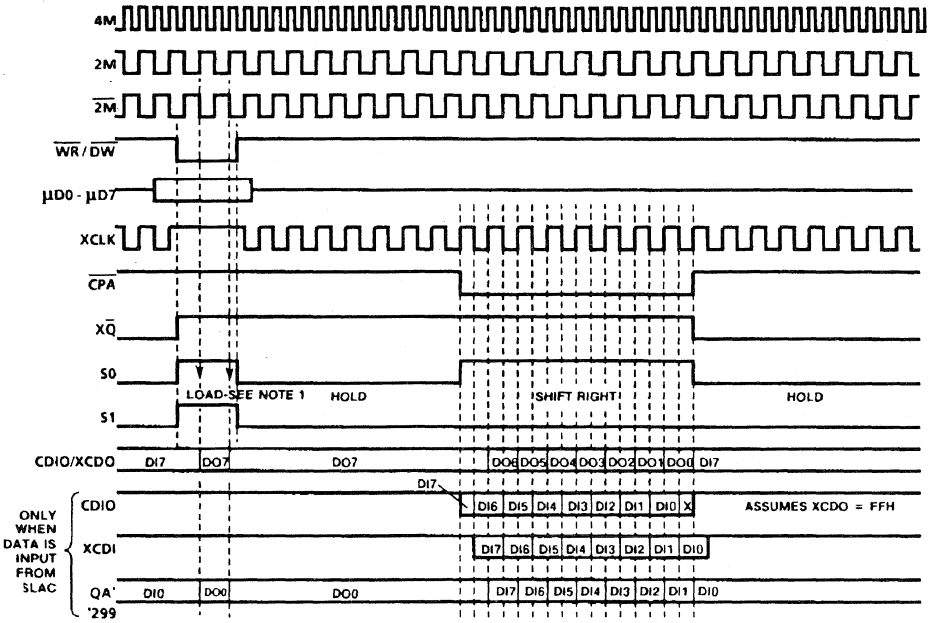


Fig.2a Control Data sequence. Note 1: $\overline{WR}$ low period must be > 500ns - see text

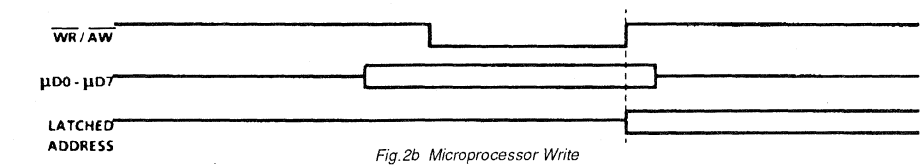


Fig.2b Microprocessor Write

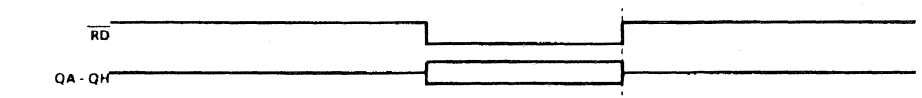


Fig.2c Micropressor Read; A0 = X, $\overline{CS}$ = 0, $\overline{WR}$ = 1

Fig.2 Timing diagrams

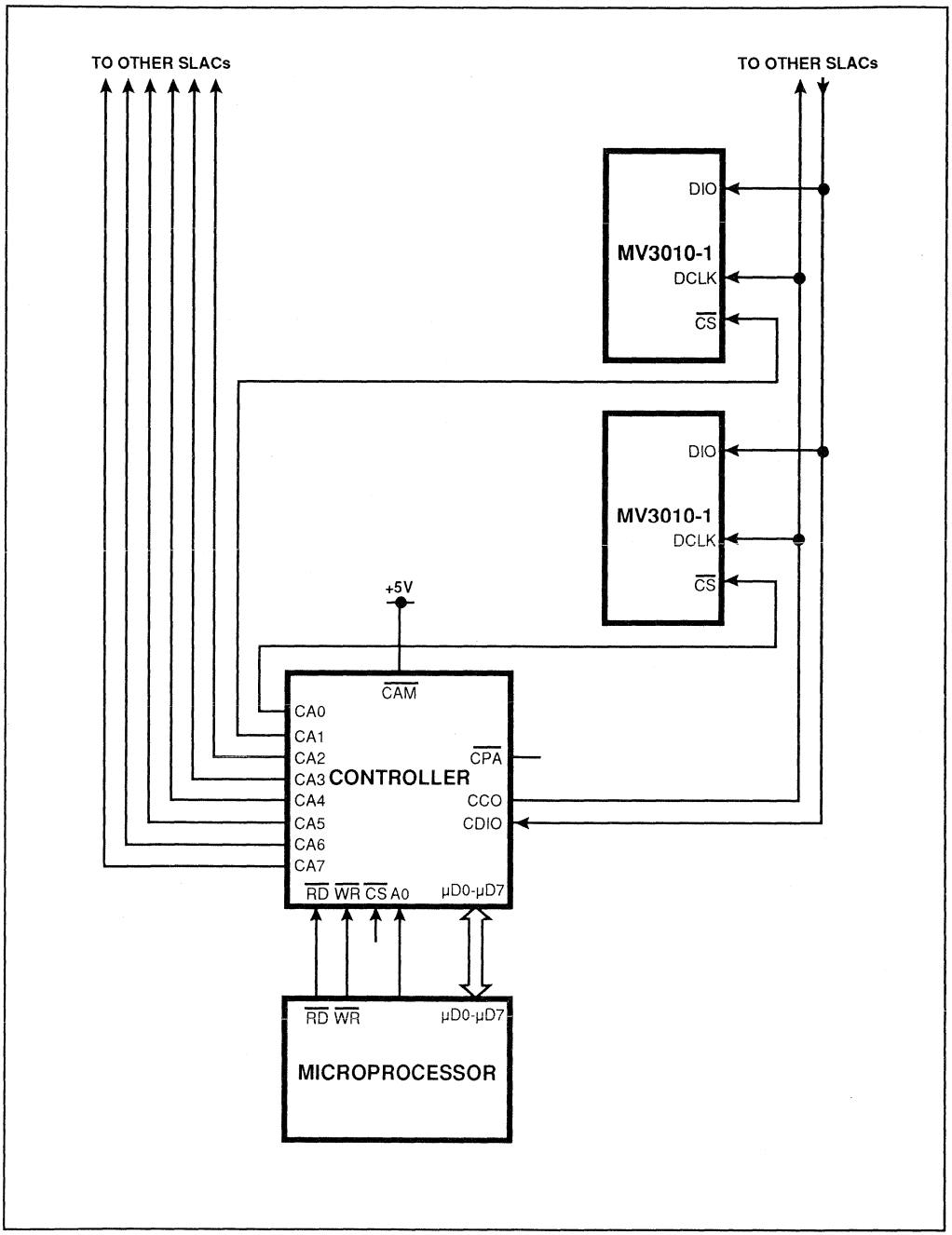


Fig.3 $\overline{CAM}$ = 1 Mode, Line Card application

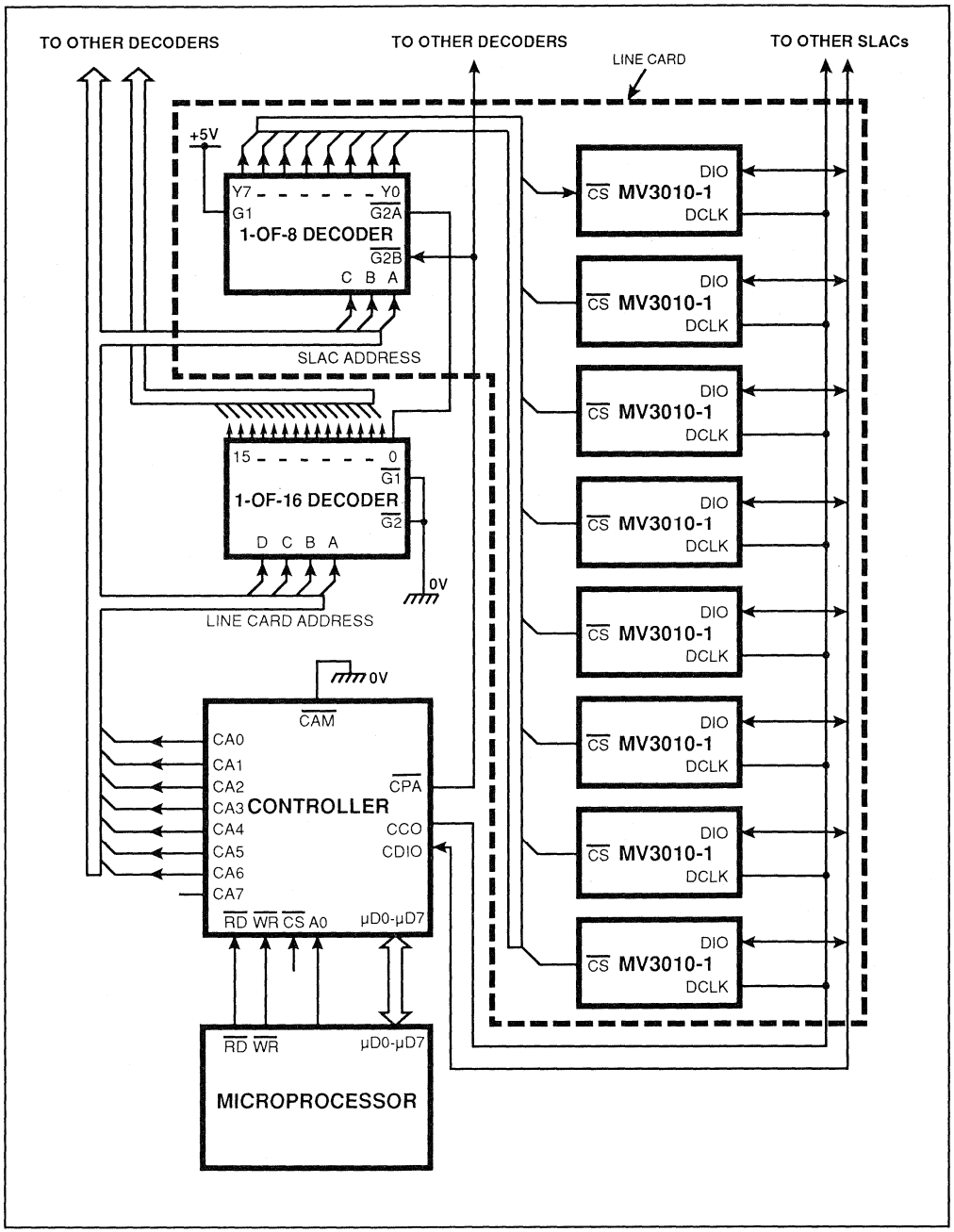


Fig.4 $\overline{CAM}$ = 0 Mode, PABX application

MV3010-1 Evaluation Package

This Application Note describes the PCBAN111 evaluation package for the MV3010-1 Subscriber Line Audio Circuit (SLAC). The package contains both hardware and supporting software for use with IBM PCs or compatibles.

Hardware for the evaluation package consists of a circuit board containing two MV3010-1 devices with full and flexible access to analog and digital ports of both devices. The board has been so designed to operate without any external control facility (Stand Alone option) or by utilising the additional on-board logic it can be interfaced to an IBM PC or compatible. In the latter case, the software of the evaluation package can be used to fully control/monitor all programmable features of both MV3010-1s on the circuit board. These features are displayed on a single screen format, one for each MV3010-1, with additional menu driven screens for access to features of the software.

Since the circuit board was designed with access to the MV3010-1's PCM ports, the software provides additional features other than control capability. This allows automated preprogramming of C Filter coefficients (using the method as described in Application Note AN84-2) and measurement/plotting of Echo Return Loss (ERL) performance. Note, however, that since these features require real time transfer of PCM data, this will only be possible with medium-to-high end performance PCs. Note also that running under a multitasking environment such as windows, will degrade the real time transfer rate and may prevent successful PCM data transfer.

HARDWARE DESCRIPTION

The hardware of the evaluation package is a circuit board which contains two SLAC devices with associated discrete components and a number of LSTTL devices to buffer the PC interface. Figure 2 shows the circuit schematic with figure 3 showing the PCB layout of the board. The design of the circuit board is such that terminal block connectors TB5, TB6 and TB7 together with uncommitted BNC connectors BNC5-BNC9 can be custom wired for interface to a test system. Thus it is possible to use the board in a Stand Alone mode of operation, or if rewired, to interface to a PC (PC Control modes) depending on the connections at the PCCONN socket. Additionally, the board provides on-board clocking (IC3 & IC4) or again by rewiring at TB5-TB7, it can be used with external clocks. This flexibility results in five possible modes of operation which will be described later.

An external +5V power supply is required for connection to the AV_{CC} and DV_{CC} supplies of the board, which should be independently connected. Note that the two PCM ports of each SLAC are connected in a cross coupled arrangement such that (unless combined at TB5-TB7) two separate analog-digital-analog paths are formed from one SLAC to the other. Simple A/D and D/A measurements are possible utilising only one SLAC with PCM ports available at TB5-TB7.

All of the SLAC analog ports connect via associated discrete components to dedicated BNC sockets on the board, in addition to being available at TB1 and TB3. Thus, TB1 is the analog interface to SLAC1 and TB3 is the Analog interface for SLAC2. Resistors R2 and R12 provide DC connection to ground for VIN of SLAC1 and SLAC2 respectively. The value of each termination can be user defined by additional resistors R1 and R13. Both the VOUT pins of the SLACs are AC coupled to the output ports (C2 and C18) to provide necessary DC blocking. This allows direct AOUT→ AIN connections on the board. Note that if an AOUT port is driving a high impedance, then it may take some time for the DC conditions to settle.

A list of all components on the circuit board is given in Table 1, whilst Tables 2, 3 and 4 show connection listings for terminal blocks TB1-7, BNC1-9 and the PCCONN socket respectively.

HARDWARE OPERATING MODES

Listed below are the five possible configurations of the hardware to give the operating modes as described.

STAND ALONE MODE - ON-BOARD CLOCKS

This mode is selected by inserting a 24 pin DIL header in the PCCONN socket. It should be wired as shown in Fig. 4. With this in place, then Active and Standby modes of each SLAC are controlled by S1 for SLAC1 and S2 for SLAC2 (S1/S2 closed sets Standby, S1/S2 open sets Active). On-board clocking is utilised by connecting the following terminal block pins together:-

TB5p2 = TB5p3 = TB5p4
TB7p2 = TB6p4 = TB6p5 = TB6p6

which gives 8k = FS1 = FS2
and 2M = MCLK = CLK2 = CLK1

STAND ALONE MODE - EXTERNAL CLOCKS

Stand alone operation is again used by inserting a header at PCCONN wired as Fig. 4. External clocking can be connected to the terminal block pins and should meet the static and dynamic requirements as given in the device data sheet.

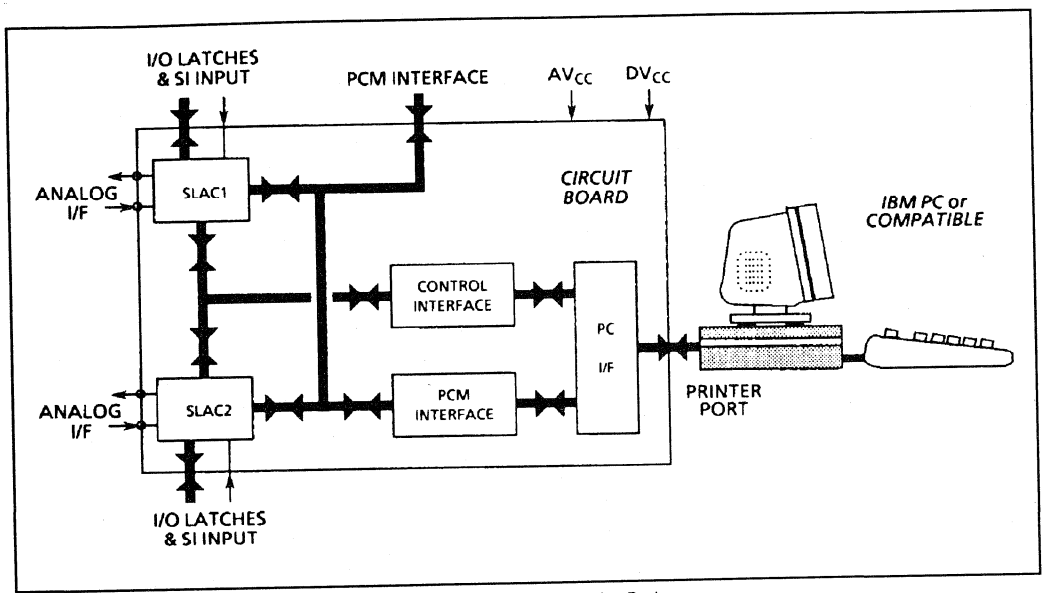


Fig.1 Block Diagram of Evaluation Package

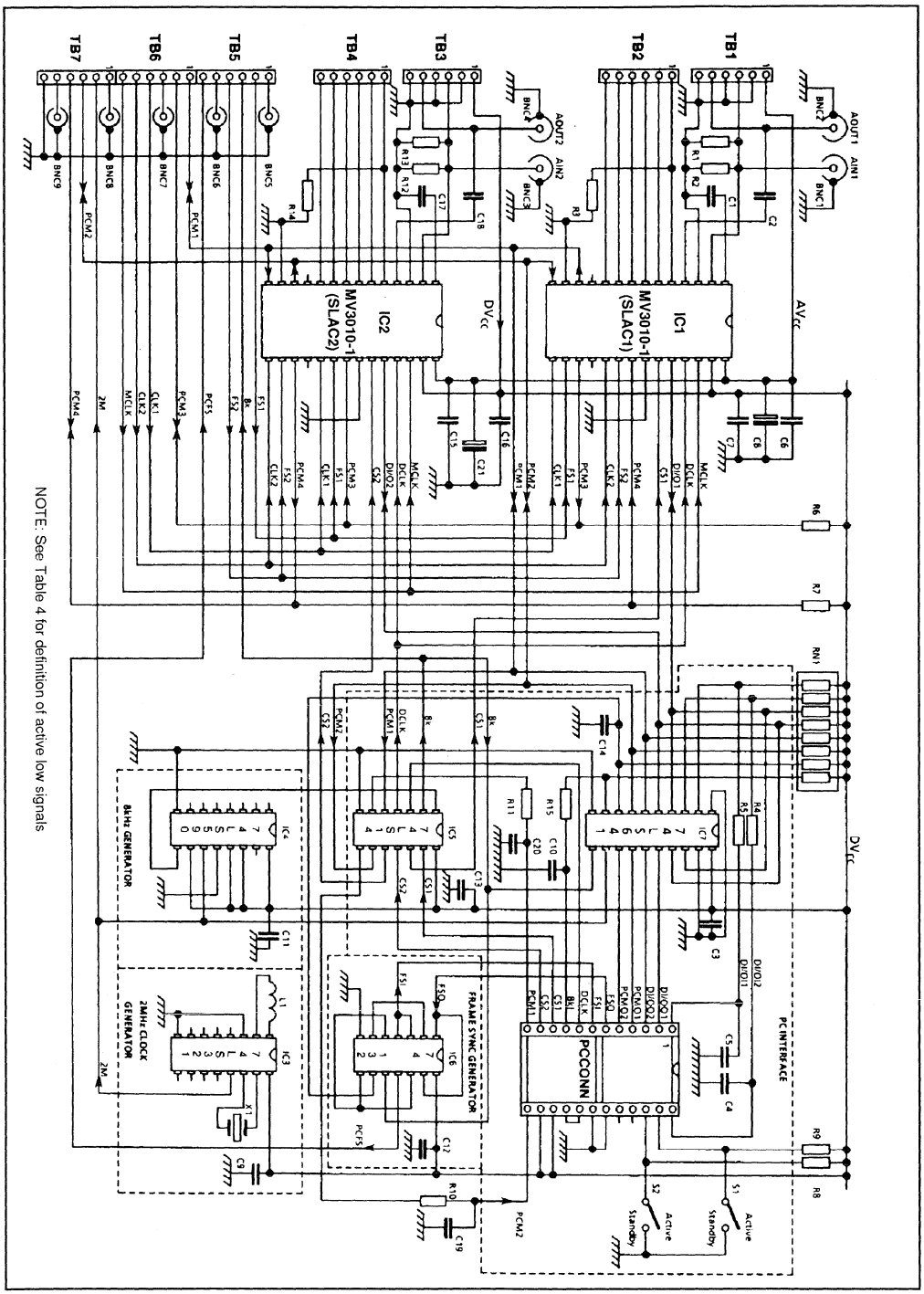


Fig.2 Circuit board schematic

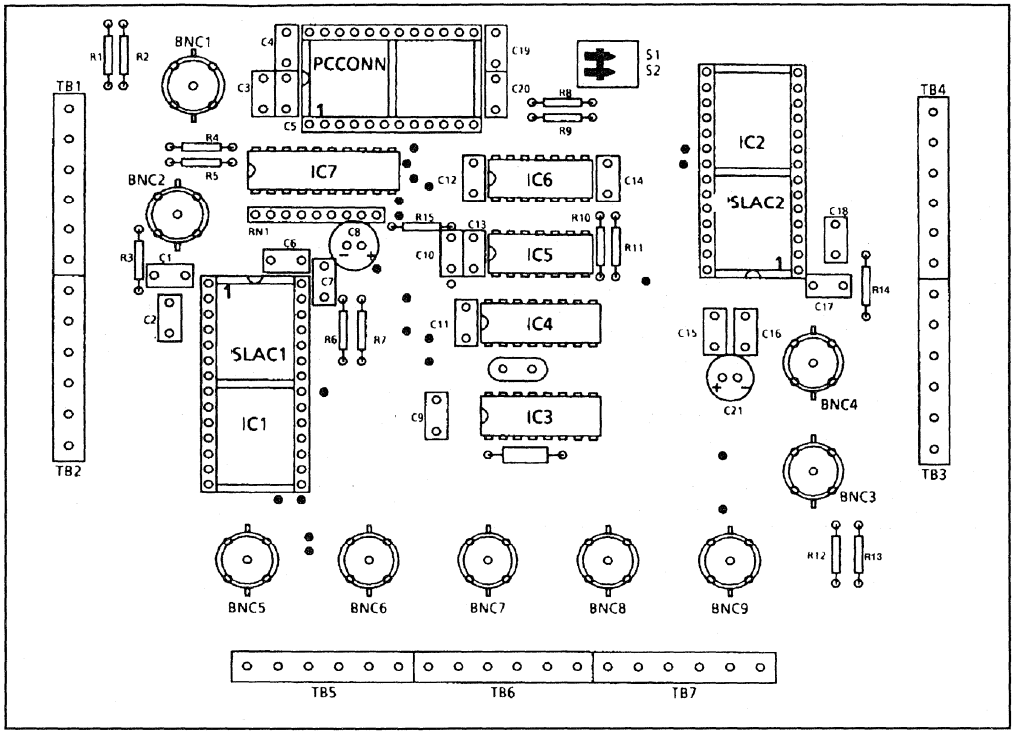


Fig. 3 Circuit board component layout

Name	Value	Name	Value	Name	Value
IC1	MV3010-1	RN1	8 x 10kΩ	X1	4096kHz Crystal
IC2	MV3010-1	C1	100nF	L1	330µH Inductor
IC3	74LS321	C2	3.3µF	S1	s.p.s.t Switch
IC4	74LS590	C3	100nF	S2	s.p.s.t Switch
IC5	74LS14	C4	Not fitted	PCC	24 WAY DIL
IC6	74132	C5	Not fitted	TB1	
IC7	74LS641	C6	100nF	TB2	Pluggable
R1	Termination AIN1	C7	1µF	TB3	6 Way 0.2"
R2	10kΩ	C8	10µF	TB4	Connectors
R3	10kΩ	C9	100µF	TB5	(see Table 2)
R4	27Ω	C10	Not fitted	TB6	
R5	27Ω	C11	100nF	TB7	
R6	10kΩ	C12	100nF	BNC1	PCB BNC Socket
R7	10kΩ	C13	100nF	BNC2	PCB BNC Socket
R8	10kΩ	C14	33pF	BNC3	PCB BNC Socket
R9	10kΩ	C15	100nF	BNC4	PCB BNC Socket
R10	27Ω	C16	1µF	BNC5	PCB BNC Socket
R11	27Ω	C17	100nF	BNC6	PCB BNC Socket
R12	10kΩ	C18	3.3µF	BNC7	PCB BNC Socket
R13	Termination AIN2	C19	Not fitted	BNC8	PCB BNC Socket
R14	10kΩ	C20	Not fitted	BNC9	PCB BNC Socket
R15	27Ω	C21	10µF		

Table 1 Circuit board component listing

BLOCK NUMBER	Pin number					
	1	2	3	4	5	6
TB1	AV_{CC} INPUT	0V	AIN1, ANALOG INPUT TO SLAC1	0V	AOUT1, ANALOG OUTPUT FROM SLAC1	0V
TB2	SI INPUT SLAC1	CP1 I/O LATCH SLAC1	CP2 I/O LATCH SLAC1	CP3 I/O LATCH SLAC1	CP4 I/O LATCH SLAC1	CP5 I/O LATCH SLAC1
TB3	DV_{CC} INPUT	0V	AIN2, ANALOG INPUT TO SLAC2	0V	AOUT2, ANALOG OUTPUT FROM SLAC2	0V
TB4	SI INPUT SLAC2	CP1 I/O LATCH SLAC2	CP2 I/O LATCH SLAC2	CP3 I/O LATCH SLAC2	CP4 I/O LATCH SLAC2	CP5 I/O LATCH SLAC2
TB5	BNC5 I/O U/C SOCKET	FS1 INPUT SLAC1 to SLAC2 PCM	8k 8kHz OUTPUT	FS2 INPUT SLAC2 to SLAC1 PCM	BNC6 I/O U/C SOCKET	PCFS OUTPUT
TB6	PCM1 DXA SLAC1 to DRA SLAC2	PCM3 DXB SLAC1 to DRB SLAC2	BNC7 I/O U/C SOCKET	CLK1 SLAC1 to SLAC2 PCM	CLK2 SLAC2 to SLAC1 PCM	MCLK SLAC1 and SLAC2
TB7	BNC8 I/O U/C SOCKET	2M 2MHz O/P INTERNAL CLOCK	PCM2 DXA SLAC2 to DRA SLAC 1	PCM4 DXB SLAC2 to SLAC1	BNC9 I/O U/C SOCKET	0V

Table 2 Terminal Blocks TB1..TB7 connection listing

BNC1 = AIN1	BNC4 = AOUT2	BNC7 = UNCOMMITTED
BNC2 = AOUT1	BNC5 = UNCOMMITTED	BNC8 = UNCOMMITTED
BNC3 = AIN2	BNC6 = UNCOMMITTED	BNC9 = UNCOMMITTED

Table 3 BNC Sockets BNC1..BNC9 connection listing

Pin Number	Name	Description	Pin Number	Name	Description
1	DI/OI1	DI/O Output from SLAC1	24	DI/OI2	DI/O Output from SLAC2
2	DI/OO1	DI/O Input to SLAC1	23	S1	Output SWITCH1 Status
3	DI/OO2	DI/O Input to SLAC2	22	S2	Output SWITCH2 Status
4	PCMO1	Input to PCM1 Bus	21	N/C	No connection
5	PCMO2	Input to PCM 2 Bus	20	N/C	No connection
6	FSO	Frame Sync Input from PC	19	0V	Ground
7	FSI	Frame Sync Output to PC	18	0V	Ground
8	$\overline{DCLK}$	Inverse of DCLK from PC	17	16	Internally connects to pin 16
9	8kI	Internal 8kHz Output to PC	16	17	Internally connects to pin 17
10	$\overline{CS1}$	$\overline{CS}$ Input to SLAC1 from PC	15	+5V	DV_{CC} Supply Output
11	$\overline{CS2}$	$\overline{CS}$ Input to SLAC2 from PC	14	+5V	DV_{CC} Supply Output
12	$\overline{PCM1}$	Inverse of PCM1 Output to PC	13	$\overline{PCM2}$	Inverse of PCM2 Output to PC

Table 4 PCCONN connection listing.

TB5p2 = FS1 = 8kHz
TB5p4 = FS2 = 8kHz
TB6p6 = MCLK = 2048kHz
TB6p4 = CLK1 = 64-4096kHz
TB6p5 = CLK2 = 64-4096kHz

PC CONTROL MODE - ON-BOARD CLOCKS

For this mode, the circuit board is connected to a PC parallel printer port via the PCCONN socket with connections made as given in figure 5 (a ready made cable is supplied with the evaluation package). On-board clocks are selected by using the same interconnect tor TB5-TB7 as the Stand alone case, ie.:-

TB5p2 = TB5p3 = TB5p4
TB7p2 = TB6p4 = TB6p5 = TB6p6

which gives 8k = FS1 = FS2
and 2M = MCLK = CLK2 = CLK1

Control of each SLAC is now achieved via the supporting software package, as described later. Note that this mode does not support software features that require use of PC generated clocks (auto preprogramming and ERL plots), this mode being described later.

PC CONTROL MODE - EXTERNAL CLOCKS

Keeping the same connections between PCCONN and PC printer port as for on-board clocks, external clocking can be used instead by changing the terminal block connections. These then become the same as for the Stand alone case, ie.:-

TB5p2 = FS1 = 8kHz
TB5p4 = FS2 = 8kHz
TB6p6 = MCLK = 2048kHz
TB6p4 = CLK1 = 64-4096kHz
TB6p5 = CLK2 = 64-4096kHz

again meeting all static and dynamic timing requirements. In order to obtain optimum results for transmission performance measurements, on-board clocking should be disabled. This can be affected by removing IC3 (74LS321) and IC4 (74LS590) from the board. Control of each SLAC is now achieved via the supporting software package, and again, this mode does not support software features that require use of PC generated clocks.

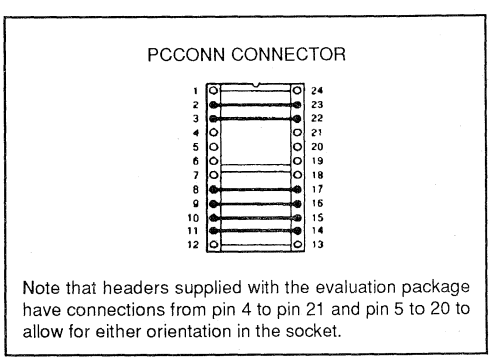


Fig. 4 PCCONN Stand Alone Modes connections.

PC CONTROL MODE - PC GENERATED CLOCKS

To obtain all of the features of the supporting software the circuit board should be wired for this mode. Again the PCCONN is connected as in Fig. 5. The necessary clocking is obtained by wiring the terminal blocks as follows :-

TB5p2 = TB5p3 = TB5p4
TB7p2 = TB6p6
TB5p6 = TB6p4 = TB6p5

which gives 8k = FS1 = FS2
2M = MCLK
and PCFS = CLK1 = CLK2

SOFTWARE DESCRIPTION

The software is normally supplied on a floppy disk as an executable file which is written in Turbo Pascal. All displays and menus use the standard textual display format, thus allowing the software to run on any IBM PC/compatible machine. Part of the program caters for display of frequency response measurements for which a graphics card in the PC will be required. Note that the PC must also have a standard parallel printer port to allow connection to the circuit board, as described in the Hardware Description section. With the circuit board wired for one of the PC control modes, the program can now be run.

RUNNING THE PROGRAM

If the program is to be run from the floppy disk, then the command SCAMP is simply entered at the keyboard. However, the program may be copied into a working directory of the PC and run from hard disk, by carrying out appropriate procedures tor the PC used. With the program running, operations are mainly menu driven via the PC Function Keys F1-F10 or accessed under cursor control. The menus available are denoted the CONFIGURATION MENU and the MAIN MENU, described later. From the MAIN MENU, access is provided to two SETUP SCREENS (one per SLAC) to allow control of programmable parameters. The SETUP SCREENS also provide a HELP screen which lists available Function Key options. Fig. 6 shows a basic flow chart for the SCAMP software.

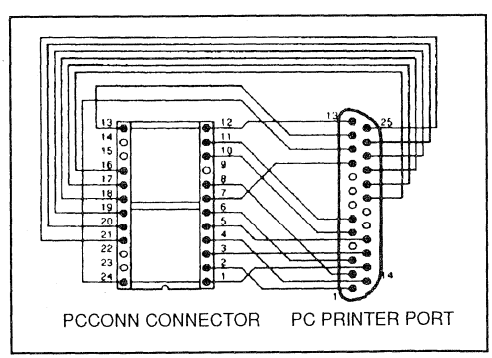


Fig. 5 PCCONN PC Control Modes connections

The CONFIGURATION MENU is used to reconfigure the PC as required and allow a number of checks on the PC and the hardware connected to the printer port. In contrast, the MAIN MENU runs measurement routines on the selected SLAC and allows access to the two SETUP SCREENS. The following sections now describe the functions within each screen format in more detail.

THE CONFIGURATION MENU

After entering the command SCAMP, one of two options occur. If the program is being run for the first time, then a file called SLAC.CON will be created. This contains data on the default printer port, graphics card set up, hardware (circuit board) status and file location. This file is simply read if the program was run previously.

In creating the SLAC.CON file, the program prompts for entry of a default printer port (i.e. where cable is connected), carries out a check on the existence of that port and if successful, checks the status of the connected hardware via further prompts. These automatically check that command data can be written to and read from each SLAC on the circuit board (as described for the F5 key of this menu) and then tests PCM transmission capability (as F6 key). After completing these checks, the CONFIGURATION MENU is displayed.

The menu itself has eight associated functions attached to keys F2 and F4-F10. These are listed below along with a brief description of available options :-

F2 KEY : This is used to change the PC printer port used to interface to the circuit board. Three ports numbered 1, 2 or 3 may be selected.

F4 KEY : Changes the hardware status between Disconnected and Connected status. If the status is set to Connected, then appropriate hardware checks will be rerun.

F5 KEY : This key reruns the control hardware status check routine when pressed.

F6 KEY : This reruns the PCM hardware check routine which will fail if the transmit and/or receive PCM verification fail.

F7 KEY : The SLAC analog ports are tested by this routine, which requires that AIN=AOUT for both SLACs on the circuit board.

F8 KEY : Toggling through the available graphics card options occurs when pressing this key. Most graphics card types can be automatically detected when set for AUTO (default option), but two types will not be. These are the IBM8514 and ATT400 which can be set explicitly with the remaining two options.

F9 KEY : Toggling to TRUE sets a monochrome mode for text displays (which may be clearer if a monochrome monitor is used with a colour interface card) and sets a higher resolution monochrome mode with low colour resolution graphics card.

F10 KEY: Pressing this key will exit the CONFIGURATION MENU and enter into the MAIN MENU.

THE MAIN MENU

This menu provides control of the SLAC devices on the circuit board. Again, the PC function keys are used to invoke the available routines. These keys allow access to the SETUP SCREENS for control of SLAC programmable parameters (described in separate section), run routines for automatic preprogramming of target SLAC C Filter and plotting of ERL response. A listing of valid function key depressions and associated actions for that key are given on the following page (note that * refers to a string of alpha characters).

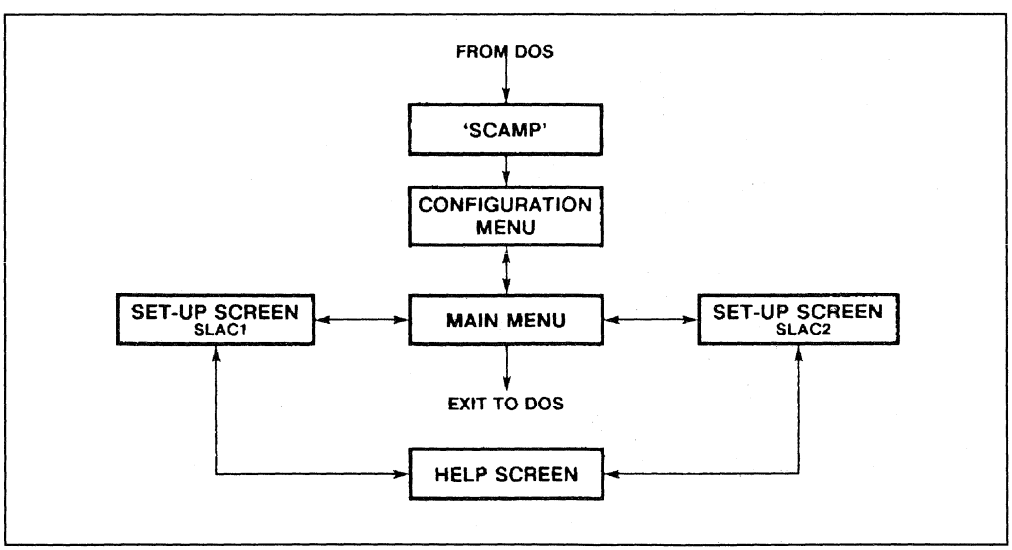


Fig.6 Basic flow chart for SCAMP software.

F2 KEY : This key returns to the CONFIGURATION MENU.

F3 KEY : Access to the two SETUP SCREENS, one screen per SLAC of the circuit board, is provided by calling up a filename in the format *.SET. Such files contain the status of both SLACs. If the file is found, then the SETUP SCREENS are entered, else a File Not Found routine occurs and exits back to the MAIN MENU. When running the program for the first time, no setup files will exist such that the F4 key should be used (see later).

F4 KEY : A file "LASTAUTO.SET" is used to enter the SETUP SCREENS. This contains the last used setup data and will be rewritten every time the user exits the SETUP SCREENS. Note that user specific setup files may be created when in the SETUP SCREENS (see later section) in addition to this automatically maintained file. If the program is being run for the first time, then no "LASTAUTO.SET" file will exist, so the program creates one using default parameters when entering the SETUP SCREENS.

F5 KEY : This routine provides automatic preprogramming of the SLAC adaptive C Filter, and as such requires PCM transmission to be verified (see Configuration Menu F6 Key). Note that only SLAC1 can be used with this routine such that the target Line Interface should be connected between AOUT1 and AIN1. After prompting for a filename of format *.TBL, measurements of spot frequency response (as described in Applications Note AN84-2) are taken and the results stored in this file. Note that the program uses a temporary *.SET file for SLAC1 status, setting SLAC2 to DXB to avoid contention with PC generated PCM. Using the same filename as for *.TBL, new files will be created in the form *.DAT and *.SET by entering the pre-programming calculation routine as described for the F6 key, before returning to the MAIN MENU .

F6 KEY : After prompting for a *.TBL file, the program now carries out a preprogramming calculation for the C Filter coefficients. This generates a set of preprogramming coefficients which are written to an extended version of the input *.TBL file and to a new *.SET file. The new *.SET file contains setup data so that both SLACs will be programmed into appropriate modes to allow frequency response measurements to be made when using the F7 key on the MAIN MENU.

The time to reach a solution to the preprogramming calculation varies according to the nature of the Echo Response to be matched (i.e. AOUT→AIN). If this proves to take too long, or for any other reason, then key F10 provides an abort option to return to the MAIN MENU.

F7 KEY : The program prompts for a *.SET file which would normally have been generated via the F6 key. The setup data in the file allows frequency response measurements to be taken (i.e. SLAC2 to DXB) with the C Filter of SLAC1 both disabled and enabled (with preprogrammed calculated coefficients). Measurements are of Echo Return Loss (ERL) from DRA to DXA and assume the target line interface is connected between AOUT1 and AIN1.

The frequencies used for ERL are between 200 and 3500 Hz at a user definable number of points in this range (default=20). A prompt is made to allow this to be changed. All results at each frequency are written to a text file called *.FRQ.

After the *.FRQ file has been created, the program allows for entry into the frequency response plot routine (using this file) as described for key F8, provided that a graphics card is present in the PC.

F8 KEY : This allows for on screen plotting of data from the user entered *.FRQ file, provided that a graphics card is present in the PC (the CONFIGURATION MENU is used to set the graphics card options). The display shows both sets of results for disabled and enabled C Filter with preprogrammed calculated coefficients.

If a print of the frequency response is required, then note that normally the PC's Print Screen Key (PRS) is disabled while SCAMP is running. However, if the hardware connected status is set to "Disconnected" (F4 key CONFIGURATION MENU) then PRS is enabled while the plots are displayed. As this is a graphics mode display, suitable software to modify the action of PRS for the Printer being used, must have been installed prior to running SCAMP.

SETUP SCREENS

This section describes the use of the SETUP SCREENS which will have been entered via the MAIN MENU (F3/F4 KEY). These screens contain all of the programmable parameters which determine the status of both SLACs on the circuit board, one screen per SLAC. When entering the SETUP SCREENS, both SLACs will be set to the status contained in the *.SET file used. Each screen also shows the SLAC with which it is associated and the format for both is now described.

Fig. 7 shows the format of the SETUP SCREENS, which now include a cursor. This is moved to any one of a number of Parameter Fields using the cursor control keys. These fields occur to the right of each parameter that is displayed on the screen, the available options for each being described in a later section. Such options may be typed manually or selected using function keys F2, F3 and F4. Remaining function keys provide additional features of the SETUP SCREENS as now described on the next page.

Key Options (< S > = SHIFT KEY, < C > = CONTROL KEY)

→ : Moves the cursor to the first character of the next parameter field to the right and initiates transfer of data, as written for the current selection, to the identified SLAC.

← : Acts as Right Cursor except that cursor moves to the left.

↑ : Moves the cursor up to the next parameter field and initiates transfer of data, as written for the current selection, to the identified SLAC.

↓ : Acts as up cursor (↑) except that cursor moves down the screen.

< C > → : Moves the cursor one character to the right within the parameter field. If this is the last character, then the cursor moves to the next parameter field to the right and initiates transfer of data, as written for the current selection, to the identified SLAC.

< C > ← : Acts as CONTROL right cursor except that the cursor moves to the left.

F1 KEY : Invokes the HELP screen which lists available options for the SETUP SCREENS.

F2 KEY : This will toggle the Active/Standby (power down) state of the selected SLAC.

<S> F2 : Changes display to the SETUP SCREEN of the other SLAC.

F3 KEY : Each depression of this key causes the currently selected parameter field to decrement one step through the available options.

F4 KEY : Each depression of this key causes the currently selected parameter field to increment one step through the available options.

F5 KEY : Depressing this key resets all parameter fields of the SETUP SCREENS to their default setting.

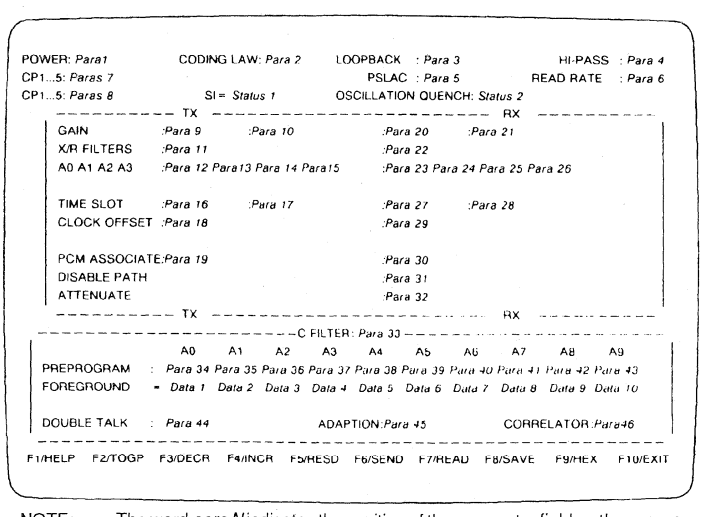
F6 KEY : Each depression of this key causes all of the available programmable parameters of each setup screen to be transmitted to the associated SLAC.

F7 KEY : This will prompt for a *.SET setup file and will alter the SETUP SCREENS to the conditions stored in that file. If the file does not exist, the program returns to the SETUP SCREENS after reporting an error.

F8 KEY : The current status of the SETUP SCREENS will be stored in a file *.SET entered after the prompt.

F9 KEY : Changes the displayed format of all the SLAC filter coefficients (X, R and C Filters) from the normalised (to + 1024) into HEX data bytes. Also changes display of gain setting data from dBs to HEX.

F10 KEY: This is the escape key to return to the MAIN MENU. Note that each time the SETUP SCREENS are exited, then the file LASTAUTO.SET is modified to the current parameter selection.



NOTE: The word *para N* indicates the position of the parameter field on the screen. The available options are given in the text for each parameter number N. Similarily, the words *Status N* and *Data N* are control data that has been read from the SLAC.

Fig. 7 SETUP SCREENS format

Parameter Options

Each programmable parameter field of one setup screen has a number of available options, always associated with the SLAC of the current setup screen. These are listed below where the *Parameter, Status or Data number* refer to the position on the setup screen as shown in Fig. 7. The format of the list uses *Parameter Number*: Parameter Name: Options A/B/-./X: Description.

Para 1: STATUS: ACTIVE/STANDBY: Places the selected SLAC in either its Active or Standby (Power Down) mode.

Para 2: PCM CODING: A-LAW/μ-LAW/LINEAR: Changes the PCM coding scheme of the selected SLAC to the displayed option.

Para 3: LOOPBACK: NONE/ANALOG/DIGITAL: Sets either no loopback or Analog/Digital as displayed.

Para 4: HI-PASS FILTERS: ENABLED/DISABLED: Allows disabling of the selected SLAC Hi-pass filters as shown.

Para 5: SLAC: 1/2: Shows the selected SLAC for each setup screen.

Para 6: READ RATE: 1/2/3/—/255: This relates to the reading of I/O Latches CP1...CP5, reading of the SI pin input level, reading of foreground C Filter coefficients and interrogation of the Oscillation Quench bit. It controls the rate at which data is read from the selected SLAC in one second steps from 1 to 255 seconds.

Para 7: CP1...CP5 I/O STATUS: I/O: The parameter field consists of a row of five alpha characters which can be either I or O. Letter I sets a CPn latch to input mode and letter O sets a CPn latch to output mode. The five letters across the screen associate with CP1, CP2, CP3, CP4 and CP5 in that order setting latch status accordingly.

Para 8: CP1...CP5 LEVEL: 0/1: The parameter field consists of a row of five numeric characters which can be either 1 or 0. Number 0 implies a low logic level and number 1 implies a high logic level. The five numbers across the screen associate with CP1, CP2, CP3, CP4 and CP5 in that order. If the latch status is input, then this implies a detected logic level and if the latch status is output, then this implies an output condition. The rate at which CPn pins are read from is set by the READ RATE parameter.

Status 1: SI LEVEL: 0/1: The character is 0 or 1 depending on whether the SI pin voltage is at logic low or logic high. The rate at which the pin is read is determined by the READ RATE parameter.

Status 2: OSCILLATION QUENCH: YES/NO: This shows whether the Oscillation Quench bit has been set in accordance with the C Filter operation, as described in the SLAC Data Sheet. The status is read at intervals as set by the READ RATE parameter. If the status becomes set to YES, then this will remain so until reset to NO by the user.

Para 9: TRANSMIT GAIN: 'VALUE': Sets the Transmit Gain stage of the selected SLAC to the value of the gain as indicated. 'Value' may be entered in dB or HEX depending on the displayed format as set by the F9 Key.

Para 10: TRANSMIT GAIN: NORMAL/INVERSE: Sets the Transmit Gain stage of the selected SLAC to Normal (0° phase shift) or Inverse (180° phase shift) as indicated.

Para 11: TRANSMIT FILTER: DISABLED/ENABLED: This is used to disable or enable the selected SLAC Transmit Filter, as indicated.

Para 12, Para 13, Para 14 Para 15: A0, A1, A2, A3: 'VALUE', 'VALUE', 'VALUE', VALUE': Four numbers in the range -2048 to +2047 (in integer steps) set the values of the four Transmit Filter coefficients (refer to Data Sheet for format description). Note that coefficients are normally in the range ±2 but are normalised to 1024 for convenience, and may alternatively be displayed in HEX format using the F9 Key of the SETUP SCREENS.

Para 16: TRANSMIT TIME SLOT: 0/1/2/--/63: The entered value in the range 0-63 in integer steps, sets the selected SLAC transmit time slot for PCM data.

Para 17: TRANSMIT TIME SLOT: NORM/EXPAND: Sets the selected SLAC transmit PCM format to Normal (0-31) or expanded (32-63) mode of operation (refer to Data Sheet for format description).

Para 18: TRANSMIT CLOCK OFFSET: 0/1/-/7: The Transmit PCM of the selected SLAC will be offset by an integer number of PCM clock periods, depending on the selected value.

Para 19: PCM ASSOCIATE: DXA/DXB: Transmit PCM of the selected SLAC will appear at the indicated PCM port.

Paras 20 to 30: Note that the SLAC has complementary types of parameters for the receive path as for the transmit path. Thus there are equivalent parameters available on the SETUP SCREENS (right hand half of upper box - see figure 7) for Receive Gain. Receive Filter status, Receive Filter A0-A3 values, Receive Time Slot, Receive Clock Offset and Receive PCM Port Associate. There are additional parameters applicable only to the Receive Path, which are included in the continuation below, of SETUP SCREENS parameters.

Para 31: RECEIVE PATH DISABLE: NO/YES: This will send the diagnostic code for receive path disable if set to YES. The NO condition clears this state (see also Diagnostic Code Control description).

Para 32: RECEIVE PATH ATTENUATE: 0dB/-6dB: Setting to -6dB sends the diagnostic control code to set 6dB attenuation in the receive path (see also SLAC Data Sheet). Setting to 0dB clears this condition (see also Diagnostic Code Control description).

Para 33: C FILTER STATUS: DISABLED/ENABLED: This is used to enable or disable the selected SLAC C FILTER as set.

Para 34, 35, -, 43: PREPROGRAM A0, A1, -, A9: 'VALUE', VALUE',-, 'VALUE': These are ten numbers listed across the screen, each with a Value in the range -2048 to + 2047 in integer steps, representing the selected SLAC C Filter coefficients. Normally values are in the range ±2 but they are normalised to 1024 for convenience. The values may be displayed in HEX format by using the F9 Key on the SETUP SCREENS. Note that it is this set of coefficients that will be preprogrammed from the *.SET file of the automatic preprogram calculation routine on the MAIN MENU (applicable to SLAC1 only).

Data 1, Data 2, -, Data 10: FOREGROUND A0, A1, -, A9: 'VALUE', VALUE',-, 'VALUE': Listed underneath the preprogram values for C Filter coefficients are the ten numbers (also normal to 1024 or HEX format) that represent the foreground C Filter coefficients. These are read from the SLAC at a rate determined by the READ RATE parameter. Actual values may of course vary from the preprogram data depending on the occurrence of C Filter adaption.

Para 44: C FILTER DOUBLE TALK: 'VALUE': A number in the range -2048 to +2047 sets the selected SLAC C Filter Double Talk Coefficient (see description in SLAC Data Sheet). Normally the value is in the range ±2 but it is normalised to 1024 for convenience. The value may be displayed in HEX format by using the F9 Key on the SETUP SCREENS.

Para 45: C FILTER ADAPTION: DISABLED/IF SI HI/ENABLED: This parameter controls the adaptive process on the selected SLAC C Filter. Disabled implies no adaption, Enabled implies adaption and IF SI HI implies that adaption occurs when the SI Input is high (see also description in device Data Sheet).

Para 46: C FILTER CORRELATER: DISABLED/ENABLED: The selected SLAC C Filter correlator can be disabled or enabled (using the SLAC diagnostic control codes) as set by this parameter (see also Diagnostic Code Control description).

Diagnostic Code Control

Within each setup screen a number of SLAC diagnostic codes can be set for the associated device. Since the diagnostic codes contain only a master reset code to reset all diagnostic conditions and no codes to reset individual conditions, the following procedure is adopted. Each time a diagnostic condition is changed, all of the diagnostics will first be reset by sending code B0 via DI/O. The status of all diagnostics is then retransmitted according to the settings on the screen.

Default Settings

The parameter default settings as associated with the F5 Key for the SETUP SCREENS are listed in the SLAC Data Sheet, and will be as for the first application of power. These are also the default settings used to create the file "LASTAUTO.SET" when the program runs for the first time (i.e. F4 Key on MAIN MENU).

SCAMP ERROR MESSAGES

In order to assist the user in fault diagnosis, a number of error messages have been built into the SCAMP software. These are so designed to aid identification of any problems with the associated hardware and/or software environment. The main error messages that can occur are briefly described below. Note that they may occur separately or in combination with other messages.

"MISSING CONFIG FILE - CREATING ONE CALLED SLAC.CON"

Usually occurs when the program is run for the first time and no configuration file exists. The program creates one using the default settings.

"CANNOT WRITE TO DEFAULT DIRECTORY - ABORTING"

This will usually occur if the disk containing the SLAC.CON file is write protected.

"NONEXISTENT PORT"

The selected parallel printer port of the PC does not exist or an illegal entry has been entered.

"DISK IS WRITE PROTECTED"
"DRIVE NOT READY"
"FILE DOES NOT EXIST"
"PATH NOT FOUND"
"ERROR READING FILE"

These are occurrences of the DOS error messages.

"NO / INCORRECT RESPONSE FROM SLAC"

Occurs during checks of the control port of the SLACs on the circuit board and implies write to and subsequent read back of coefficients has failed.

"SORRY NOT IMPLEMENTED YET - TO BE INCLUDED IN A LATER RELEASE"

This function key has no operation associated with it, but may do in future SCAMP issues.

"FILE ACCESS ERROR"

This normally occurs in association with one of the DOS error messages.

"NOT A VALID FILE FOR THIS OPERATION"

Each file in SCAMP contains a header to identify the type of file for use in the program. This message implies an error in the header or no such header (i.e. not a SCAMP file).

"HARDWARE PROBLEM - FRAME SYNC SIGNAL NOT DETECTED"

The PCM frame sync signal on the circuit board is not functional or is disconnected; check hardware.

"SLAC TRANSMITTING PCM MAYBE IN STANDBY STATE - $FF PCM CODES RECEIVED"

The received PCM is at logic high state and a check on hardware operation should be made.

"CANNOT ACHIEVE MINIMUM ACCEPTABLE NULL - ABORTING MEASUREMENT SEQUENCE"

The C Filter automatic preprogram routine contains a target value for spot frequency measurements. If this minimum level of cancellation is not achieved for any one measurement frequency, then the process is aborted. A check should be made on the target line interface and/or associated hardware.

"NOT ENOUGH SPACE ON THIS DISK TO SAVE RESULTS"

Occurs if the program cannot find enough disk space to store data or results. Any unwanted files should be deleted to make space or a new SCAMP disk inserted.

"DATA PORT"
"CONTROL PORT"
"DATA AND CONTROL PORT"

These are error reports associated with the PC internal hardware, and occur during the hardware test routines to identify problems with the data port and/or control port of the selected I/0 port of the PC. Appropriate checks should therefore be made.

"CONTROL DATA HARDWARE SLAC N"

Occurs during testing of the control interface to the circuit board, and may be associated with other error messages. Appropriate checks should therefore be made.

"PCM HARDWARE SLAC N
CHECK CLK1, CLK2 ARE CONNECTED TO PCFS ON CONNECTOR BLOCK OR PC MAY NOT BE FAST ENOUGH OR OTHER PROBLEM"

Identifies problems associated with the PCM interface to the circuit board, and appropriate checks should be made.

"ANALOG LOOP CHECK, SLAC N"

Identifies the SLAC undergoing analog loop verification, and occurs as part of any error report should verification fail.

"SLAC N"

Occurs as part of an error report to identify a given SLAC.

"H/W ERROR. FRAME SYNC SIGNAL IS NOT ASSERTED"

Indicates that the FS signal is continually low and that the hardware should be checked.

"H/W ERROR. FRAME SYNC SIGNAL IS CONTINUALLY ASSERTED"

Indicates that the FS signal is continually high and that the hardware should be checked.

"NOT ENOUGH MEMORY TO CREATE PCM TEST SEQUENCE"

During testing of the PCM transmission capability, a PCM sequence is generated and results of received PCM stored for analysis. This indicates that memory space is insufficient for this to take place and corrective measures will be required.

"PCM HARDWARE MUST BE VERIFIED BEFORE TAKING MEASUREMENTS
GO TO CONFIG MENU TO RUN HARDWARE CHECKS"

When running preprogramming or ERL measurement routines the hardware status in the CONFIG menu should be verified. This indicates that the status is incorrect for these routines to be implemented and corrective action, as described, should be taken.

"NO GRAPHICS CARD DETECTED"

There is no graphics card in the PC or the program is unable to detect it. This will occur for example when trying to display ERL plots.

"ERROR WHILE ATTEMPTING INIT GRAPH"

This error message may occur if the graphics card is not a type that is catered for by SCAMP and therefore it cannot successfully be initialised.

MV3010-1 SLAC IN CT2/PORTABLE BASE STATIONS

INTRODUCTION

Following the introduction of the Common Air Interface (CAI) for CT2/Portable phones, there is a growing market for base stations meeting this standard. These can be of a subscriber specific nature or a public access basis, with handsets being usable via either route to the exchange. In each case the base station interfaces into the PSTN at the local 2 Wire (analog) loop. There are several problems associated with this connection, in addition to provision of consistent performance of the handset (particularly in association with sidetone levels). This Application Brief describes how the MV3010-1 SLAC can be used to overcome such difficulties.

DESCRIPTION

When designing the base station interface to the 2 wire loop, several parameters are unknown or changeable over the lifetime of the equipment. Thus, if the base station is to work as a subscriber specific piece of equipment, it must be capable of handling both unknown line lengths up to, and differing terminations in, the PABX/Exchange (dependent on the PTT administration). Whilst it is easy to design a circuit which will present a known/predetermined impedance to the exchange, the largely unknown/variable impedance seen by the base station can present a problem, particularly in the control of sidetone levels.

These problems are overcome by use of the MV3010 - 1 SLAC. The block diagram of Fig. 1 shows the basic application. Issues affecting the detailed design of the circuit are now discussed below.

Firstly, a standard telephone device (analog 2 wire-4 wire) can be used to provide a termination of the local loop. Such devices as are readily available on the market, provide control of transmit level by monitoring the loop current (which will vary with line length) and adjusting the gain accordingly. If a nominal exchange + line impedance is assumed (e.g. 600 Ohm + 3km cable) the telephone chip can be set to give an initial sidetone cancellation. Since this device is interfaced to the MV3010-1 4 wire port, the C Filter is now readily used to provide further sidetone cancellation in the PCM signal which is being transmitted to the handset. Even if the telephone device only gives an initial 6 dB sidetone cancellation, the MV3010-1 C Filter can adapt to changeable line conditions to maintain an overall figure of some 25 or 30 dB. This may or may not involve preprogramming initial conditions into the C Filter, improving the results of adaptation. Preprogramming of the C Filter is fully supported by GPS via the SLAC Evaluation Package (see Application Note AN111-2). If a circuit to provide local sidetone in the handset is used, predictable and reliable control of sidetone level will result.

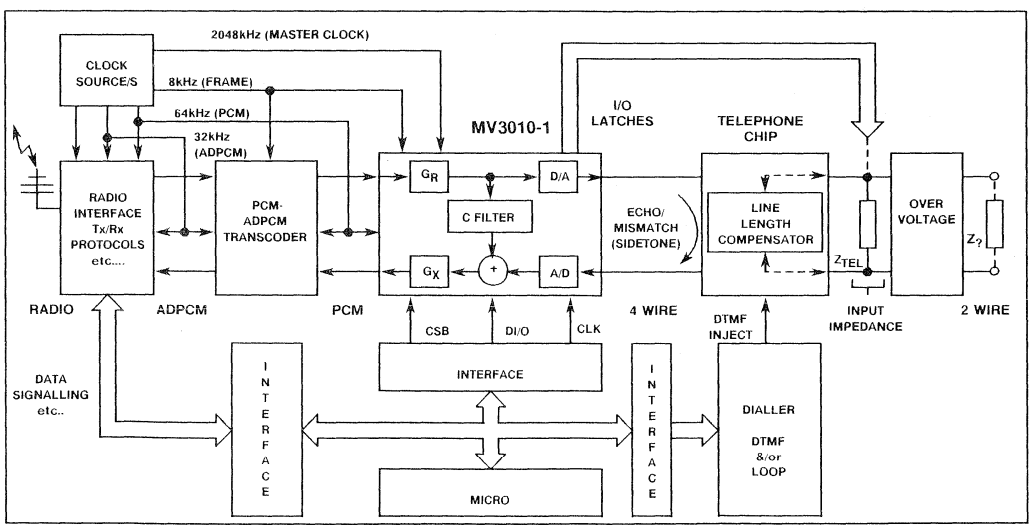


Fig. 1 Block diagram of base station using MV3010-1

Also note that since cancellation of sidetone is done in the base station, the typical 20-30 ms (or greater) delay in the mouthpiece-base station-earpiece loop will present no problems in this solution.

Since the MV3010-1 provides a PCM 'backplane' (normally expected to interface to an exchange backplane) this can be used to connect to a PCM transcoder device providing the necessary 32Kbit ADPCM required by the radio link to the handset. This second feature of the MV3010-1, together with the C Filter, provides a readily available solution to many of the problems associated with the base station design.

Additional features of the MV3010-1 can be used to give other functions. These include use of the Transmit and/or Receive Gain stages for control of signal levels, programming of Transmit and/or Receive Filters for modification of frequency response and use of the I/O Latches for switching/enabling functions in the base station. For example, software in the micro which controls the circuit, could be used to switch the I/O Latches and select (e.g. via analog switches) a given impedance to be presented to the exchange. This would allow one hardware design the capability of satisfying various PTT requirements. Indeed, one use of an I/O Latch could be to provide equivalent hook status in the base station.

The signalling in the radio link would normally be handled by the micro. Thus dialling data can be read by the software and the micro then used to drive a standard DTMF generator/loop dialler.

Since many of the telephone chips are designed with a DTMF input, this readily allows injection of such signalling onto the 2 wire line. Some of these devices are also capable of providing loop disconnect dialling, whilst others contain DTMF generation on chip.

Let us now consider some of the points concerning the digital aspects of the circuit (i.e. the PCM/radio link). First we note that the radio link requires data rates (and hence clocking) based on 72kHz and divisions of 64kHz (i.e 32kHz, 8kHz, 2kHz, 1kHz). The MV3010-1 needs a Master Clock at 2048kHz (note that PCM may be clocked in/out between 64kHz and 4096kHz) to work correctly (i.e. 256 clock edges per transmit frame sync which is at 8kHz). All these clock rates can be derived from a source at 18.432MHz (crystal standard frequency) and will thus be phase locked. This is required since none of the circuitry in the base station can handle completely asynchronous data/clocks (there is no slip/frame alignment capability between MV3010-1, transcoder and radio interface).

Lastly, we consider the difference between a subscriber specific design and that for a public base station. This will primarily be a result of the number of subscribers interfaced to the PSTN. To expand the basic circuit, one analog interface to the exchange/PABX is required per subscriber. Again, the MV3010-1 is used to provide control of sidetone for each subscriber link. A number of such 2 wire to ADPCM circuits can now be connected to the radio interface which is so designed to provide multiple channel communication to the users.

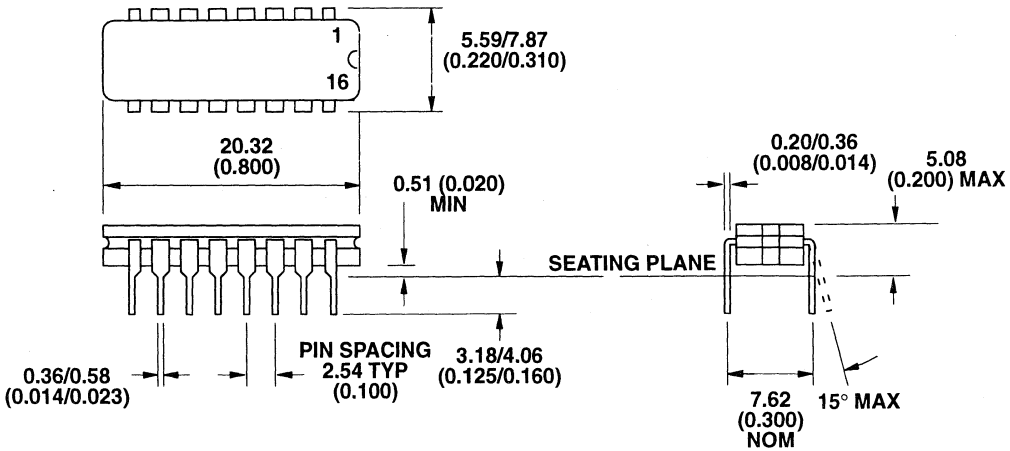
DEVICE TYPE	DEVICE NUMBER	MANUFACTURER
4 Wire - PCM with Echo Cancellation	MV3010-1	GPS
DTMF Dialler DTMF/pulse Switchable Dialler Micro Interface Dialler	MV5087/9 MA541 series MA525	GPS GPS GPS
Radio/Handset parts	Refer to Personal Communications Handbook (HB2123)	GPS
Transcoder	MC145532 D77521 GC	Motorola NEC
Telephone Chip	TCM1715/45 (DTMF inject) TEA1066 (=//=) MC34014 (=//=) PSB4500 series (=//=) TCA3383/8 (DTMF/Loop inject) TCA3386 (Including DTMF) TEA7036/7 (=//=) TEA3046/7 (=//=)	Texas Philips Motorola Siemens Motorola =//= Thompson =//=

Table 1: Suitable devices for base station circuit.

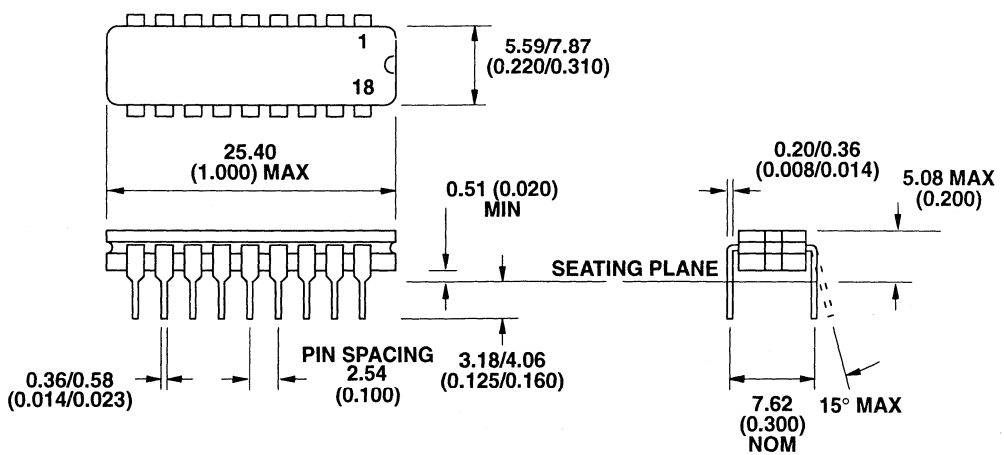
Section 6
Package Outlines

Dimensions are shown thus: mm (in).
For further package information, please contact your local Customer Service Centre.

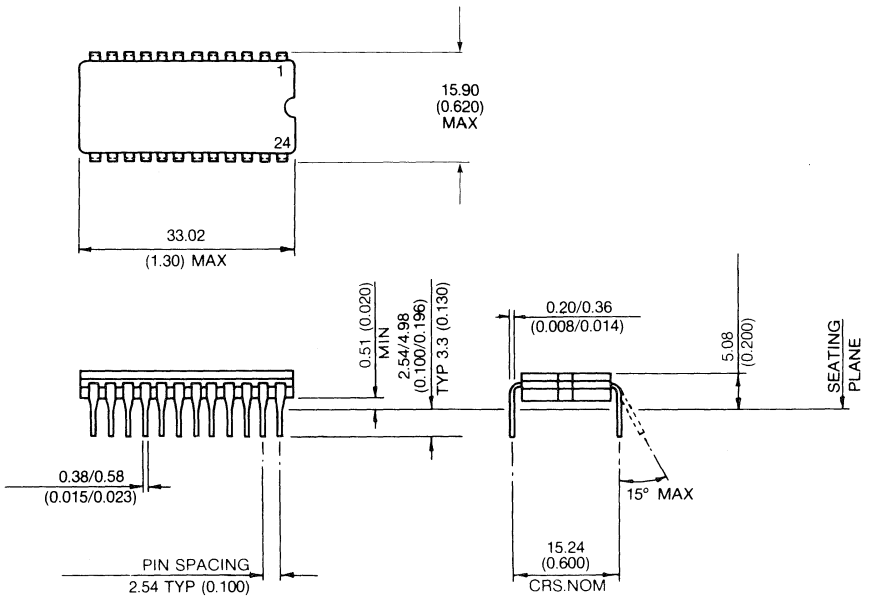
GEC PLESSEY
SEMICONDUCTORS



16-LEAD CERAMIC DIL - DG16



18-LEAD CEARMIC DIL - DG18



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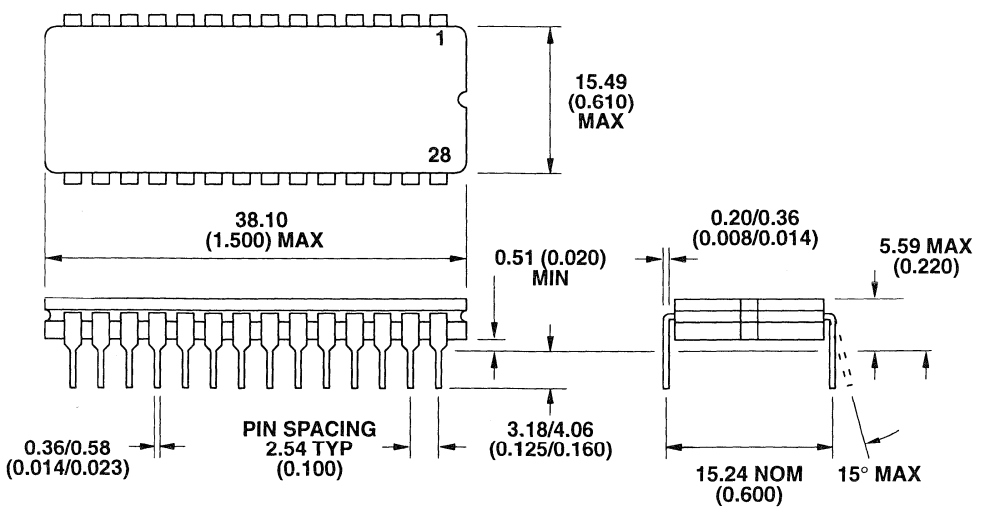

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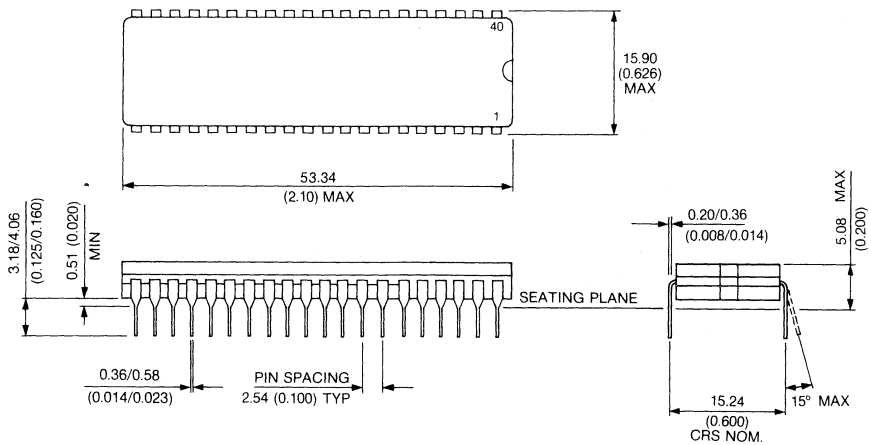

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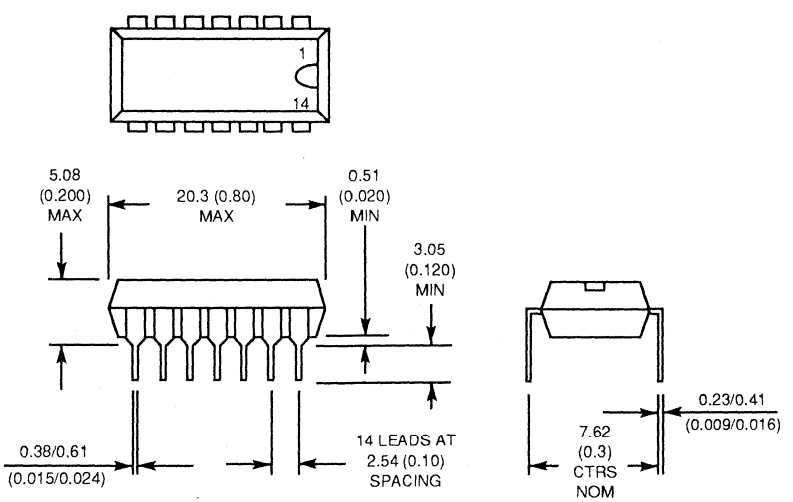
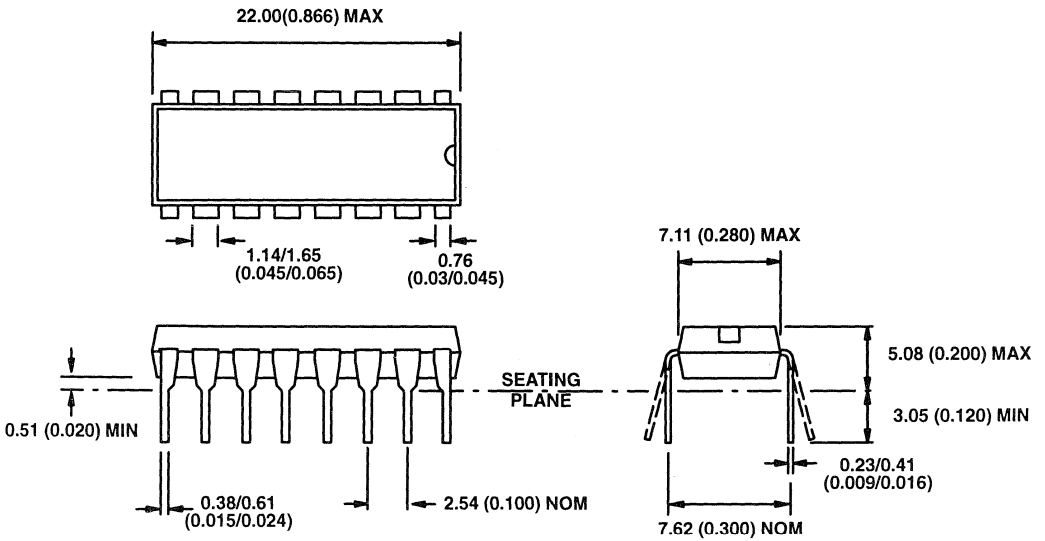


14-LEAD PLASTIC DIL - DP14



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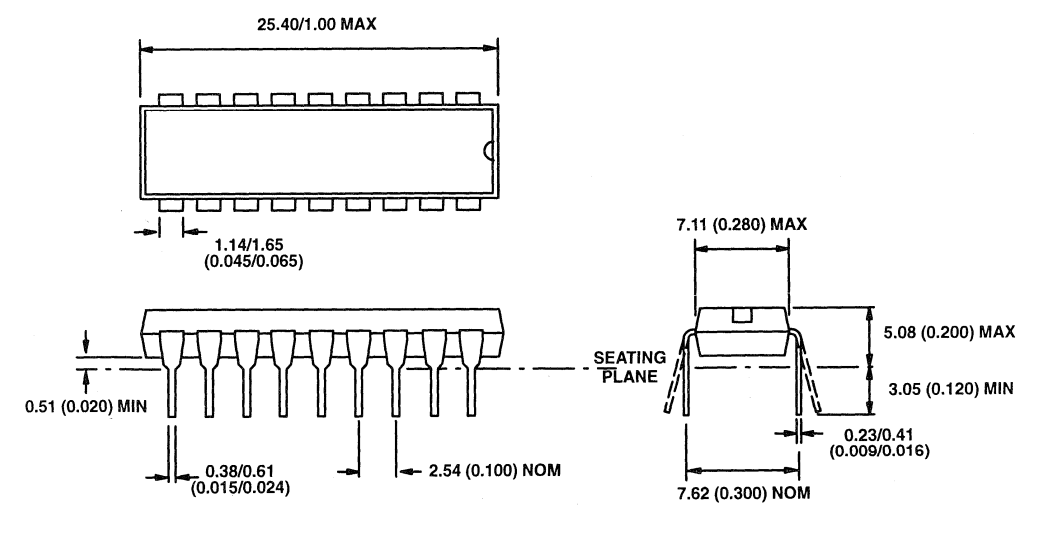

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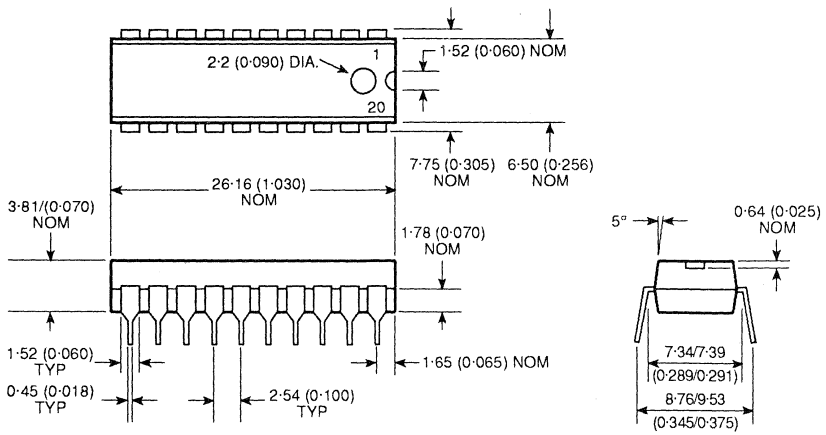

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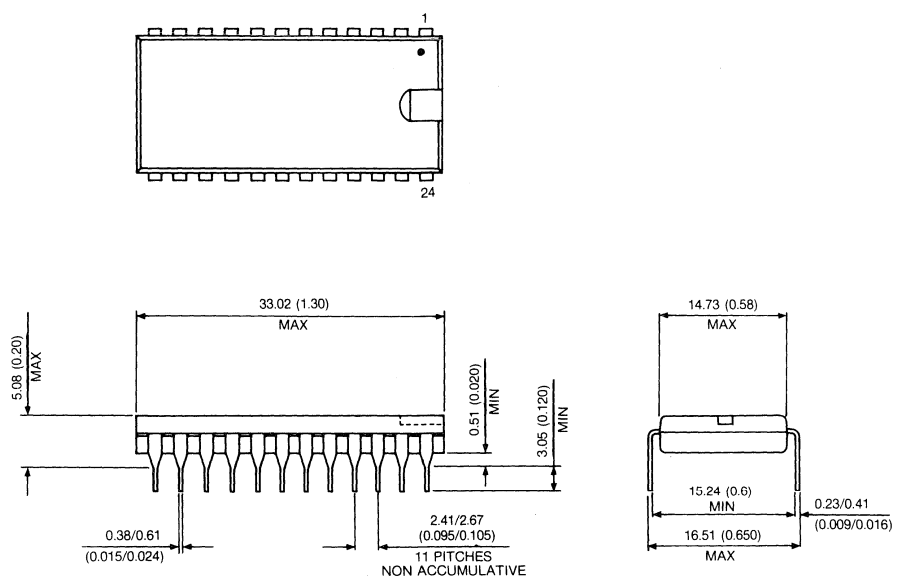

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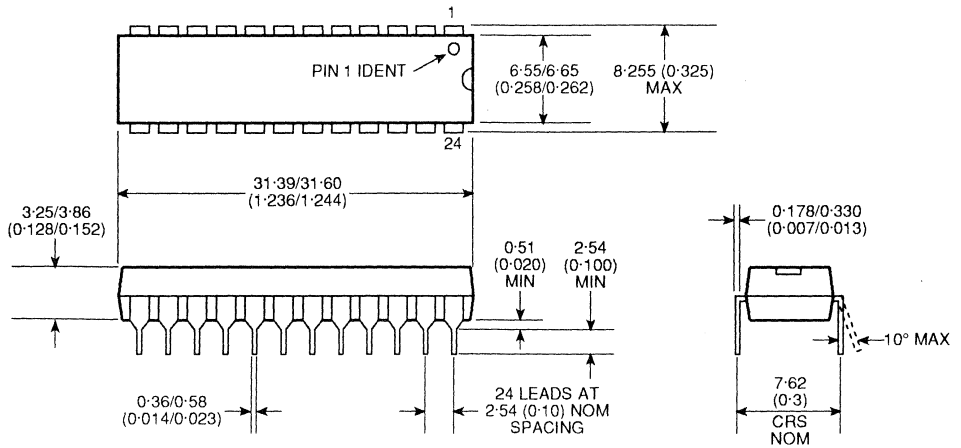

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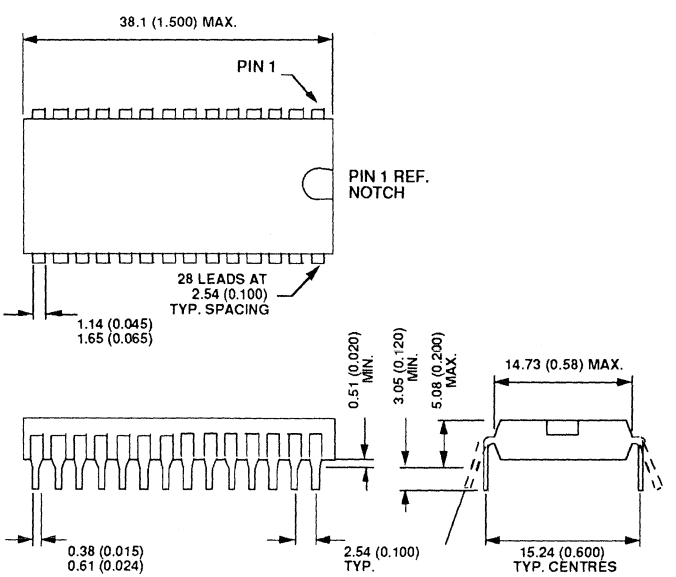

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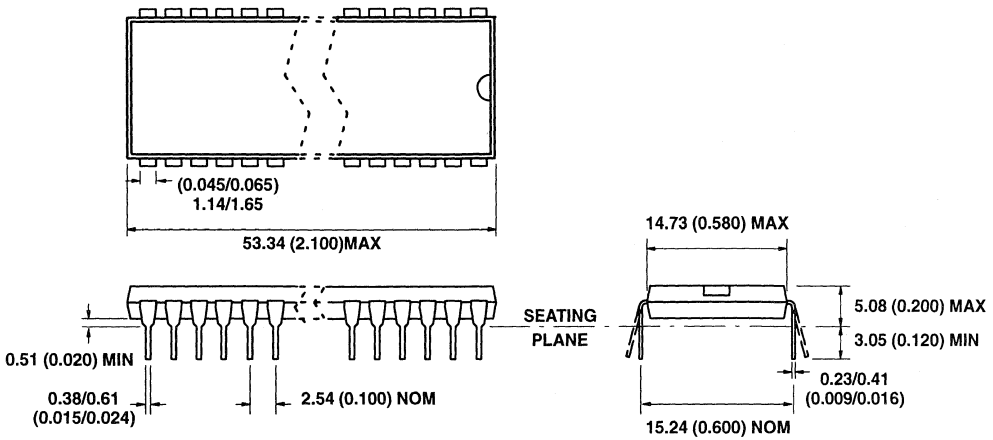

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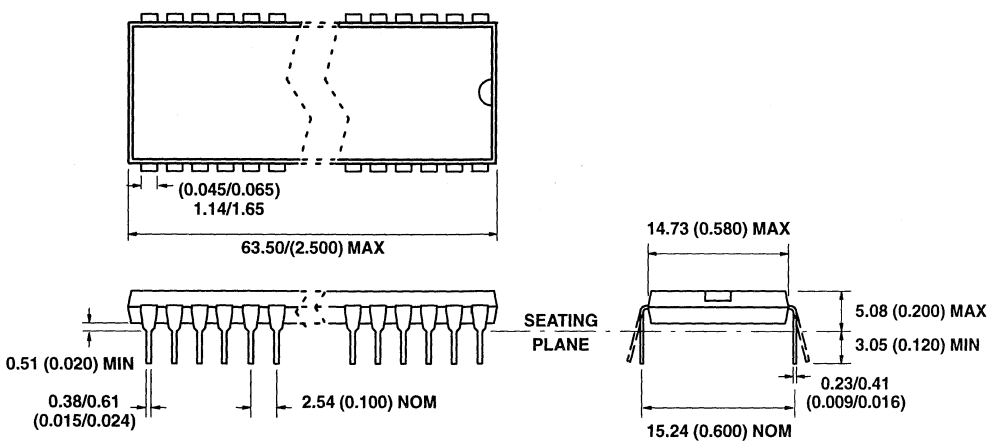

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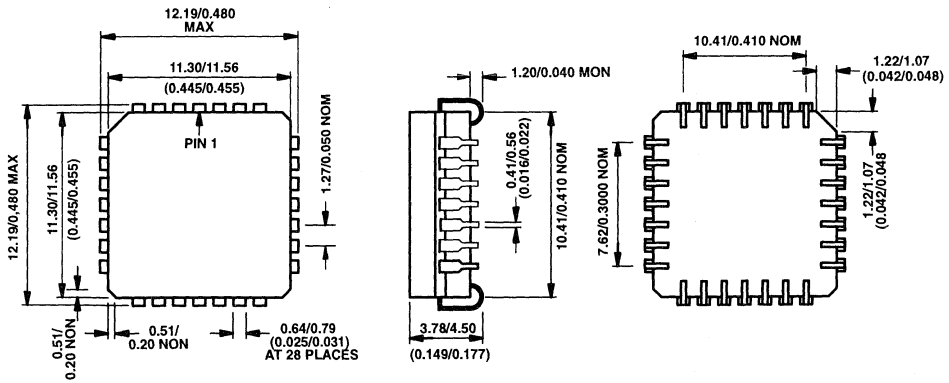
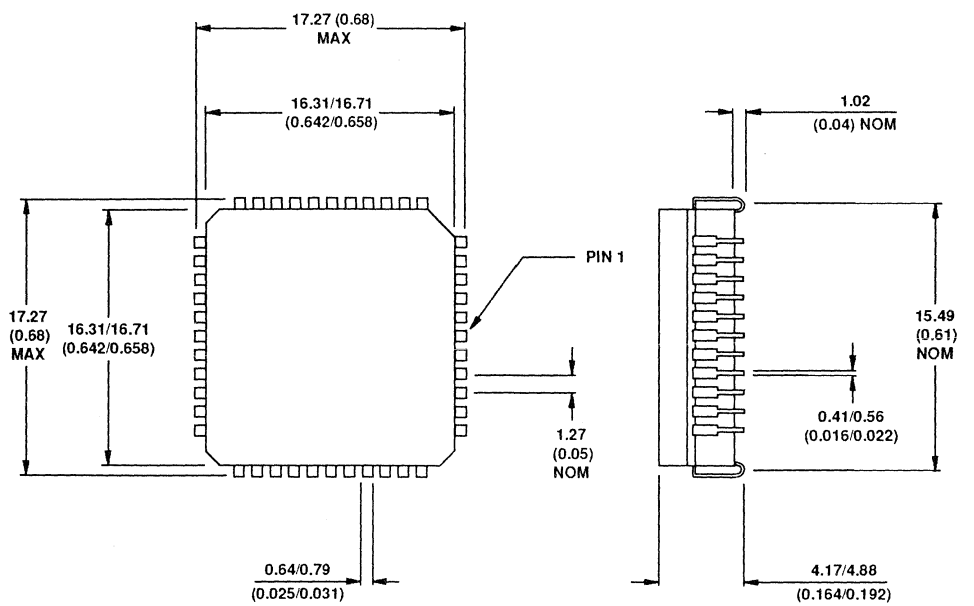
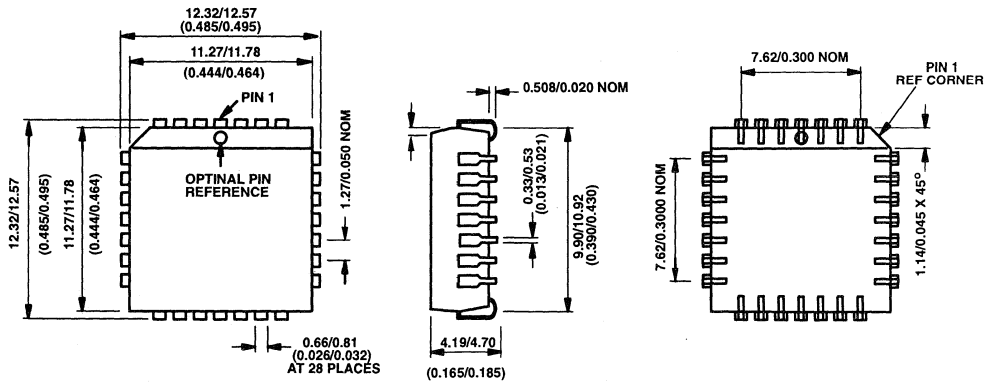


28-LEAD QUAD CERPAC CHIP CARRIER - HG28



44-LEAD QUAD CERPAC CHIP CARRIER - HG44



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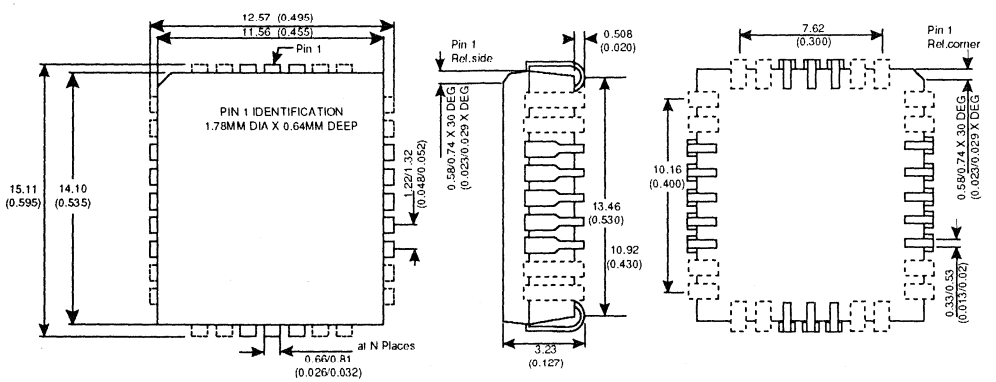

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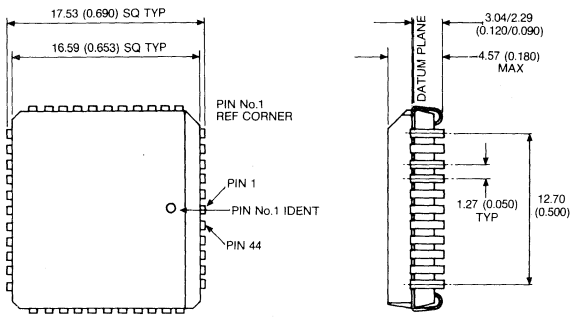

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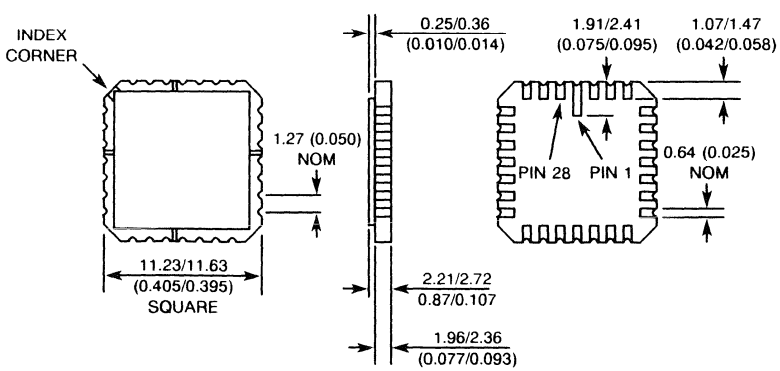
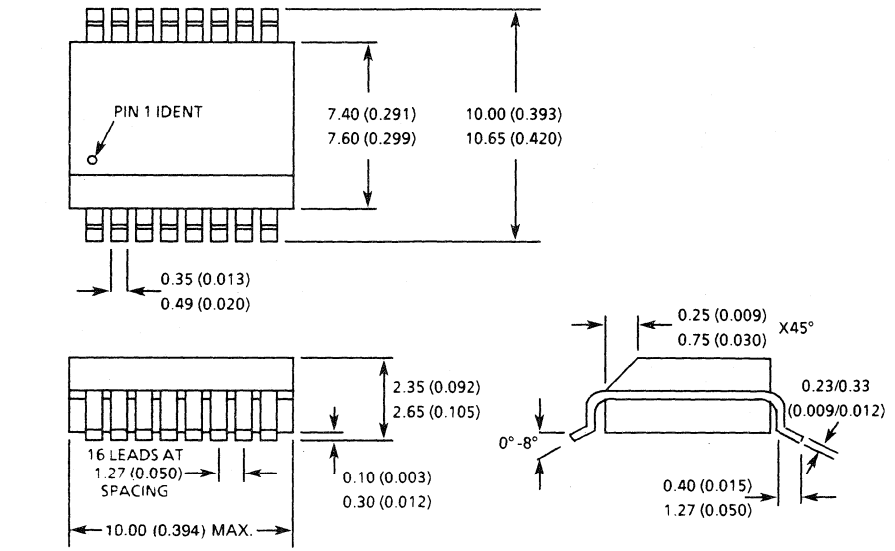
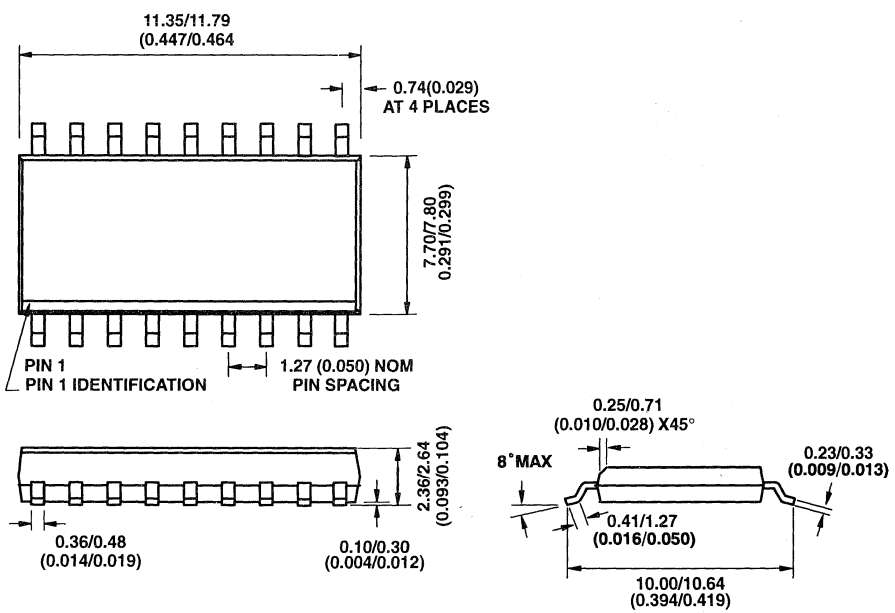


28-PIN LEADLESS CHIP CARRIER - LC28



16-LEAD MINIATURE PLASTIC DIL (WIDE BODY) - MP16/W



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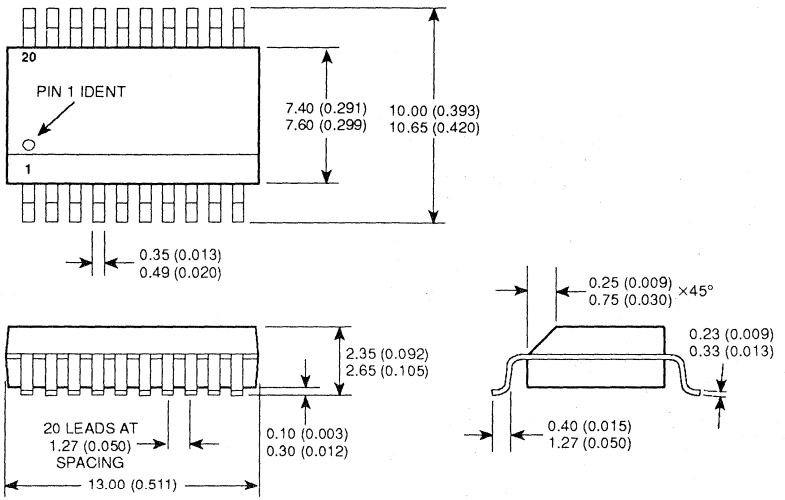

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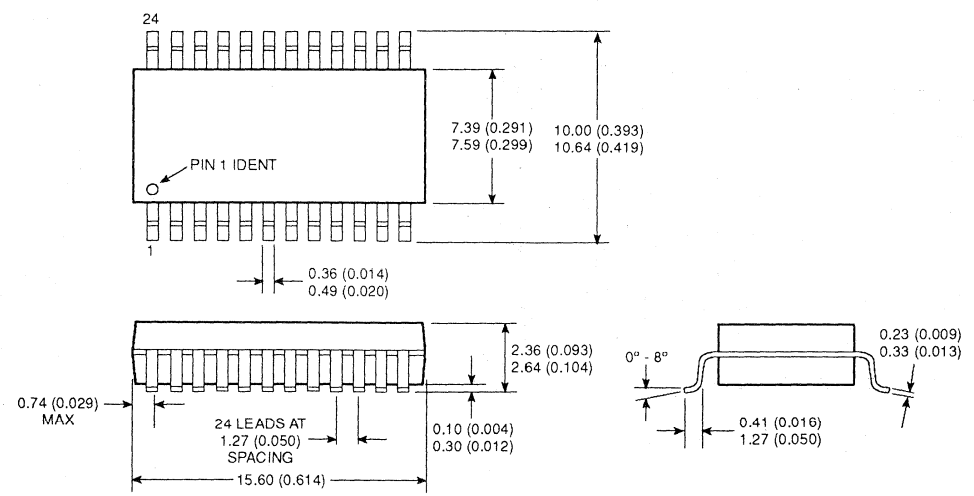
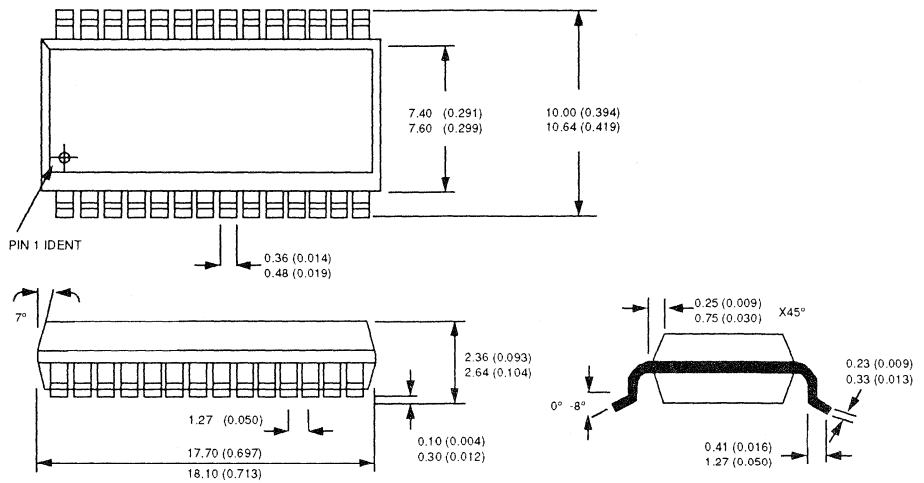
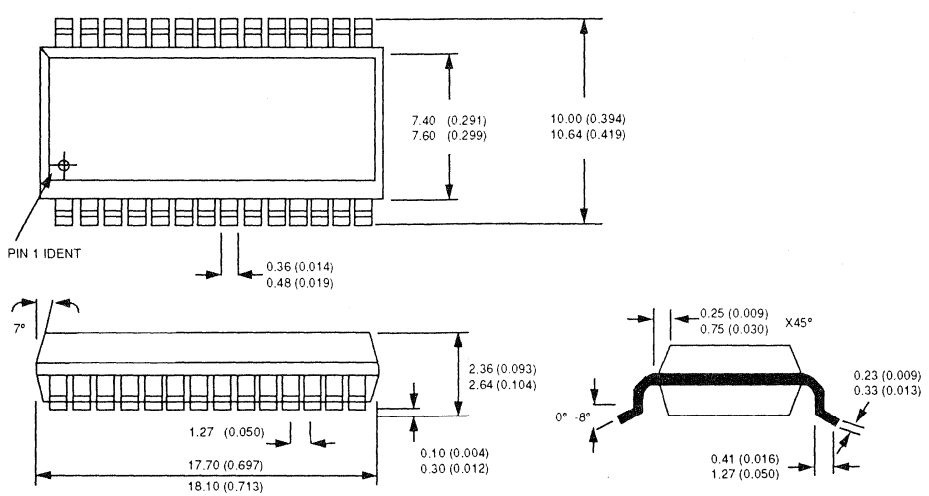


24-LEAD MINIATURE PLASTIC DIL (WIDE BODY) - MP24/W



28-LEAD MINIATURE PLASTIC DIL - MP28



28-LEAD MINIATURE PLASTIC DIL (WIDE BODY) - MP28/W

Section 7
GPS Locations

GEC PLESSEY
SEMICONDUCTORS

Headquarters Operations

UNITED KINGDOM	Cheney Manor, Swindon, Wiltshire, United Kingdom, SN2 2QW. Tel: (0793) 518000 Fax: 0793 518411
NORTH AMERICA	P O Box 660017, 1500 Green Hills Road, Scotts Valley, California 95067-0017, USA. Tel:(408) 438 2900 Fax: (408) 438 5576

Customer Service Centres

FRANCE & BENELUX	Z.A. Courtaboeuf, Miniparc-6, Avenue des Andes, Bat. 2-BP 142, 91944, Les Ulis Cedex A. France.Tel: (1) 64 46 23 45. Fax: (1) 64 46 06 07
GERMANY, AUSTRIA and SWITZERLAND	Ungererstraße 129, 80805 Munchen 40, Germany. Tel: 089/36 0906-0. Fax: 089/36 0906-55
ITALY	Via Raffaello Sanzio, 4, 20092 Cinisello Balsamo (MILAN). Tel: (02) 66040867. Fax: (02) 66040993.
JAPAN	CTS Kojimachi Building (4th Floor), 2-12, Kojimachi, Chiyoda-ku, Tokyo 102. Tel: (03) 5276-5501. Fax: (03) 5276-5510.
NORTH AMERICA	P O Box 660017, 1500 Green Hills Road, Scotts Valley, California 95067-0017, USA. Tel: (408) 438 2900. Fax: (408) 438 7023
SOUTH EAST ASIA	No. 3 Tai Seng Drive, GEC Building, Singapore 1953. Tel: (65) 3827708. Fax: (65) 3828872
SWEDEN	Katarina Bangata 79, 116 42 Stockholm. Tel: 46 8 7029770. Fax: 46 8 6404736
UK, EIRE, DENMARK, FINLAND and NORWAY	Unit 1,Crompton Road,Groundwell Industrial Estate, Swindon, Wilts, U.K., SN2 5AF. Tel: (0793) 518510. Fax: (0793) 518582. **Power Division** Carholme Road, Lincoln, U.K., LN1 1SG. Tel: (0522) 510500. Fax: (0522) 510550

North American Sales Offices

NATIONAL SALES	P O Box 660017, Scotts Valley, CA 95067-0017. Tel: (408) 438-2900. ITT Telex: 4940840. Fax: (408) 438-5576.
EASTERN	Two Dedham Place, Suite 1, Allied Drive, Boston, MA 02026. Tel: (617) 320-9790. Fax: (617) 320-9383.
WESTERN	1735 Technology Drive, Suite 100, San Jose, California 95110. Tel: (408) 451-4700. Fax: (408) 451-4710.
ARIZONA/NEW MEXICO	4635 South Lakeshore Drive, Tempe, AZ 85282. Tel: (602) 491-0910. Fax: (602) 491-1219.
SOUTH CENTRAL	9330 LBJ Freeway, Ste. 665, Dallas, TX 75243. Tel: (214) 690-4930. Fax: (214) 680-9753.
NORTHWEST	7935 Datura Circle West, Littleton, CO 80120. Tel: (303) 798-0250. Fax: (303) 730-2460.
DIXIE and FLORIDA	668 N. Orlando Ave., Suite 1015 B, Maitland, FL 32751. Tel: (407) 539-1700. Fax: (407) 539-0055. 385 Commerce Way, Longwood, FL 32750. Tel: (407) 339-6660. Fax: (407) 339-9355.
SOUTHWEST	2600 Michelson Drive, Suite 830, Irvine, CA 92715. Tel: (714) 852-3900. Fax: (714) 852-3910.

DISTRIBUTION SALES	1500 Green Hills Road, Scotts Valley, CA 95066. Tel: (408) 438-2900. ITT Telex: 4940840. Fax: (408) 438-7023.
CANADA	3608 Boul. St. Charles, Suite 9, Kirkland, Quebec, H9H 3C3. Tel: (514) 697-0095. Fax: (514) 694-7006.
	Shucho-Gu, CPO Box 7981, Seoul. Tel: 2 595 9101-6. Tx: K25981 KMLCORP. Fax: 2 595 9107.

Semi-Custom Design Centres

AUSTRALIA	Unit 1, 38 South Street, Rydalmere, NSW 2116, Australia. Tel: 612 638 1888. Fax: 612 638 1798.
FRANCE & BENELUX	Z.A. Courtaboeuf, Miniparc-6, Avenue des Andes, Bat.2-B.P. No.142 91944 Les Ulis Cedex A, France.Tel: (1) 64 46 23 45. Fax: (1) 64 46 06 07.
ITALY	Via Raffaello Sanzio, 4, 20092 Cinisello Balsamo (MILAN). Tel: (02) 66040867. Fax: (02) 66040993.
GERMANY	Ungererstraße 129, D 80805 Munchen 40. Tel: (089) 3609 06 0. Fax: (089) 3609 06 55.
JAPAN	CTS Kojimachi Building (4th Floor), 2-12, Kojimachi, Chiyoda-ku, Tokyo 102. Tel: (03) 5276-5501. Fax: (03) 5276-5510.
N AMERICA: Canada	**Alberta Microelectronics Center,** 3553 31st St., N.W., Calgary, Alberta T2L2K7. Tel: (403) 289-2043.
	Microstar Technologies, 7050 Bramelea Rd., #27A Mississaugo, Ontario L5SITI Canada. Tel: (416) 671-8111
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